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Degradation of Atomic Surface Flatness of SiO_2 Thermally Grown on a Si Terrace

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In this study, the atomic-scale roughness and uniformity of SiO_2 thermally grown on an atomically flat Si surface were investigated. The SiO_2 surface roughness increased with increasing oxide thickness in the initial rapid oxidation region of the Deal–Grove model. This roughness growth was a result of reoxidation of SiO species near the SiO_2 surface, which were emitted from the Si/SiO_2 interface during oxidation. However, the surface roughness growth is saturated in the linear-rate oxidation region. This is because the emitted SiO species within the SiO_2 were reoxidized without thickness increment, and the generated oxidation stress was absorbed within the film. Although the amount of the emitted SiO decreases by the surpassing relaxation effect, the surface roughness is kept without shrinking. An incubation period before the onset of roughening was found, during which the surface roughness remained unchanged.
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As the downsizing of metal-oxide-semiconductor field-effect transistors (MOSFETs) progresses, the dispersion of gate leakage currents among narrow gate electrodes becomes enhanced even if accidental external defects of metallic contamination,[1] crystal-originated particles,[2,3] and so on are not included in the gate SiO_2 films.[4] However, there have been many reports of time-dependent change in gate or flatband voltage under the application of constant-current stresses, that is, an average degradation has been discussed.[5] However, a dielectric breakdown, even in a clean thin SiO_2 film, is a local phenomenon. This has been confirmed by the observation that the gate electrode after dielectric breakdown is locally removed.[6] These results indicate that the distribution of dielectric degradation of the gate SiO_2 films after the application of high electric stress is not two dimensionally uniform on an atomic scale.[7] Thus, the dielectric degradation has not only an average component but also a two dimensionally distributed component.[8]

Okamoto et al. reported using an evaluation method named stress-induced etched-oxide surface roughness that electrical stress induced a two dimensionally distributed roughness on surfaces of SiO_2 films partially etched away in diluted HF due to nonuniformity of trapped charges in the SiO_2 films.[8] The two-dimensional nonuniformity of the degradation increased with increasing injection of charges during the stress application. However, the origin of the two-dimensional distribution of the time-dependent degradation is not yet clear.

It has been reported that the percolation model can explain why the distribution of the time-dependent dielectric breakdown lifetime increases with decreasing thickness of thermally grown SiO_2 films. The percolation model, however, does not refer to a specific origin of the nonuniform charge trapping in thermally grown SiO_2 films.[9]

Chen et al. suggested the presence of a weak area in which holes are easily trapped.[10] It is reasonable to consider gate oxide thinning as the origin of the weak area. At the top convex corner or the bottom corner of the silicon trenches, oxide thinning and concentration of the oxide electric field occur, followed by the short time of dielectric breakdown.[11,12] However, there have been few reports that the two-dimensional distribution of dielectric breakdown lifetime or gate leakage current is due to the atomic-scale nonuniformity of the SiO_2 films on the planar silicon surface.[13]

To discuss the atomic-scale nonuniformity of thermally grown SiO_2 film thickness, the SiO_2 films must be grown on an atomically flat silicon surface. Hahn and Henzler reported that Si/SiO_2 interface roughness in thermally grown SiO_2 on a mirror-polished Si surface changed, depending on the oxidation conditions over an oxide thickness range of more than 3 nm, based on low energy electron-diffraction observations.[14] However, it has been reported that the thermal oxidation of the Si surface progresses in a layer-by-layer mode.[15] However, there are some phenomena, such as the oxidation of the Si trench corner[11] and the disappearance of the atomic step lines of the Si/SiO_2 interface that cannot be explained by strict layer-by-layer oxidation.[16,17] If the layer-by-layer oxidation was strictly sustained, oxidation should progress, keeping the similar interface topography. Based on a precise evaluation, thermal oxidation, roughly speaking, progresses in a layer-by-layer manner, although strictly speaking, it progresses via multilayer oxidation.[17]

To suppress the leakage current distribution and improve the reliability of thermally grown SiO_2 films in a miniaturized MOSFET, the atomistic mechanism of the two-dimensional roughness growth must be understood.

In this study, we investigate the roughness of the surface and interface of thermally grown SiO_2 on an atomically flat Si surface.

Experimental

(111)-oriented, Czochralski-grown, mirror-polished Si wafers were used. After modified RCA cleaning, the wafers were immersed in ultralow dissolved-oxygen water (LOW).[16,18,19] We more easily obtained the well-defined surfaces covered with single atomic steps and atomic terraces on the (111)-oriented Si surface than on other crystal orientations. The terrace width after the LOW treatment depended on the miscut angle. A terrace width of more than 500 nm can be obtained on a Si surface with a miscut angle of less than 0.03°. Such an atomically flat wide terrace surface enabled us to investigate the atomistic phenomena of the thermal oxidation, which could be clarified in the root-mean-square (rms) range of less than 0.1 nm.

After LOW immersion, the Si wafers were thermally oxidized in dry O_2 ambient at 600 and 1000°C. The oxide thicknesses were measured by ellipsometry. The SiO_2 surface topographies were observed using atomic force microscopy (AFM). The Si/SiO_2 interface topographies were observed after removal of SiO_2 films by a diluted HF solution. It was confirmed that the terrace surface was stable for immersion in the diluted HF solution to remove the SiO_2.[17] The rms values of the surfaces and interfaces were measured in areas of 200 nm square within an atomic terrace. An average of the rms values from at least three areas was applied as a typical rms.

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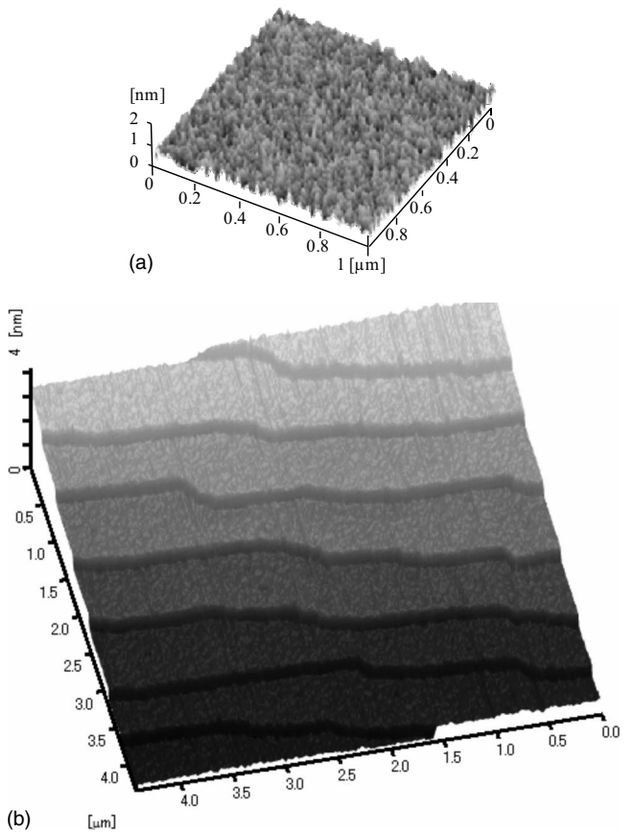

Figure 1. Typical AFM surface images of (a) as-received mirror-polished silicon and (b) LOW-treated silicon. The rms value of (a) is more than 0.1 nm, while the rms within a terrace of (b) is less than 0.05 nm.

Results and Discussion

Well-defined surface structures.— Figure 1a shows a typical AFM image of an as-received mirror-polished silicon wafer surface. The rms value of the surface is more than 0.1 nm, so, clearly the surface is not atomically flat. To investigate the SiO_2 surfaces and interfaces on an atomic scale, the initial silicon surface should be atomically flat. During the LOW treatment, OH ions in the water attack various Si–H bonds on the surface of the mirror-polished wafer. Among various Si–H bonds, the vertical Si–H bonds, which terminate the silicon atoms at the terrace surface of the (111)-oriented silicon, are most stable.[20] After the LOW treatment, a well-defined structure with a clear step/terrace appears on the Si surfaces, as shown in Fig. 1b. The atomic step height is approximately 0.3 nm corresponding to the spacing of the lattice plane. The height histogram within an area of 200 nm square on the terrace can be fitted by a sharp Gaussian peak.[17] The rms value of the silicon surfaces within a terrace is less than 0.05 nm, much less than that of the mirror-polished Si surface.

Oxidation at 600°C.— Figure 2 shows typical AFM images of the surfaces and interfaces of SiO_2 thermally grown at 600°C in dry O_2 ambient with various oxide thicknesses. The oxide thicknesses are 0.7, 1.1, 1.4, and 2.2 nm. Color contrast in all images represents the same height range. In the surface images of 0.7 nm thick oxide, small dark spots and bright spots are observed. At the former, oxidation is delayed, while at the latter oxidation is advanced. However, in the interface images, both small and large spots are observed in images of every oxide thickness. Figure 3 shows the rms values of the SiO_2 surface and interface topographies as a function of SiO_2 film thickness. The rms value of the initial silicon terrace surface is plotted at an oxide thickness of zero. The rms values change in the range of less than 0.1 nm. This indicates that the roughness growth mechanism cannot be precisely discussed until an atomically flat initial surface is obtained. The surface roughness gradually increases with oxide thickness in the region above 0.8 nm. For an oxide thickness of less than 0.8 nm, the rms remains at its initial value. This represents an incubation period of the SiO_2 surface roughness growth. However, the interface roughness initially increases rapidly but then is fluctuated within a width of approximately 0.01 nm around an average rms value of approximately 0.09 nm. The oxide surface roughness may have been influenced by the interface roughness because an oxide grows at the Si/SiO_2 interface with a volume increase, and the previously grown oxide film is pushed up from the interface. However, it is clear that there is the difference between both oxide thickness dependences of the surface and interface roughness. This means that the interface roughness is not necessarily the unique origin of the surface roughness. As described below, the increasing rate of the interface roughness is too rapid to be observed during oxidation at 600°C, while it is clearly observed at 1000°C. It seems that the influence of the interface roughness on the surface roughness changes depending on the oxidation conditions.

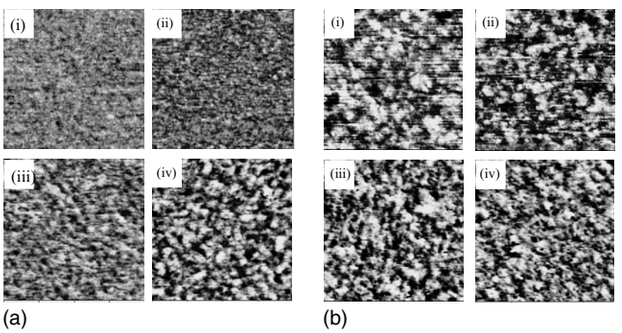

Figure 2. Typical AFM images of (a) surface and (b) interface of SiO_2 thermally grown on atomically flat silicon at 600°C in dry O_2 ambient. The SiO_2 thicknesses are (i) 0.7, (ii) 1.1, (iii) 1.7, and (iv) 2.2 nm. The scanning area is 200 nm square.

Oxidation at 1000°C.— In Fig. 3, it remained unclear to what extent the surface roughness growth trend continues. To investigate the surface roughness over a wide oxide thickness range from a few

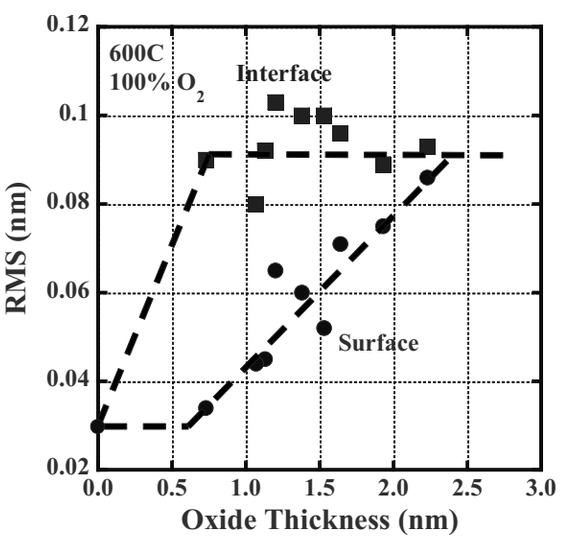

Figure 3. SiO_2 thickness dependence of rms values at the surface and interface of SiO_2 films thermally grown at 600°C in dry O_2 ambient.

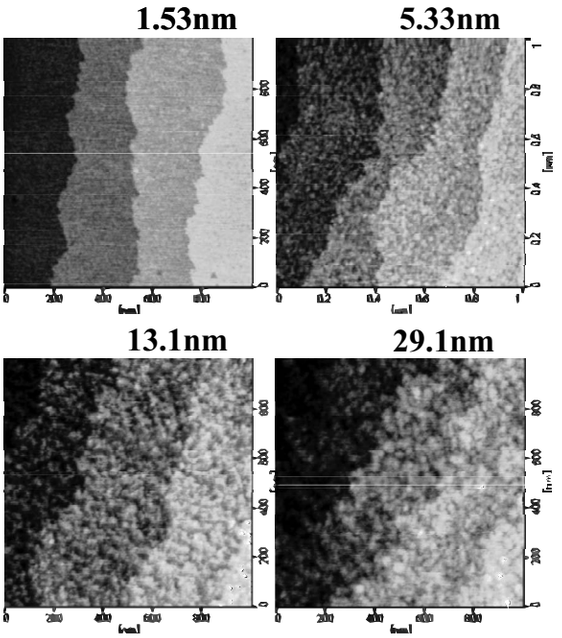

Figure 4. Typical AFM images of SiO_2 surfaces. The SiO_2 are thermally grown on an atomically flat Si surface at 1000°C in diluted 3.8% O_2 ambient.

nanometers to more than 10 nm, the atomically flat Si surface was thermally oxidized at 1000°C in a diluted 3.8% O_2 ambient. Figure 4 shows AFM images of the SiO_2 surface. Their oxide thicknesses are 1.5, 5.3, 13.1, and 29.1 nm. Among 1.5, 5.3, and 13.1 nm, the terrace surface roughness increases with increasing oxide thickness. The surface topography images of both 13.1 and 29.1 nm thick oxides, however, are almost the same. Figure 5 shows the rms value of the surface roughness as a function of oxide thickness. Initially, the trend of increasing surface roughness is similar to that of Fig. 3, but it becomes saturated at an oxide thickness of approximately 10 nm. The average rms value in the saturation region is approximately 0.12 nm. The rms distribution width is approximately 0.01 nm. The oxygen concentration in the oxidation ambient at 600°C is 100%. The oxidation rate in the dilution of the oxygen at 600°C is too low to evaluate the oxide thickness dependence of the roughness. We

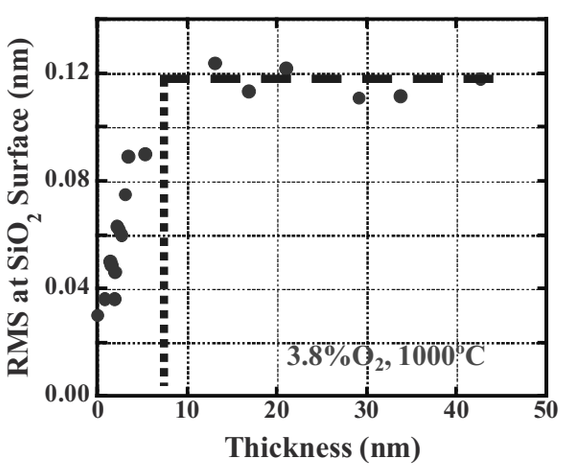

Figure 5. Thickness dependence of surface rms of SiO_2 films thermally grown at 1000°C in 3.8% diluted O_2 ambient.

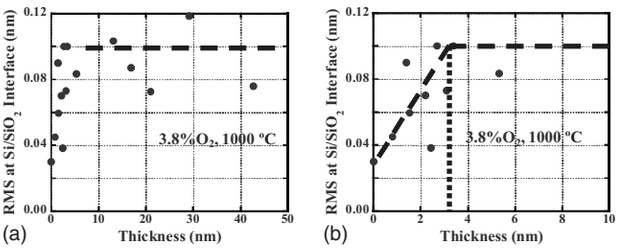

Figure 6. The rms value of the Si/SiO_2 interface as a function of oxide thickness. SiO_2 films are thermally grown at 1000°C in a 3.8% diluted O_2 ambient.

consider that the relaxation time of the oxidation stress is long enough not to change the surface and interface roughness,[11] even if the oxygen concentration is 100%.

However, in Fig. 6a and b, the rms value of the interface roughness of SiO_2 thermally grown at 1000°C in a diluted 3.8% O_2 ambient is plotted as a function of oxide thickness. The rms of the interface roughness fluctuates with a deviation width of approximately 0.03 nm around an average rms value of approximately 0.1 nm in the oxide thickness range of more than 10 nm, as shown in Fig. 6a. In the magnified oxide thickness region of less than 10 nm in Fig. 6b, the rms fluctuates, but also increases.

Furthermore, in Fig. 3 the increasing region of the interface roughness is too rapid to be observed within our experimental range of oxide thickness. However, in Fig. 6b, the rms of the interface roughness gradually increases with a significant fluctuation and saturates at an oxide thickness of approximately 3 nm. That is, the oxide thickness at which the interface roughness reached the saturation is higher at 1000°C than that at 600°C. The interface roughness at 1000°C gradually increases while fluctuating. It is believed that this relates to the high relaxation rate of the oxidation stress at high temperature.[11]

Next, let us consider the growth mechanism of the SiO_2 surface roughness.

Figure 7 shows the oxide thickness as a function of oxidation time at 1000°C in diluted 3.8% O_2 ambient. As described in the Deal–Grove model, we did observe an initial rapid oxidation region.[21] The initial oxidation switched to linear growth at approximately 10 nm. Massoud et al. described two typical exponential functions to represent this oxidation behavior,[22] but the oxidation mechanism in this region remains unexplained for a long time. Recently, Kageshima et al. reported that the initial oxidation can be

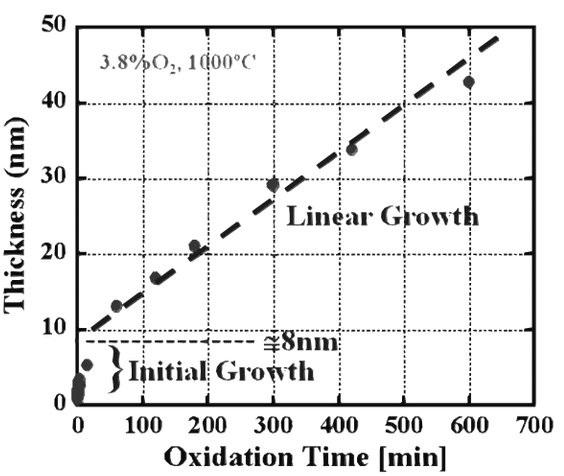

Figure 7. Oxide thickness as a function of oxidation time at 1000°C in 3.8% diluted O_2 ambient.

explained by considering reoxidation of the SiO species emitted from the Si/SiO_2 interface to the neighboring SiO_2 surface.[23] Their first-principles calculation suggested that the SiO emission is attributed to oxidation stress. Their calculation results are supported by Takakuwa et al., who reported that the emitted SiO species were detected during oxidation at a low oxygen pressure.[24]

Comparing Fig. 5 and 7 gives us consideration that roughness growth of the SiO_2 surface is closely related to the initial rapid oxidation. As the oxidation temperature becomes lower, the oxide thickness, at which the oxidation switches from the initial rapid phase to the slow linear-rate phase, is decreased.[21] As the oxidation rate is very low at 600°C, we evaluated only approximately 4 nm thick oxide. Its surface roughness was approximately 0.1 nm. That is, the surface roughness is saturated at approximately 2.5 nm. Therefore, we can say that the critical oxide thickness, at which the surface roughness becomes saturated, decreases with decreasing oxidation temperature.

Based on first-principles calculations, the origin of the SiO emission has been attributed to oxidation stress.[22] The oxidation stress results from volume expansion in the oxidation reaction of Si. As reported in Ref. 11 and 25, the oxidation stress changes, competitively depending on the increase with the oxide thickness and the relaxation. So, it initially increases during the high oxidation rate and changes to decrease when the oxide rate becomes low with an increase in the oxide thickness. That is, as the oxide thickness increases, the SiO emission increases, and the oxide surface roughness increases. The oxide growth in the initial oxidation region is enhanced by reoxidation of emitted SiO. At the same time, the SiO_2 surface roughness grows, as shown in Fig. 8. However in the linear-rate oxidation region, the oxide stress becomes low in order for the oxidation rate to decrease. So, the amount of the emitted SiO gradually decreases. The surface roughness monotonously increases, corresponding to the total amount of the emitted SiO reoxidized near the oxide surface. Even if the amount of the emitted SiO decreases by the surpassing relaxation effect, the surface roughness is kept without shrinking. However, the interface roughness generally proceeds in the manner of the layer-by-layer oxidation.[18,26] Accordingly, the interface roughness increases from the initial atomistic flatness and then is periodically repeated.

We consider another mechanism of the roughness saturation in the linear oxidation region. The emitted SiO is reoxidized within the SiO_2 films. Although volume expansion occurs at that time, the stress is relaxed or absorbed by reconfiguration of the Si–O–Si network in SiO_2 because of the low volume occupation of atoms in SiO_2 films.

Following the rms value of the SiO_2 surface and interface, particle analysis results of AFM data at the SiO_2 surfaces and Si/SiO_2 interfaces are shown in Fig. 9a and b. As the oxide thickness increases, the number of protuberances rapidly decreases, while their average diameter increases. When the oxide thickness grows beyond 10 nm, they becomes saturated. In the saturation region, the number of protuberances was nearly 3×10^{11} cm^{-2}, while their diameters at the surface and interface were 9 and 9.5 nm, respectively. The diameters of protuberances at the SiO_2 surface and interface increase in the oxide thickness range below 10 nm. However, their number decreased. These results support the model that the surface roughness growth is closely related to SiO emission in oxidizing at the Si/SiO_2 interface.

Two possibilities explain the surface roughness growth. One is the lateral migration of SiO at the SiO_2 surface following nucleation. The other is the nonuniform generation of SiO attributed to the island growth of the SiO_2 at the Si/SiO_2 interface. We have been unable to determine the origin of the lateral roughness growth. To clarify the roughness growth mechanisms, we need to investigate the correlation between the positions of the surface and interface protuberances.

Surface roughness in the ultrathin region.— There is another interesting aspect of the roughness growth at the SiO_2 surface. In the incubation period before roughening at 600°C in Fig. 3, the surface roughness remains unchanged, and the rms value does not increase. The appearance of the incubation period can be explained as follows. Because the oxide is ultrathin and the oxidation stress is very low, the total amount of emitted SiO is too low to cause an increase in roughness detectable by our AFM technique.

Dilution of the oxidation species at a high oxidation temperature can effectively suppress the oxidation stress because of the substantial increase in the stress relaxation time, as described in the

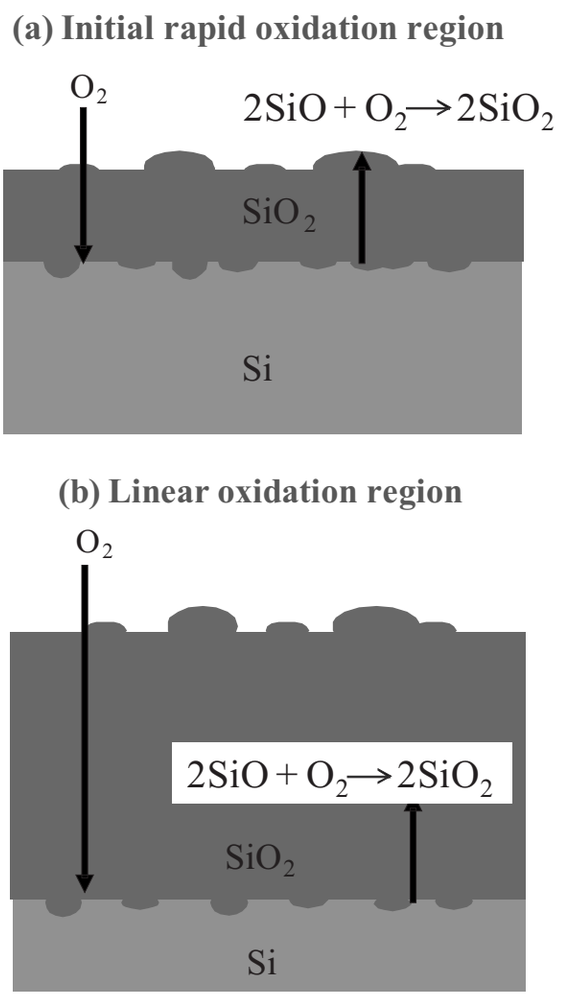

Figure 8. Surface roughness growth model.

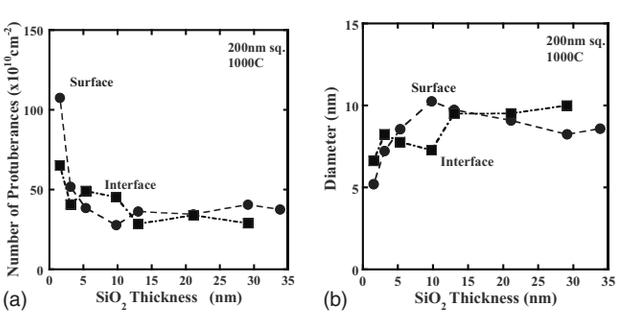

Figure 9. (a) Number of protuberances and (b) their diameters at the surfaces and interfaces as a function of the oxide thickness.

rounding-off oxidation model at the Si trench corner,[11] and this suppression of the oxidation stress can expand the incubation region.

Conclusion

In summary, an atomically flat Si surface enabled us to investigate the atomistic phenomena of thermal oxidation. As a result, some of the following phenomena are clarified. The SiO_2 surface roughness gradually increases before saturation. In the initial rapid oxidation region, the roughness growth is caused by reoxidation of SiO emitted from the Si/SiO_2 interface. However, in the linear-rate oxidation region, the roughness growth is saturated because the emitted SiO species are reoxidized within the SiO_2 film, and the oxidation stress generated is absorbed there. Although the amount of the emitted SiO decreases by the surpassing relaxation effect, the surface roughness is kept without shrinking. In the roughness growth region, the number of protuberances at the surface decreases with oxide thickness, while their diameter increases.

We observed an ultrathin oxide region in which the surface roughness remains unchanged. The presence of this region demonstrates that an ultrauniform thermally grown ultrathin SiO_2 film can be grown on an atomically flat Si surface. Such an ultrauniform SiO_2 would be useful to realize metal-oxide-semiconductor devices with ultrauniform electrical characteristics and could suppress the two-dimensional distributed component of the degradation under an applied electrical stress, leading to highly reliable thin gate dielectric films.

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References

1. K. Yamabe, K. Taniguchi, and Y. Matsushita, in *Proceedings of the Symposium on Defects in Silicon*, W. M. Bullis and L. C. Kimerling, PV83-9, p. 629, The Electrochemical Society Proceedings Series, Pennington, NJ (1983).
2. J. Ryuta, E. Morita, T. Tanaka, and Y. Shimanuki, *Jpn. J. Appl. Phys., Part 2*, **29**, L1947 (1990).
3. K. Yamabe and K. Taniguchi, *IEEE Trans. Electron Devices*, **ED-32**, 423 (1985); K. Yamabe and K. Taniguchi, *IEEE J. Solid-State Circuits*, **SC-20**, 343 (1985).
4. R. Hasunuma, J. Okamoto, N. Tokuda, and K. Yamabe, *Jpn. J. Appl. Phys., Part 1*, **43**, 7861 (2004).
5. Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, *J. Appl. Phys.*, **60**, 2024 (1986).
6. K. Yamabe, K. Taniguchi, and Y. Matsushita, in *Proceedings of the International Reliability Physics Symposium*, The IEEE Electron Device Soc. and The IEEE Reliability Soc., East 47th St., NY, p. 184 (1983).
7. K. Yamabe, K. Liao, H. Minemura, and M. Murata, *J. Electrochem. Soc.*, **148**, F9 (2001).
8. S. Okamoto, Y. Tokukawa, R. Hasunuma, M. Ogino, H. Kuribayashi, Y. Sugahara, and K. Yamabe, *J. Phys.: Conf. Ser.*, **106**, 012017 (2008).
9. R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, *Tech. Dig. - Int. Electron Devices Meet.*, **1995**, 863.
10. I.-C. Chen, S. E. Holland, and C. Hu, *IEEE J. Solid-State Circuits*, **SC-20**, 333 (1985).
11. K. Yamabe and K. Imai, *IEEE Trans. Electron Devices*, **ED-34**, 1681 (1987).
12. K. Imai and K. Yamabe, *J. Appl. Phys.*, **83**, 3849 (1998).
13. M. Miyashita, T. Tsuga, K. Makihara, and T. Ohmi, *J. Electrochem. Soc.*, **139**, 2133 (1992).
14. P. O. Hahn and M. Henzler, *J. Appl. Phys.*, **52**, 4122 (1981).
15. H. Watanabe, K. Kato, T. Uda, K. Fujita, M. Ichikawa, and T. Kawamura, *Phys. Rev. Lett.*, **80**, 345 (1998).
16. N. Tokuda, M. Murata, D. Hojo, and K. Yamabe, *Jpn. J. Appl. Phys., Part 1*, **40**, 4763 (2001).
17. D. Hojo, H. Oeda, N. Tokuda, and K. Yamabe, *Jpn. J. Appl. Phys., Part 1*, **42**, 1903 (2003).
18. D. Hojo, N. Tokuda, and K. Yamabe, *Thin Solid Films*, **515**, 7892 (2007).
19. H. Fukidome and M. Matsumura, *Jpn. J. Appl. Phys., Part 2*, **38**, L1085 (1999).
20. J. Flidr, Y.-C. Huang, T. A. Newton, and M. A. Hines, *J. Chem. Phys.*, **108**, 5542 (1998).
21. B. E. Deal and A. S. Grove, *J. Appl. Phys.*, **36**, 3770 (1965).
22. H. Z. Massoud, J. Plummer, and E. A. Irene, *J. Electrochem. Soc.*, **132**, 1745 (1985).
23. H. Kageshima, K. Shiraishi, and M. Uematsu, *Jpn. J. Appl. Phys., Part 2*, **38**, L971 (1999).
24. Y. Takakuwa, F. Ishida, and T. Kawawa, *Appl. Surf. Sci.*, **216**, 133 (2003).
25. E. Kobeda and E. A. Irene, *J. Vac. Sci. Technol. B*, **7**, 163 (1989).
26. T. Yasuda, N. Kumagai, M. Nishizawa, S. Yamasaki, H. Oheda, and K. Yamabe, *Phys. Rev. B*, **67**, 195338 (2003).