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Effects of annealing temperature on ultra-low dielectric constant SiO_2 thin films derived from sol–gel spin-on-coating

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Abstract

The results of ultra-low dielectric constant (k) SiO_2 films, derived from sol–gel spin-on-coating process using a combination of tetraethylorthosilicate (TEOS) and methyltriethoxysilane (MTES) (mole ratio of TEOS:MTES = 4:1), have been reported. The effects of post deposition annealing temperature (300–500 °C for 30 min in argon ambience) on the physical, chemical, and electrical properties of the oxide have been systematically investigated. Filmetric system, Fourier transform-infrared spectroscope, X-ray diffraction system, atomic force microscope, and field-emission scanning electron microscope with energy dispersive X-ray have been employed for physical and chemical analyses. Electrical property of the oxide, in terms of leakage current through the oxide, has also been investigated. The oxide, annealed at 500 °C, produced the lowest dielectric constant value ($k = 2.3$) and the lowest leakage current with no obvious oxide breakdown. The explanation of this observation has been discussed.

Keywords: Ultra-low dielectric constant thin film; Sol–gel; Porosity; Leakage current

1. Introduction

The growth of integrated circuit technology is primarily based on the ability of minimum feature size in the circuits to continue shrink down to deep submicron region. Smaller devices give higher packing density as well as higher operating speeds. However, with a higher device speed, there is an almost inevitable need to reduce RC delay in multilevel interconnections, where R and C are resistance and capacitance, respectively. This RC delay can either be reduced by lowering R value of metal interconnect, where aluminum is replaced by copper, and/or C value of interlayer dielectric (ILD), where a conventional oxide is replaced by a lower k material [1,2].

A variety of low k materials have been reported, such as non-fluorinated polymers, organic polymer, and silica (SiO_2) [2,3]. Among these materials, low k SiO_2 has demonstrated a more structural and thermal stable film than others [2]. Many techniques have been used to produce SiO_2-based low k materials. Sol–gel spin-on-coating appeared to be a more extendible method, as it is able to fill various aspect ratio of interconnects and produce porous structures that can further lower the k value (1.3–2.5) [2–5]. Although a lower k or ultra-low value of sol–gel derived SiO_2 films can be produced from inorganic Si source, such as tetraethylorthosilicate (TEOS), a few issues need to be addressed. One of the issues is the absorption of moisture on SiO_2 surface due to the presence of hydrophilic (Si–OH or Si–OCH_3) groups. This may cause the films to crack and properties to deteriorate with time. In order to solve this problem, organic solution has been added into the TEOS precursor [5,6]. In this paper, we are reporting the physical, chemical, and electrical results of sol–gel derived SiO_2 thin films from a combination of a higher TEOS:methyltriethoxysilane (MTES) ratio (4:1). The effect of annealing temperature (300–500 °C) on the properties of the films has also been systematically investigated.

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2. Experiment

Two types of sols have been prepared in order to produce a silica sol. Sol A consisted of a mixture of TEOS (Fluka), ethanol (J.T. Baker) and deionized (DI) water, and an appropriate amount of HCl (J.T. Baker) as a catalyst. Sol B contained a mixture of MTES (Fluka) as an organic precursor, ethanol, DI water, and NH_4OH (J.T. Baker) as a base catalyst. Both sols, with a mole ratio of sol A:sol B = 4:1, were mixed together and allowed to hydrolyze for 24 h. After that, the solution was applied on a pre-cleaned Si(1 0 0) substrate placed on a spin coater. The sol–gel spinning process was conducted at a speed of 3000 rpm for 30 s. Subsequently, the as-deposited film was soaked into a mixture of hexamethyldisilazane (HMDS) (Merck) and toluene (BDH) solution, so that surface modification was initiated. After this process, the film was then heat-treated independently at 300, 400 and 500 °C in argon-flow ambience for 30 min. After the heat treatment, the samples were sent for physical characterization. For electrical characterization, a layer of aluminum was evaporated onto the film and then patterned into area (A) of $9.98 \times 10^{-4}\,cm^2$. The subsequent process of fabricating it into metal-oxide-semiconductor (MOS) test structure has been described elsewhere [7].

The oxide thickness (t_{ox}) and refractive index (n) of the films were examined by a Filmetrics system. From the n value, density of the oxide, ρ, can be determined using the following relationship [8]:

$$\rho = \frac{n-1}{0.202}. \quad (1)$$

By knowing ρ value, porosity (Π) and dielectric constant (k) of the oxide can be deduced from the following equations [6]:

$$\Pi = 1 - \frac{\rho}{\rho_s} \quad (2)$$

and

$$k = 1 + 6.33(n-1), \quad (3)$$

where ρ_s is the density of a thermally grown conventional SiO_2 film ($2.27\,g/cm^3$). Chemical structure of the oxide was characterized at room temperature using a Fourier transform infrared spectrometer (FT-IR) (Perkin-Elmer). X-ray diffractometer (XRD) (PANalytical X'pert Pro MRD 3040) was used to investigate structure, phase, preferred crystal orientation, and crystallite size of the oxide. Energy dispersive X-ray analyzer (EDX) (JSM-6460LV) together with field emission scanning electron microscope (FESEM) was employed to study the morphology and chemical element of the oxide. Surface roughness of the oxide was characterized by an atomic force microscope (AFM) (Nano Navi SII). The electrical behavior of the oxides, in terms of leakage current through the oxide, has been evaluated using current–voltage (I–V) measurement (KEITHLEY 238 High Current Source Measurement Unit). The obtained I–V measurement was then transformed into current density (J)–electric field (E) plot. The J value was calculated by $J = I/A$, and E is approximated by $E \cong V/t_{ox}$.

3. Results and discussion

Fig. 1 shows the results of t_{ox} and n as a function of annealing temperature. The t_{ox} is in the range of 110–160 nm for all samples. The effect of annealing temperature has great influence on n value of the oxide. It can be seen that n value decreased with an increase in annealing temperature [9]. Fig. 2 presents the calculated percentage of porosity (Π%) and k values of the oxide as a function of the annealing temperature. When annealing temperature increases from 300 to 500 °C, Π% value increases from 19.07% to 54.19%, while k value decreases from 4.5 to 2.3. This observation may be attributed to the increase of open void appearances in the oxide, which contributed to the lowering of k value as the annealing temperature is increased.

Fig. 3 shows the transmittance mode of FT-IR spectra of the oxides annealed at different temperatures. The strongest

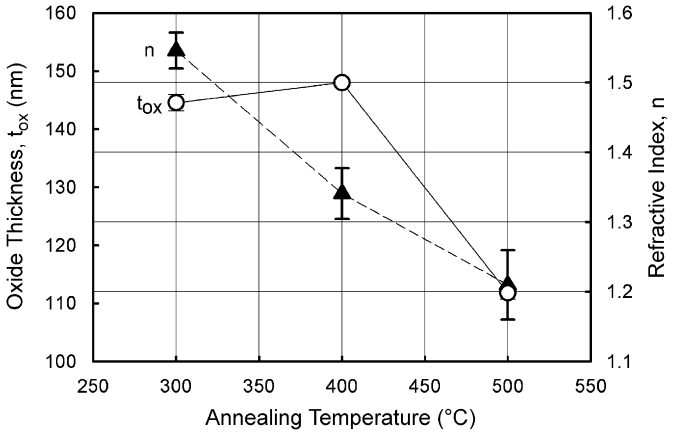

Fig. 1. The oxide thickness and refractive index as a function of annealing temperature.

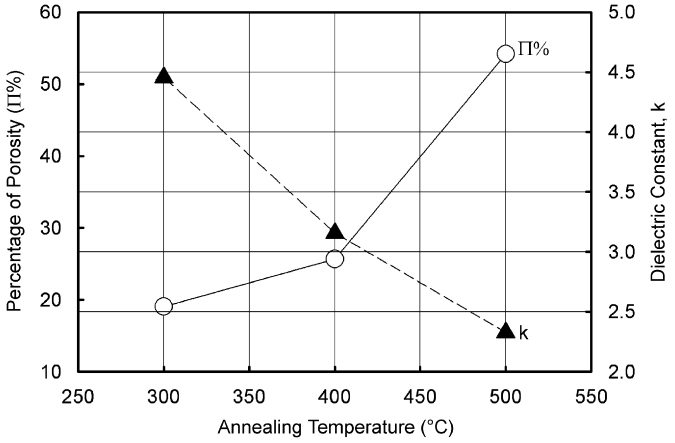

Fig. 2. The calculated percentage of porosity and dielectric constant of SiO_2 films annealed at different temperatures.

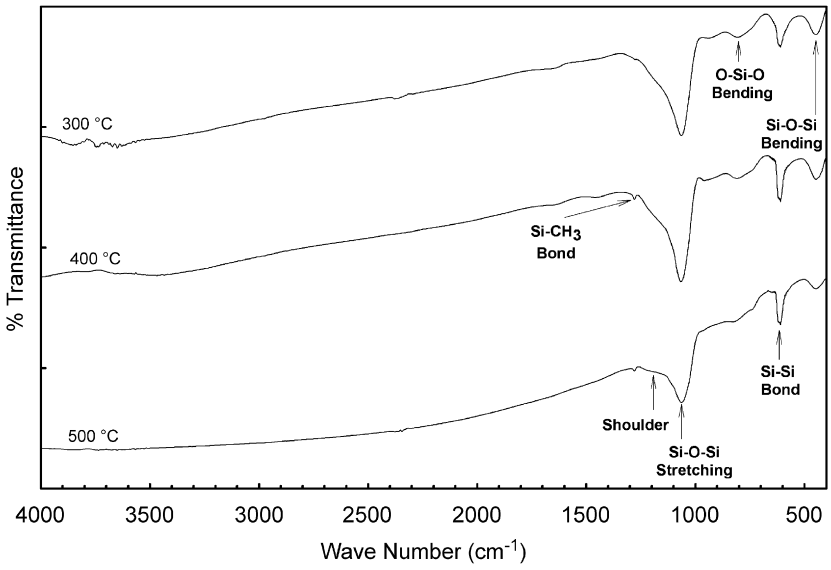

Fig. 3. Transmittance mode FTIR spectra of the investigated oxides annealed at different temperatures.

peak located at around 1060 cm^{-1} is attributed to stretching of Si–O–Si bond. A shoulder of this peak is extended to wave numbers of approximately 1100–1200 cm^{-1} depending on the annealing temperature. This shoulder refers to a longitudinal optical (LO) vibration of Si–O–Si linkage. The appearance of this LO shoulder is due to optical scattering effect of porous samples [6]. This is an indirect method to deduce the porosity appearances in a sample, and it will be elaborated further in the subsequent paragraph. There are other two peaks revealed at around 800 and 460 cm^{-1}. These are contributed by bending of O–Si–O and Si–O–Si bonds. The bending of O–Si–O bond is caused by hydrolysis process occurring in the oxide. Meanwhile, the previously mentioned stretching of Si–O–Si bonds is attributed to the condensation process of the oxide, which involves hydroxyl groups, and subsequently initiated the formation of inorganic polymer of Si–O–Si bond. These are the transmittance peaks related to SiO_2. Besides, peaks associated with Si substrate and incomplete or contamination of organic substances have been detected at location around 610 cm^{-1} (Si–Si bond) and $>2300\,cm^{-1}$ (2340, 3400, and 3600 cm^{-1} are related to stretching of $Si–CH_3$, Si–H, and O–H, respectively). As the annealing temperature increases, the later peak is reduced until it could not be detected [10].

The shift of transmittance peak located around 1060 cm^{-1} as a function of annealing temperature is shown in Fig. 4. The shift of the position is also accompanied by the change of full-width at half-maximum (FWHM) of the peak. When the annealing temperature increases from 300 to 400 °C, the peak of Si–O–Si stretching bond is shifted to a higher value, which is closer to its theoretical value of 1080 cm^{-1}. However, there is a reduction in the FWHM of the peak. Hence, we may conclude that a densification of the film is obtained as the stretching of Si–O–Si bond is

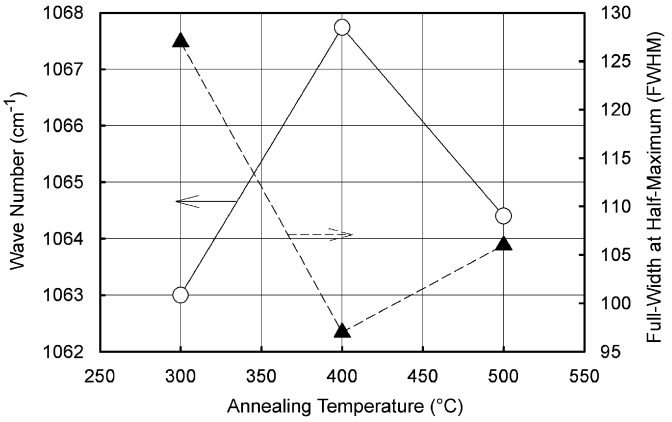

Fig. 4. Wave number and full-width at half-maximum (FWHM) of Si–O–Si stretching bond as a function of annealing temperature.

less in oxide annealed at 400 °C if compared with oxide annealed at 300 °C [11]. However, when the annealing temperature is further increased to 500 °C, the position of the peak is shifted to a lower wave number, which is further away from 1080 cm^{-1}. At the same time, the FWHM value of the particular peak is increased. This indicates that the stretching of Si–O–Si bond is increased if compared with the oxide annealed at 400 °C. During this bond stretching process, it may generate vacancy of oxygen atom. This vacancy may be treated as a donor like trap (Si^{+}). The deficiency of oxygen has been proven by EDX results (Fig. 5) obtained from FESEM investigation under a full area of 10,000 × magnification (the micrographs are not shown). It can be observed that the weight percentage and atomic percentage of oxygen is decreased when the oxide is annealed at 500 °C.

The XRD patterns for samples annealed at different temperatures are shown in Fig. 6. The result is matched

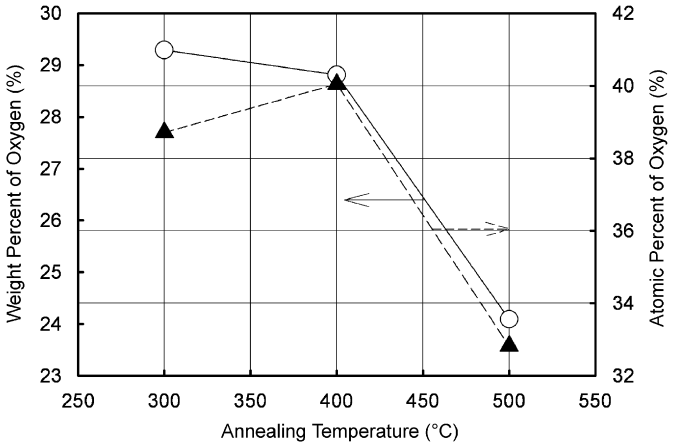

Fig. 5. Weight percentage and atomic percentage of oxygen element detected in oxides annealed at different temperatures. The percentages were deduced from an area of 10,000 × magnification.

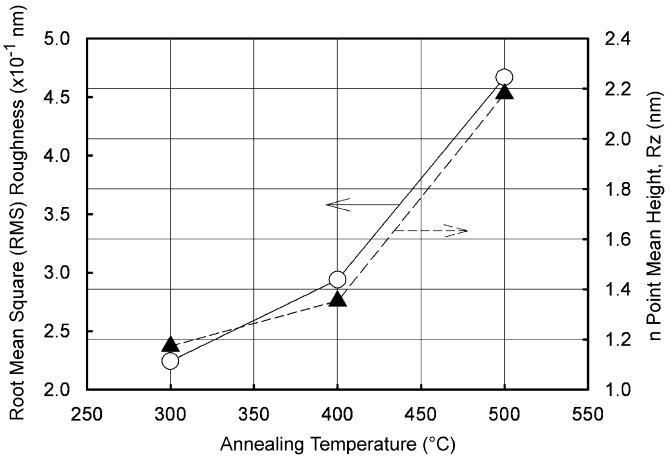

Fig. 7. A comparison between root-mean-square (RMS) roughness and n-point mean height (R_z) as a function of annealing temperature.

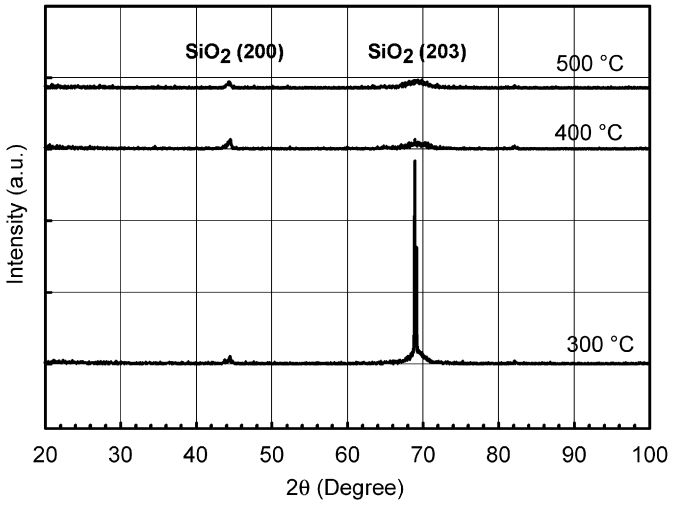

Fig. 6. Pattern of XRD as a function of annealing temperature.

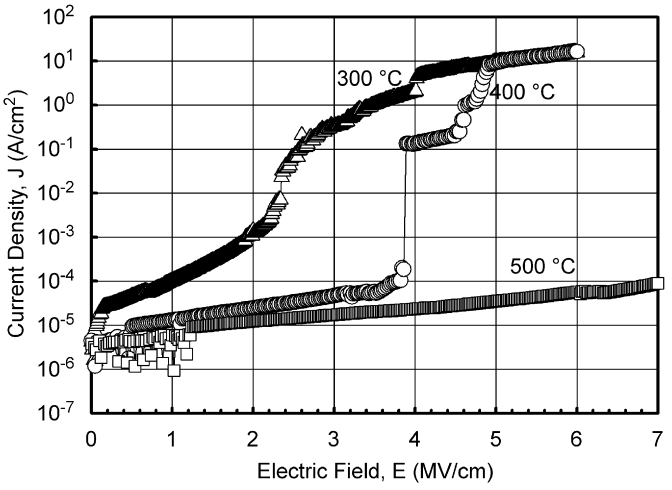

Fig. 8. Current density–electric field characteristics of oxides annealed at different temperatures.

with phase and structure of SiO_2 using a JCPDS file no. 5-0490. There are two obvious peaks at 44.35° and 68.99°, associated with SiO_2 (2 0 0) and (2 0 3), respectively, in all samples. As the annealing temperature increases, the later orientation of SiO_2 is reduced.

Topography of oxide surface has been altered as the annealing temperature increases. Quantitatively, root-mean-square (RMS) roughness and *n*-point mean height (R_z) of the investigated surfaces have been extracted and their results are presented in Fig. 7. The value of RMS roughness and R_z are increased with the increase of annealing temperature. The surface of the film becomes rougher as the annealing temperature increases and this may be attributed to grain growth process [12].

Fig. 8 presents the *J–E* plot of oxides annealed at different temperatures. When annealing temperature increases, at a specific *E*, the *J* value is reduced. This indicates that leakage current has been reduced. The oxide breakdown field of the investigated oxide has been extracted from the *J–E* plots. This field refers to an instantaneous increase of *J* value at a particular electric field. It is obvious that oxide annealed at 400 and 300 °C have demonstrated a sharp increase of *J* at approximately 3.8 and 2.3 MV/cm, while there is no significant increase in oxide annealed at 500 °C.

The increment of breakdown field and reduction of leakage current at higher annealing temperature may be attributed to the increase of surface roughness as what has been revealed in Fig. 7. As the surface becomes rougher, the probability of a region with thicker oxide is high. The thicker oxide may restrict the movement of charge passing through the oxide. Therefore, a lower leakage current is detected. Besides surface roughness, deficiency of oxygen in oxide annealed at 500 °C may act as a donor-like trap for the injected electron. As the electron is injected from Si

into the oxide, majority of the electron is captured and neutralized in the trap. This is not happening in samples annealed at 300 and 400 °C. Therefore, the leakage current is much lower than those oxides. From the electrical results, it could be concluded that the oxide structure is strong as it is becoming more difficult to electrically break the oxide, even though the percentage of porosity in the oxide is increasing with the increase of annealing temperature (Fig. 2).

4. Conclusion

Ultra-low dielectric constant ($k = 2.3$) SiO_2 thin films were fabricated using sol–gel process with a combination of TEOS and MTES. The post-deposition annealing temperature has a great effect on the physical, chemical, and electrical properties of the films. With increasing annealing temperature, percentage of porosity has been increased while the dielectric constant and refractive index of the oxide have been decreased. The high value of oxide surface roughness and appearance of donor-like trap in the oxide was mainly caused because of the low leakage current detected in oxide annealed at higher temperature.

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