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Chemical Vapor Deposition of Tungsten (CVD W) as Submicron Interconnection and Via Stud

Pei-Ing Lee, John Cronin, and Carter Kaanta

IBM General Technology Division, Essex Junction, Vermont 05452

ABSTRACT

Blanket-deposited CVD W has been developed and implemented in a 4-Mbit DRAM and equivalent submicron VLSI technologies. CVD W was applied as contact stud, interconnect, and interlevel via stud. The technologies have been proven reliable under several reliability stress conditions. Major technical problems involved in CVD W processing, such as adhesion, contact resistance, etchability, and hole fill will be discussed. A novel technique that uses TiN as a contact and adhesion layer will be presented. This technique has lead to the resolution of the above technical problems and significantly improved the manufacturability of blanket CVD W processes.

As circuit density increases in VLSI technology, the limitations of conventional metallization techniques become more apparent. Polysilicon has been widely used as gate electrode material, particularly with the assist from low pressure chemical vapor deposition (LPCVD) refractory metal and metal silicide, which is known as polycide (1). The use of polysilicon as back end of line (BEOL) interconnect is limited by its high resistance capacitance (RC) delay. Sputtered or evaporated aluminum-based metallurgies do not present RC delay difficulties, but they have their own concerns. The major concern comes from the poor step coverage and conformality in the conventional sputtered or evaporated aluminum. This concern has greatly limited the capability to wire high-density VLSI that typically requires vertical wiring structure and multiple levels of interconnect. While LPCVD aluminum process has received much attention (2), other techniques such as laser reflow planarization (3) and high heat and high bias sputtering aluminum (4) have been investigated to improve the hole fill capability of aluminum metallurgy. However, these processes are yet to be proven manufacturable. Aluminum metallurgies also suffered from low electromigration resistance (5), hillock formation (6), and creep failure (7). These failures have resulted from the relatively poor electrical, thermal, and mechanical stability of aluminum.

Because of the above limitations and concerns of the conventional metallurgies, a lot of attention was drawn into CVD refractory metal and metal silicide, and particularly CVD W. CVD W has offered several attractive key features. CVD W can be deposited by reducing tungsten hexafluoride, tungsten hexachloride, and tungsten carbonyl in the gas phase. The reduction of tungsten hexafluoride offers convenient handling advantages. Excellent step coverage and hole fill can be obtained by carefully choosing a process condition. The chemistry of these reactions can be found in several excellent studies (8). Tungsten has been proven to be extremely reliable against electromigration in a previous publication (9). In addition, the thermal expansion coefficient of tungsten is much more compatible to silicon than that of aluminum. The incompatibility of thermal expansion coefficient between aluminum and silicon has resulted in problems such as film delayering and hillock formation (6). Furthermore, the mechanical stress induced creep formation has not been observed in tungsten metallurgy as in aluminum metallurgy.

The CVD W can be deposited either selectively or nonselectively. During the past few years, the selective CVD W has faced problems such as selectivity, contact resistance, encroachment, growth rate, and device leakage (10). Recently, promising progress has been made in each of these areas (11). The blanket CVD W process has also provided its own problems. The major problems include adhesion, contact resistance, etchability, and device impact. Each of these problems has raised questions of the manufactur-

ability of blanket CVD W processes. In the sections to follow, we will first briefly discuss our experimental condition and some historical background of CVD W, and then present our approach in solving the CVD W problems. Finally, we will conclude this paper with the reliability results from integrating CVD W into a submicron VLSI technology.

Experimental

The CVD W was processed in a commercial coldwall batch reactor. The wall of the reactor was maintained around 15°C. Most of the deposition was made at wafer chuck temperature of 450° +/− 8°C. Both silane and hydrogen were used to reduce tungsten hexafluoride. The wafer temperature, reactor pressure, reactant ratio has varied for several experiments. The result will be discussed elsewhere. Here in this paper, we will focus our discussion on the above-mentioned problems that have been the major obstacles of integrating CVD W process into VLSI technology.

Two adhesion test techniques were used. The first test technique, the adhesive tape test, was done by first scribing the tungsten film, and an adhesive tape was applied and pulled vertically at roughly 3 cm/s speed. This technique qualitatively determines film adherence. The second test technique, the Instron pull test, was used to obtain semiquantitative adhesion results. A stud with surface area of 0.02759 in.^{2} was glued to the tungsten film by epoxy and cured. The stud was then pulled by the Instron tester. The adhesion was calculated by dividing the load at yield point by surface area. These two techniques provided a comparison for the relative adhesion of CVD W under different experimental conditions.

Historical Background

The adhesion of CVD W to most insulators, such as silicon oxide and nitride, PSG, and BPSG, is extremely poor. Special surface preparation techniques (12) or using an adhesive layer (13) have been proposed to improve the adhesion of CVD W. The method of using an adhesive layer seems to provide more consistent results. The most convenient adhesive layer that was suggested by the equipment vendors is tungsten silicide (WSi_x), which can be deposited *in situ* in a CVD W tool. The tungsten silicide can also be applied as a cap layer on the top of tungsten film to prevent tungsten from oxidation at deposition temperature. In our study, we have found that the adhesion between tungsten and adhesive layer tungsten silicide relies on a vendor-suggested RIE surface treatment process. This RIE surface treatment roughened the silicide surface, as shown in Fig. 1a, to improve the adhesion. Unfortunately, this technique has been shown to cause damage to the contact region. Figure 1b shows the additional problem of using tungsten silicide as an adhesive layer. Severe undercut etching was observed when the WSi_x/W/WSi_x stack was patterned by RIE etching in SiF_4/O_2 etch chemistry. It is known that the isotropic etching in RIE can be reduced by sidewall passivation techniques (14). Several other fluorinated and chlorinated chemistries and sidewall passivation processes were evaluated to reduce the isotropic etching in the silicide layer. Little success was made in producing a consistently manufacturable anisotropic etching process.

In addition to the adhesion and etchability problems, CVD W using tungsten silicide as an adhesive layer has also resulted in contact resistance of as high as $5 \times 10^{-6}\ \Omega\ cm^2$.

Etchability

It is inevitable to search for an adhesive layer other than WSi_x due to etchability and contact resistance problems. Many adhesive layers were suggested by Bryant (13). However, the dependency of the etchability and contact resistance on adhesive layers has not yet been discussed. It was found that sputtered tungsten, titanium/tungsten alloy, and molybenum as an adhesive layer for CVD W, have all produced some degree of undercut etching on the adhesive layer. SiF_4, Cl_2, SF_6, BCl_3, and CF_4 etch chemistry with an additive of either O_2, Ar, $CHCl_3$, or HCl was used

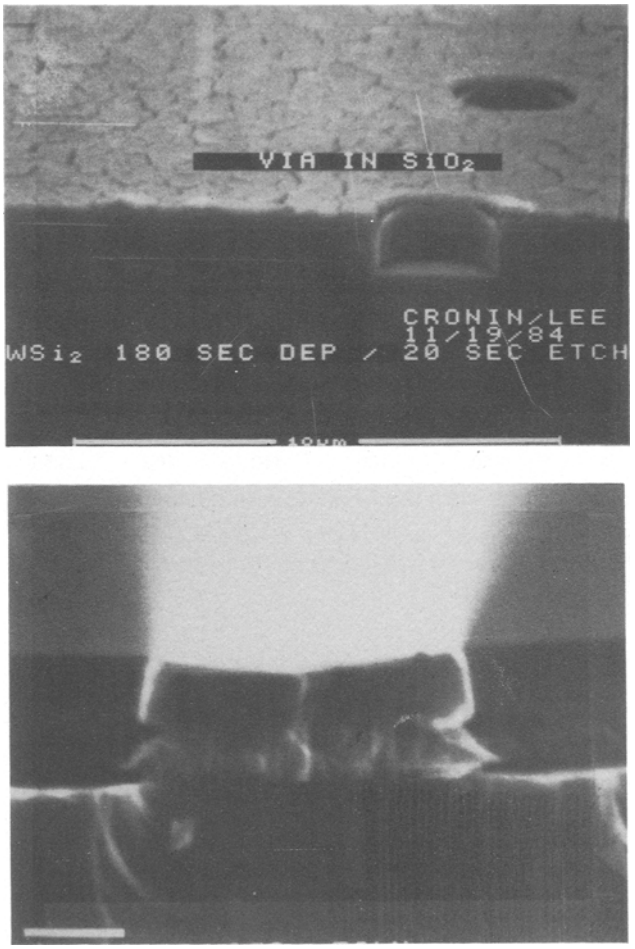

Fig. 1. (a, top) The tungsten silicide adhesive layer after *in situ* RIE surface treatment in the deposition tool. Note that the surface was severely damaged. (b, bottom) Isotropic etching of CVD tungsten using tungsten silicide as adhesive layer. Note the severe undercut etching in the tungsten silicide layer.

for this investigation (15). Sputter chromium and titanium as adhesive layers have caused little or no undercut etching problem in either fluorinated or chlorinated etch chemistry. Best results were obtained by using sputtered titanium as an adhesive layer and Cl_2/O_2 etch chemistry (15).

Holland *et al.* (15) have also reported that the Cl_2/O_2 etch chemistry has resulted in a severe resist erosion problem. Therefore, a multilayer mask is required when using Cl_2/O_2 etch chemistry. Recently, Kaanta *et al.* (9) have reported that using silicon nitride or oxide as an inorganic mask eliminated the resist erosion concerns.

Adhesion

Although sputtered titanium as an adhesive layer produces the best etching result, the adhesion of CVD W using titanium as an adhesive layer is very poor. In addition, the CVD W using sputtered titanium as an adhesive layer has resulted in extremely poor contact resistance and will be discussed in the following section. Reasonable adhesion was observed between sputtered tungsten and sputtered titanium. The poor adhesion between CVD W and sputter titanium adhesive layer was suspected to be caused by the unique situation of CVD W processes. Mass spectroscopy was used to study the background gas in the CVD W deposition tool after a deposition run was made. A high concentration of fluorinated species can be detected even without introduction of reactive gases. It is suspected that the fluorinated species play a major role in the adhesion and contact resistance of CVD W.

A dummy experiment was carried out to test the effect of deposition ambient by loading wafers with Ti adhesive layer into the deposition tool at several chuck tempera-

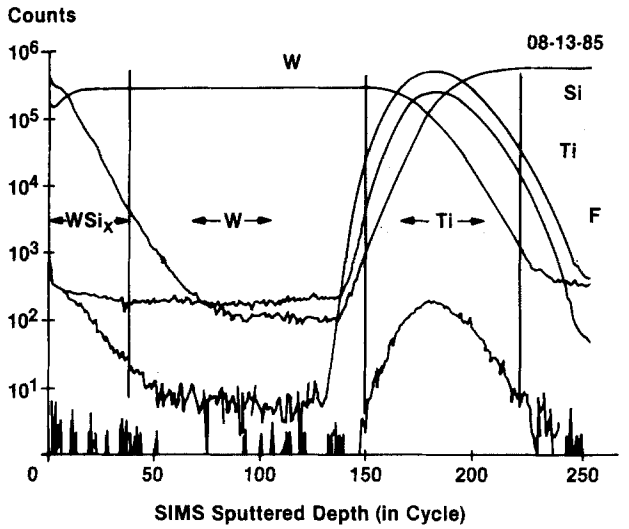

Fig. 2. SIMS depth profile of CVD W using sputter titanium as adhesive layer. Note the high fluorine concentration in the titanium adhesive layer.

Table Ia. The adhesion of CVD W using titanium as adhesive layers

Substrate	Preclean	Ti nitridation	Scotch tape pull test	Instron pull test (lb/in.^{2})
$TiSi_x$	No	No	Peeled	580
	BHF	No	Peeled	650
	C/P	No	Peeled	510
	BDE	No	Peeled	590
TOX	No	No	Peeled	540
BPSG	No	No	Peeled	600

Table Ib. The adhesion of CVD W using titanium nitride as adhesive layers

Substrate	Preclean	Ti nitridation	Scotch tape pull test	Instron pull test (lb/in.^{2})
$TiSi_x$	No	Yes	Adhered	>950
	BHF	Yes	Adhered	>950
	C/P	Yes	Adhered	>950
	BDE	Yes	Adhered	>950
TOX	No	Yes	Adhered	>950
BPSG	No	Yes	Adhered	>950

tures. The wafers were immediately unloaded without any deposition, *i.e.*, no gas was introduced. Significant increase in the sheet resistance of titanium was found after unloading these test wafers from the deposition tool. The sheet resistance increased as the tool chuck temperature increased.

The result from the above dummy experiment clearly shows the impact of deposition ambient on sputtered titanium, even before CVD W was deposited. However, it did not confirm the impact had resulted from fluorinated species in the deposition tool. Secondary ion mass spectroscopy (SIMS) depth profile analysis on a CVD W film using sputtered titanium as an adhesive layer is shown in Fig. 2. Elements of tungsten, silicon, titanium, fluorine, and oxygen were detected. Small amounts of oxygen were detected on the interfaces between each layer, but little oxygen was detected in the tungsten bulk layer. This indicates that the surface tungsten silicide layer had effectively prevented tungsten from being oxidized. Significantly high fluorine concentration was detected in the titanium adhesive layer. The penetration of fluorine can be deep into silicon substrates. F/Ti ratio of as high as 1 in the titanium layer has been observed. This fluorine was suspected of weakening the titanium and insulator interface by breaking the Ti-O-Si bonding and resulted in poor adhesion. It is also suspected that the formation of volatile titanium fluoride or subfluoride may also play a role in weakening the adhesion.

In order to reduce fluorine from diffusing into the titanium adhesive layer and devices, an effective diffusion barrier is required. TiN was found to be one of the most effective diffusion barriers in a CVD W deposition ambient. TiN was also found to provide an excellent anisotropic etching profile for the CVD W/TiN stack. TiN can be made by thermally nitridizing titanium in a nitrogen or forming gas ambient. TiN can also be made by reactive-sputtered titanium in a nitrogen/argon ambient or by sputtering from a TiN target. Thermally annealed TiN has provided more consistent results as far as adhesion and contact resistance are concerned. Figure 3 shows the fluorine counts in the adhesive layer using either titanium or thermally nitridized TiN as an adhesive layer. Drastic reduction on the fluorine count in the adhesive layer was observed when TiN was used as an adhesive layer. The fluorine counts decrease as the nitridation temperature is increased.

Table I shows the adhesion of CVD W using either sputtered titanium or nitridized TiN as an adhesive layer. Three substrates were used: titanium silicide (TiSix), thermal oxide (TOX), and borophosphoro silicon glass (BPSG). The substrates were precleaned either by 50:1 buffered HF (BHF), 50:50 chromic/phosphoric (C/P), or ammonium fluoride (BDE), or without preclean. After preclean, the substrate was deposited with sputter titanium within a 2h time window. Half of the wafers was then deposited with CVD W without nitridation. The other half was nitridized by thermal annealing before CVD W. Two

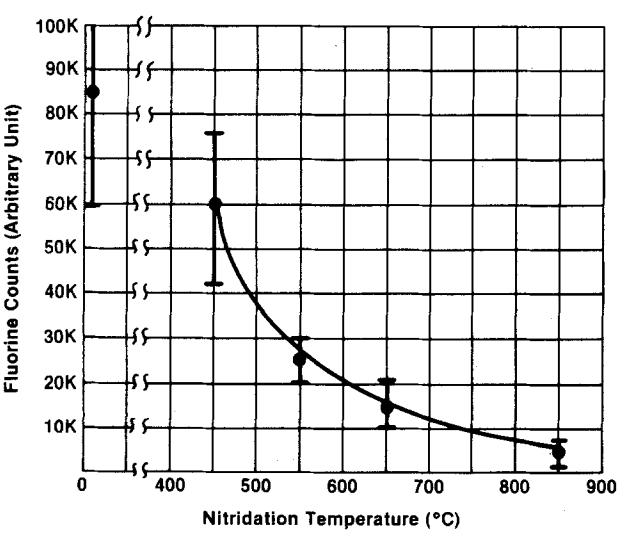

Fig. 3. The fluorine content in the titanium adhesive layer as a function of titanium nitridation temperature. The fluorine content decreases as the nitridation temperature is increased.

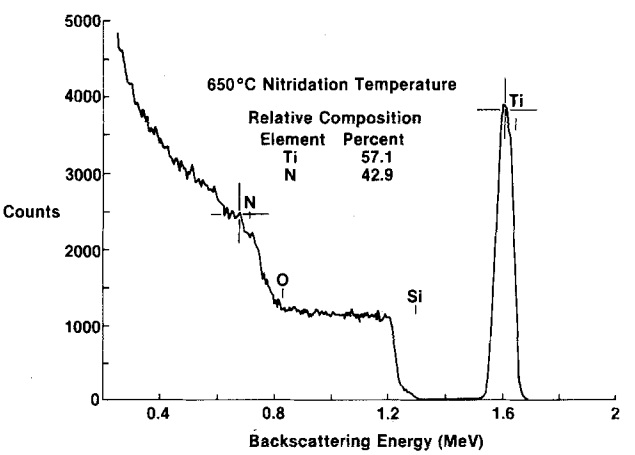

Fig. 4. Typical RBS of a nitridized titanium. The titanium was nitridized by thermally annealing pure titanium in a nitrogen ambient at 650°C.

Table II. A comparison of the contact resistance of CVD W using titanium as adhesive layers vs. using titanium nitride as adhesive layers

Contact substrate	Contact size	Nitridation temperature (°C)	Contact resistance (Ω)
N^+ diffusion	0.8	No anneal	>1,300
P^+ diffusion	0.8	No anneal	>1,300
Polysilicon	0.8	No anneal	>1,300
N^+/P^+/poly	0.8	450	0.5 to 9.0
N^+/P^+/poly	0.8	650	0.4 to 1.9

adhesion test techniques described in the previous section were used to test the adhesion of CVD W with adhesive layers. In the adhesion tape peel test, it was interesting to note that all the wafers without titanium nitridation had peeled, and all the wafers with nitridation had adhered. Prelean techniques showed slight effect on the adhesion result from Instron pull test. The effect of thermal nitridation makes the most noticeable difference. Very significant improvement in adhesion for the wafers with nitridation were also noticed. In the Instron pull test, most wafers with nitridation showed epoxy fail or substrate fail at yield point. We also noticed that the nitridation temperature between 450° and 850°C all provided improvements on adhesion. The difference in TiN as a function of nitridation temperature will be discussed in the following section.

Contact Resistance

TiN has been shown to reduce fluorine content and improve adhesion significantly. Table II shows a comparison of the contact resistance of CVD W using either Ti or TiN as an adhesive layer. N^+ and P^+ junction and polysilicon with a titanium silicide surface layer was contacted by CVD W. The CVD W was patterned by the RIE technique described in the previous section. The contact resistance was evaluated on a Kelvin four-point structure. The adhesive layer was found to be a dominating factor on the contact resistance. It was noticed that the CVD W using Ti as an adhesive layer had contact resistance as high as 1300Ω per contact, which is equivalent to 8.3×10^{-6} Ω cm^2. There are three orders of magnitude improvement in contact resistance for CVD W using TiN as adhesive layer. The contact resistance of as low as 2.6×10^{-9} Ω cm^2 has routinely been achieved. Both thermal nitridation at 450° and 650°C have shown significant improvement in contact resistance. Thermal nitridation at higher temperatures seems to provide tighter control on the range of contact resistance.

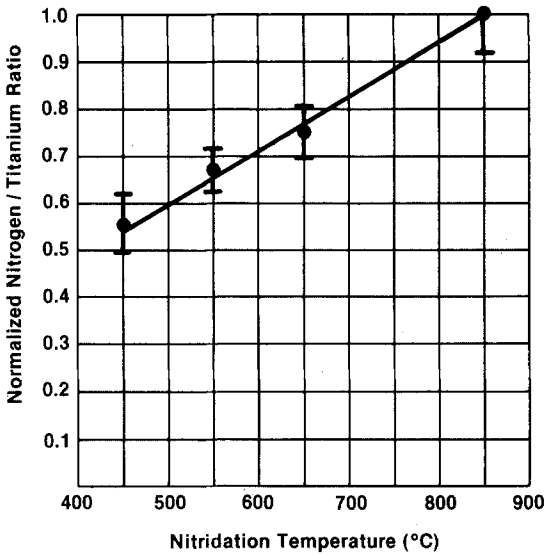

Fig. 5. Normalized nitrogen to titanium ratio (N/Ti) as a function of titanium nitridation temperature. The ratio was normalized to the data point at 850°C nitridation temperature. Note that the N/Ti ratio increases as the nitridation temperature is increased.

It is indicative in Fig. 3 and Table II that the higher nitridation temperatures favor lower fluorine penetration and better contact resistance. The TiN with several nitridation temperatures was analyzed with Rutherford backscattering spectroscopy (RBS). Figure 4 shows the typical RBS spectrum on a TiN with 650°C nitridation. Relative nitrogen-to-titanium ratios (N/Ti) were calculated by the atomic composition in the TiN layer. Figure 5 shows the N/Ti ratio as a function of nitridation temperature. The

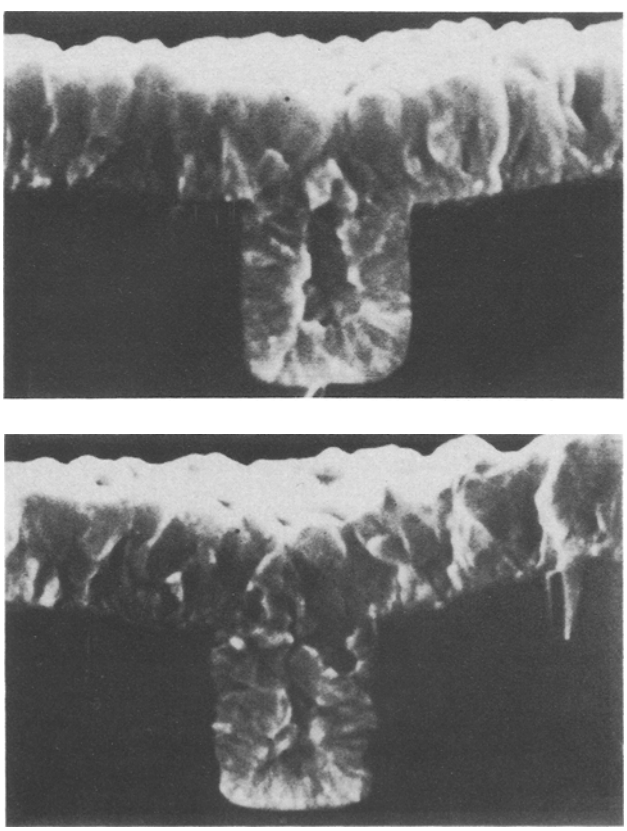

Fig. 6. (a, top left) The comparison of void formation in a submicron via using various deposition chemistry. Note the severe void formation in SiH_4 reduction reactions. (b, top right) No void formation in H_2 reduction reactions. (c, bottom) No void formation for two-step process, *i.e.*, SiH_4 reduction followed by H_2 reduction reactions.

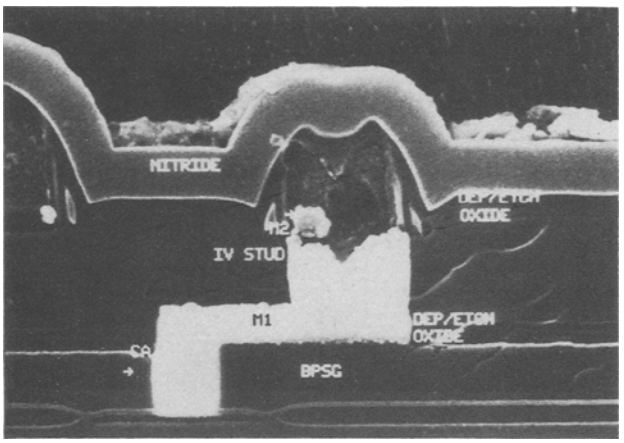

Fig. 7. Two-level submicron interconnection technology featuring CVD W and complete planarization. Note that CVD W provides excellent via fill for vertical contact and vias.

ratio was normalized to 850°C nitridation temperature. The N/Ti ratio increases as the nitridation temperature is increased. Further supplemental analysis by Auger electron spectroscopy (AES) and SIMS have indicated that the higher N/Ti may have resulted from the thicker TiN formed from the surface.

Several follow-on experiments were carried out to verify that titanium nitridation is essential for contact resistance improvement. At the first experiment, a titanium adhesive layer was thermally annealed in an inert argon ambient before CVD W deposition. At the second experiment, the CVD W using titanium as an adhesive layer was thermally annealed in an inert argon ambient after CVD W deposition. Neither of these two experiments showed improvement on contact resistance. It was also found that the reactive-sputtered TiN could also improve the adhesion and contact resistance. However, relatively scattered contact resistance results were obtained. It is suspected that the reactive-sputtered TiN may not be effective as a diffusion layer as the thermally nitridized TiN. This might have been the result of the narrow process window on producing the reactive-sputtered TiN in our sputtering equipment.

Via Fill

Step coverage of CVD W is known to be better than aluminum metallurgy. Typical step coverage of CVD W is greater than 80%. However, submicron via fill of CVD W can be challenging. The reasons can be explained by fundamental chemical reaction engineering theories (16). Void formation may result when a CVD W process is operated under mass-transfer control region. Complete via fill can be achieved when a CVD W is operated under kinetic control region. Reactor design, process parameter (pressure, temperature, gas ratio, flow rate), process reactant selection, and reaction kinetics are among the key factors that determine these operational regions. Detailed discussion of the above reaction engineering theory is beyond the scope of our paper. Further discussions can be found in several excellent reviews (16).

In order to achieve the reasonable via fill in our commercial reactor, the above process parameter was optimized. In addition to the process parameter optimization, we found that the selection of process chemistry played an important role in determining via fill capability. For silane and hydrogen mixture as reducing agents, the CVD W deposition rate is 27+/−3 Å/s at 450°C. Void size of 0.3 μm may result since this process is operated under mass transfer control. On the other hand, for pure hydrogen as a reducing agent, the CVD W deposition rate is 7+/−1 Å/s at 450°C, and excellent via fill can be obtained. SIMS analysis shows that there is no measurable difference between these two films. A two-step process using both silane and hydrogen reduction reactions was developed to achieve both reasonable throughput and via fill. Comparison via fill results using (a) SiH_4 reduction reactions, (b) H_2 reduction reactions, and (c) a two-step process is shown in Fig. 6.

Process Integration

Kaanta *et al.* (9) have described a multilevel submicron VLSI interconnect technology that features blanket CVD W. Figure 7 shows the double-level metal implementation of the interconnect technology that he described. The CVD W was applied as contact stud, MI interconnect, and interlevel via stud. Notice that CVD W provides excellent vertical wiring capability, which greatly improves the wiring density. This was made possible by the resolution of the above-mentioned technical problems, namely, the problems of adhesion, etchability, contact resistance, and via fill. In combination with the excellent insulator processing, the overall technology has been proven to be extremely reliable against electromigration stress, thermal/humidity stress, thermal cycle stress, and thermal voltage stress. The detail of this reliability result was discussed by Kaanta (9).

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