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Silicon Epilayers Grown by Chemical Vapor Deposition from High-Purity Silane

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Abstract—Structurally perfect, high-purity silicon epilayers up to 20 μm in thickness, with a carrier concentration $n = 10^{12}$ cm^{-3} are grown through thermal decomposition of silane. Experimental evidence is presented that the concentration of "electrically active" impurities in high-purity silane can be evaluated from the electrical parameters of Si epilayers grown from it.

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INTRODUCTION

In a number of device applications, high-purity epilayers of silicon, a basic semiconductor material, are needed. In particular, the fabrication of microwave diodes, photodetectors, quantum computers, Si–Ge superlattices, and nuclear detectors requires high-purity Si films with a carrier concentration below 10^{13} cm^{-3} and high structural perfection [1–7].

One attractive precursor for the growth of high-purity silicon films is silane. As the impurity content of silane decreases to below 0.01 ppma, this compound becomes increasingly difficult to analyze by conventional techniques, such as gas chromatography, IR spectroscopy, and atomic absorption spectroscopy, since even the most sensitive techniques have detection limits for impurities at a level of 0.01 to 0.1 ppma [8].

The purity of silane can be assessed with high sensitivity by measuring the concentration of electrically active impurities in silicon single crystals grown from it [9]. This approach, however, requires a large amount of silane. In connection with this, it is of interest to develop procedures for evaluating the purity of silane by determining electrical parameters (conductivity type and carrier concentration) of single-crystal silicon epilayers grown from it.

In this paper, we describe a process for the growth of structurally perfect, high-purity silicon epilayers through silane pyrolysis and compare their electrical properties with those of silicon single crystals.

EXPERIMENTAL

Silicon epilayers were grown via silane pyrolysis at a pressure of 10^5 Pa in a water-cooled horizontal metallic reactor fitted with a graphite heater (Fig. 1) [10]. As substrates, we used *n*- and *p*-type silicon wafers 30 mm in diameter, doped to various levels, which were mounted on the heater in a zone with a temperature difference of 5–10°C. During the epitaxial process, the substrate temperature was maintained at 1050°C, the flow rate of silane was about 10 ml/min, and the growth rate of the epilayers was about 0.3 μm. The epilayer thickness was varied from 5 to 20 μm.

Varied experimentation showed that the growth of high-purity silicon epilayers with a carrier concentration at a level of 10^{13} cm^{-3} involved serious problems due to contamination originating from the graphite heater. Before being mounted in the reactor, the heater was annealed at 1600°C in vacuum (residual pressure below 10^{-4} Pa) for 10 h. High-vacuum annealing, however, did not rule out background contamination, and the concentration of uncompensated charge carriers (holes) in the epilayers was as high as ~10^{16} cm^{-3}. To reduce the contaminating effect of the heater, it was coated with a silicon layer ~5–10 μm thick, which was deposited through decomposition of high-purity silane before epilayer growth and was then heat-treated. Next, the substrates were mounted on the heater, and the epitaxial process was run. With this procedure, the contamination from the heater was insignificant. The

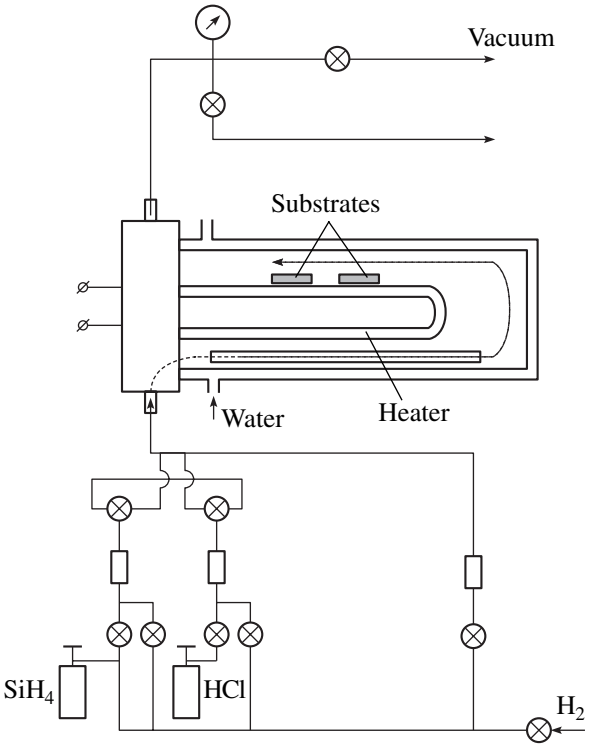

Fig. 1. Schematic of the apparatus for the growth of silicon epilayers.

grown epilayers were *n*-type, with a carrier concentration within 10^{12} cm^{-3}.

The electrical properties of the epilayers were assessed by determining the carrier concentration N due to electrically active impurities using capacitance–voltage (CV) measurements on an electrolyte/silicon barrier (electrochemical CV (ECV) measurements) [11] and, for comparison, on an Au/Si Schottky barrier. In addition, Hall effect measurements in a van der Pauw geometry were used as an independent technique. The presence of impurities producing deep centers in the band gap of silicon was ascertained by deep-level transient spectroscopy (DLTS) measurements [12] on a Schottky barrier.

ECV measurements provide more accurate carrier concentration depth profiles in comparison with standard CV measurements [11] and offer the possibility of measuring N in epilayers that have intricate depth profiles of the dopant. Because it has two measuring cells differing in area (2.6 and 10 mm in diameter), the ECV profiler enables determination of *p*- and *n*-type impurity concentrations in a broad range, from ~10^{13} to 10^{19} cm^{-3}. Throughout this concentration range, the error of determination is within ±15% for layer thicknesses no less than the width of the space charge region in electrolyte/semiconductor barriers.

Parameters of silicon epilayers

Thickness, μm	σ, deg	*W*, seconds of arc	
		substrate	film
4.35	1.60	13.5	13.9
4.30	1.60	13.5	13.7
4.90	1.50	13.7	14.1

The depth profiles of impurities in epilayers were obtained by CV measurements at a fixed low voltage (150–300 mV) in conjunction with successive electrochemical etching in the same cell. This profiling procedure is faster than standard CV measurements on metal/silicon barriers in combination with chemical etching of Si steps. Moreover, owing to some inherent features of the Si–electrolyte barrier potential, ECV profiling can be performed on thinner epilayers in comparison with Schottky barriers [11]. Consequently, smaller amounts of silane are needed to grow epilayers for assessing its purity.

Silane for epilayer growth was prepared through trichlorosilane disproportionation on an ion-exchange catalyst [13]. In our experiments, we used two different batches of silane, prepared by simple distillation and by fine purification via fractional distillation. The silane was analyzed by gas chromatography as described by Devyatykh and Krylov [14]. The analytical results indicated that the impurity concentration in the silane samples purified by distillation was below the detection limit (1×10^{-4} to 1×10^{-6} wt % for hydrocarbon impurities and 5×10^{-4} to 1×10^{-5} wt % for Group III to V hydrides).

The structural perfection of the epilayers and substrates was assessed using double-crystal x-ray diffraction [15]. The structural perfection was quantified by the full width at half maximum (FWHM) W of the rocking curves measured on the surface of the epilayer and the backside of the substrate using CuK_{α_1} radiation and the (001) crystallographic plane of the crystal monochromator and the crystal being studied. As the crystal monochromator, we used a structurally perfect germanium single crystal set to the symmetric 004 reflection. The rocking curves of the samples were measured using the symmetric 004 reflection. The x-ray penetration depth for this reflection was 1.5 μm, so that, in measurements on the epilayer surface, we recorded the beam reflected only from the epilayer since its thickness notably exceeded the x-ray penetration depth. The uncertainty in W was 0.5″, and that in the angle between the substrate surface and (001) plane (σ) was 0.05°. Our results on the structural perfection of the epilayers are summarized in the table.

RESULTS AND DISCUSSION

Determining the orientation of the substrate surface by rotating the sample about the normal to its surface [15–17], we found that the angle between the substrate

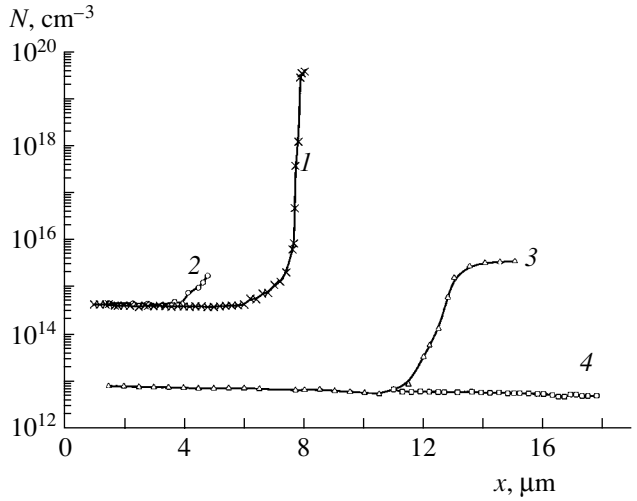

Fig. 2. Impurity profiles in silicon epilayers grown using two batches of silane: (*1*, *2*) first purification (simple distillation), (*3*, *4*) second purification (fractional distillation); measurements on (*1*, *3*) electrolyte/silicon and (*2*, *4*) Au/Si contacts.

surface and the (001) crystallographic plane was σ = 1.5°–1.6°. This small misorientation of the substrate surface had no significant effect on the width of the diffraction peaks from the substrate and epilayer. The grown silicon epilayers were single-crystalline, and their structural perfection ($W \sim 14''$) was close to that of the substrates (table).

The rocking curves of the silicon substrates used in epilayer growth had FWHM = 13.5″, which exceeds the intrinsic broadening predicted theoretically for single crystals (7.3″) [18]. It can be seen from the table that, in all of the samples, the W of the epilayer (0.2″–0.4″) exceeds that of the substrate only slightly.

All of the Si epilayers were *n*-type, independent of the silane used. The carrier concentration in the epilayers depended on the purity of the silane and varied from 8×10^{14} cm^{-3} in the case of the silane purified by simple distillation to $\leq 1 \times 10^{13}$ cm^{-3} in the case of the silane purified with the use of fractional distillation.

Figure 2 shows the impurity profiles in four silicon epilayers grown using the two batches of silane—after the first (simple distillation) (curves *1*, *2*) and second (fractional distillation) (curves *3*, *4*) purification cycles. The carrier concentration is 4×10^{14} cm^{-3} in the case of the silane purified by simple distillation and 8×10^{12} cm^{-3} after fractional distillation. The results in Fig. 2 were obtained by measurements on electrolyte/silicon contacts (curves *1*, *3*) and Au/Si barriers (curves *2*, *4*). The samples differed in thickness. Comparison of curves *3* and *4* clearly demonstrates one advantage of measurements in an electrolyte for the epilayers grown from the high-purity silane, purified by fractional distillation: for measurements on the Schottky barrier, the layer thickness must exceed 10 μm since, at zero bias, the space charge region in the Schottky barrier is ~10 μm in thickness. It is also seen in Fig. 2 that the carrier concentration is constant throughout the thickness of the epilayers, which was the case in most of our samples.

In addition to layers on heavily doped, n^+ substrates (KEM-0.05 silicon), we grew epilayers on high-resistivity *p*-type substrates (KDB-10 silicon) for CV and Hall measurements. Hall measurements are, however,

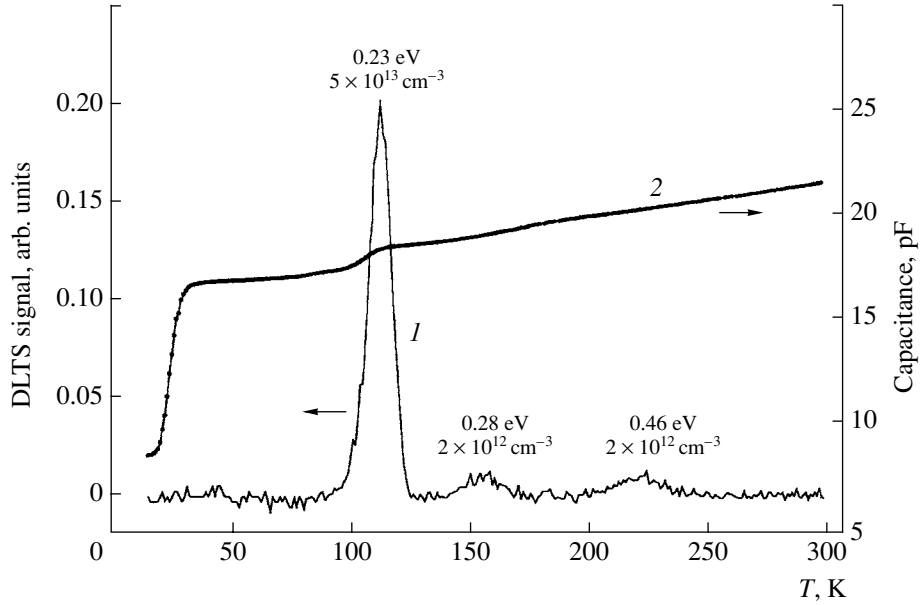

Fig. 3. (*1*) DLTS spectrum and (*2*) temperature-dependent capacitance of the Schottky contact for silicon epilayers grown from the first silane batch; the numbers at the peaks specify the concentrations and ionization energies of the corresponding levels; the carrier concentration in the epilayers at $T = 300$ K, $V_{sample} = 4$ V, and $f = 400$ kHz is $n = 4 \times 10^{14}$ cm^{-3}.

inapplicable in the case of epilayers with carrier concentrations of ~10^{13} cm^{-3} and below. For comparison with the electrical properties of the films, the purity of the silane purified by fractional distillation was determined by a well-known method, from the parameters of a reference silicon single crystal [9]. Hall measurements were performed on plates cut from a reference single crystal grown using the same batch of purified silane as the epilayers for CV measurements. The measurement results for the epilayers and reference single crystal were in good agreement. The carrier concentration determined from the Hall data for the reference single crystal was 9×10^{12} cm^{-3}.

Figure 3 shows the DLTS spectrum and the temperature-dependent capacitance of the Au/Si contact for the epilayers grown from the silane purified by simple distillation. The impurity profile in these epilayers is represented by curve *2* in Fig. 2. Analysis of the DLTS spectrum indicates that the carrier concentration in the epilayers is determined primarily by electrically active impurities with shallow levels in the band gap of silicon. The concentration of deep levels with ionization energies above 200 meV is 2×10^{12} to 5×10^{13} cm^{-3} (see Fig. 3), which is one order of magnitude lower than the concentration of shallow impurities. The ionization energies of the deep levels suggest that these originate from impurity–defect complexes forming during the epitaxial process [9].

In the epilayers grown from the silane purified by fractional distillation, the concentration of electrically active impurities (Fig. 2, curves *3*, *4*) was almost two orders of magnitude lower, and the concentration of deep impurities was below 10^{11} cm^{-3}. The good agreement between the electrical parameters of Si epilayers and reference single crystals suggests that the techniques we used are sufficiently accurate at impurity concentrations in epilayers on the order of 10^{13} cm^{-3}. Therefore, the purity of silane can be evaluated from the electrical parameters of Si epilayers grown from it.

CONCLUSIONS

High-purity silicon epilayers were grown through silane pyrolysis. The layers offer high structural perfection ($W \sim 14''$) and carrier concentrations within 10^{13} cm^{-3}.

The present results demonstrate that the purity of silane can be evaluated from the electrical parameters of Si epilayers grown from it.

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