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Properties of SiO₂ thin films prepared by anodic oxidation under UV illumination and rapid photothermal processing

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Abstract

Anodic oxidation under ultraviolet (UV) illumination and rapid photothermal processing technique used for high quality oxide preparation in terms of device surface passivation and gate or tunnel dielectrics are reported. A number of samples of SiO₂ thin films were prepared using this technique. It is shown that anodic oxidation under UV illumination followed by rapid photothermal processing (450 °C, 15 s) in the inert ambient yields the best optimization of the SiO₂ thin films properties. Avoiding high temperature process should result in a better performance of the semiconductor devices. Anodic oxidation under UV illumination at low temperature and post-oxidation photothermal processing can be a possible alternative to the furnace growth silicon oxide; not only because of the low temperature process, but also because this technology essential improves the oxides properties.

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1. Introduction

SiO₂ is one of the "building block" films used in making both simple and complex semiconductor devices. To grow SiO₂ films in typical integrated circuit fabrication, Si is exposed to high temperature (> $850 \,^{\circ}$ C) in the presence of dry or wet oxygen. When Si wafer is heated to a very high temperature for an extended period of time, dopants may migrate and create problems in the fabrication of active devices. Therefore, growing SiO₂ thin films rapidly at lower temperatures is desired. Also, in order to accommodate the perceived requirement for reduced thermal budgets in ULSI fabrications, many approaches to enhanced low temperature growth and the processing of thin high quality SiO₂ films have been investigated. These have included anodic oxidation technique [1-5], but much attention has also been focused on the use of photon annealing to the full fabrication process of SiO₂ instead of conventional quartz-tube furnace annealing [6–8].

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Avoiding high temperature process should result in a better performance of the silicon oxide thin films and respective of the fabricated devices [9–12].

2. Experimental

This work reports the properties of SiO_2 thin films prepared by anodic oxidation under UV illumination followed by rapid photothermal processing (RPP) used for high quality oxide preparation in terms of device surface passivation and gate or tunnel dielectrics. A number of SiO_2 samples were prepared using this technique and their properties have been investigated. It is shown that the combination of UV illumination and post-oxidation rapid photothermal processing in the inert ambient yields the best optimization of the SiO_2 properties.

Anodic oxidation at room temperature and post-oxidation rapid photothermal processing can be a possible alternative to the thermal growth silicon oxide; not only because of the low temperature process, but also because of enhanced oxides properties being obtained.

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2.1. Anodic processing technique

In this study, the substrate was the <100>-oriented *n*-Si. The substrates have been cleaned in hydrofluoric acid in two steps. First, cleaning in solution of sulfuric acid (H₂SO₄)/hydrogen peroxide (H₂O₂) (H₂SO₄:H₂O₂ = 1:4, sulfuric acid–peroxide mixture called SPM) for 5 min performed to remove any organic material and metallic impurities after redistilled water cleaning for 5 min. Second, cleaning by acetone and alcohols and the next step in a solution of dilated hydrofluoric acid (HF:H₂O = 5:100) was performed to remove chemical and native oxides which might have been formed on Si surface for 1 min and produced a stable surface with minimum contamination and low density of surface states. Finally the samples were cleaned in redistilled water.

Anodic oxidations of the *n*-Si wafers are made with UV illumination in order to generate the necessary holes at the silicon-oxide interface. Beynon et al. [10] have grown anodic oxide of 80–1100 Å thickness on $10 \Omega \text{ cm } n$ -Si wafers with p^+ diffusion at the backside. Mende and Kuster [11] have reported inhomogeneous SiO₂ growth and nucleation domains for films thinner than a minimum thickness of 350 Å. We have grown homogeneous SiO₂ layers in the silicon anodization process using EG–KNO₃–KNO₂ bath [2].

Homogeneous oxides were grown anodic by applying two different constant current densities. First, a small precurrent is applied and then the current is increased to a level that produces sufficient oxide growth of layers with thickness in the range of 180–1500 Å.

<100> oriented *n*-doped silicon wafers were oxidized, with the surfaces of the test cells in order of $1-5 \text{ cm}^2$.

Selection of the anodization bath was done from the following:

- (a) Mixture of 0.02 M KNO₂ and 0.02 M KNO₃ in ethyleneglycol used by Beynon et al. [10];
- (b) N-methylacetamide (NMA)–KNO₃ employed by Revesz [5] with small variations: 0.04 M KNO₃ in a nearly anhydrous bath or 0.001 M KNO₃ in 3% water bath;
- (c) ethyleneglycol (EG)–KNO₃ used by Mancheste; 0.1 M H₃BO₃–Na₂B₄O₇ water solution [12];
- (d) EG-0.4% KNO₃-10% H₂O solution used by Manara et al. [12];
- (e) electrolyte 1 M HCl used by Grecea et al. [13].

In order to select the anodizing bath was considered the flexibility and ease of use. A careful analysis from the point of view of the anodization technique has been performed for the electrolytes. The EG–KNO₃ bath has been investigated in [12], and obtained the best results by using the composition of an electrolyte: EG–0.4% KNO₃–10% H₂O.

In our investigations we obtained the best results using an electrolyte consisted of 0.03 M KNO_2 and 0.03 M KNO_3 in ethyleneglycol. During the oxidation process of the *n*-type silicon wafer the chemical bath was illuminated by a UV



Fig. 1. Voltage across the silicon slice vs. anodization time dependence of the current density: curve 1, process with UV illumination of chemical bath; curve 2, process without UV illumination.

lamp adjusted for minimum initial voltage. The electrolyte was stirred in order to prevent polarization effects at the both electrodes. The cathode was made from a platinum wire in form of spiral. The silicon probe was connected to a constant-current source. Voltage was monitored and after it had reached a predetermined value the current was allowed to decay to about 0.1 mA cm^{-2} and then disconnected. The silicon probe was cleaned again with redistilled water.

In this constant-current oxidation procedure the voltage across the silicon slice is a measure for the oxide thickness [2]. The UV light assisted growth can be controlled by the anode current in order to obtain a uniform oxide film. Experimentally was determined the applied initial current density of value 1.0 mA cm^{-2} for 15 min and then during SiO₂ growth the current was 3–4 mA cm⁻².

Fig. 1 shows dependence of voltage across the silicon slice during the oxidation process versus current density for cases: with UV illumination (curve 1) and without UV illumination (curve 2). Curve 1 describes the case when silicon slice is illuminated and are applied two regions of current I and II. In region I no increase in voltage is observed during the period of current I₁ (1.0 mA cm⁻²). From the experimental observations we can conclude that no oxide growth takes place during the period I of the current. Region II represents the growth period when applied current is in the range of 3-4 mA cm⁻². Was observed that initially the efficiency of the current is very low and a slow growth of SiO₂ and it seems this is the reason of the homogeneity of the oxide layers grown by described technique. Curve 2 represents anodization process without illumination and only one constant current density of 4 mA cm^{-2} . In this experiment due to a high initial voltage the oxide film was inhomogeneous.

The comparison of the properties of these two types of films evident shown that the anodic oxides grown without UV illumination could be grown only at high voltage (U > 90 V) and at a high growth rate (>20 Å min⁻¹), whereas the films under UV illumination starts to grow at low voltage (40–60 V), and low growth rate (3–7.5 Å min⁻¹). The oxides obtained at a high growth rate 60–90 Å min⁻¹ (without UV illumination) have a lower quality compare to the oxides grown under UV illumination: the nonhomogeneity of the



Fig. 2. Oxide thickness dependence on the net forming voltage for Si slices under UV illumination (growth rate 7.5 Å min^{-1}).

film thickness being $\pm 80\%$; nonlinearity of the film thickness dependence on anodic potential being ~100%; nonlinearity of the film thickness dependence on etching time $\pm 90\%$; the complex shape of the CV curves and large deviation of the threshold voltage. In this study, we present only the results of the anodic SiO₂ thin films grown under UV illumination with two current densities (I₁ = 1.0 mA cm⁻² + 5 min and I₂ = 3–4 mA cm⁻²).

This method of Si anodization was applied to obtain test samples oxide films with thickness in the range of 180–1500 Å. Was used an initial current with duration of 15 min and current densities of 3 mA cm^{-2} . As the film grew the potential difference across it increased. When this reached a predetermined value, the voltage was maintained at this value and the current decreased. This forming voltage was maintained until the current dropped to 0.1 mA cm^{-2} . Anodic potentials from 35 to 200 V were used to produce desired oxide thickness. Anodic SiO₂ films thickness was measured by ellipsometry.

Fig. 2 shows the oxide thickness dependence on the net forming voltage. The net voltage is the difference between the sample voltage and the initial applied voltage.

An extrapolation of the curve in Fig. 2 to thickness smaller than 300 Å comes very close to the origin and can be concluded that very thin SiO₂ films can be obtained by the described method on Si slices.

2.2. Rapid photothermal processing technique

Annealing is the most important process for removing the defects and improving the properties of the oxide films. Halogen Lamp-based RPP systems have been introduced as an alternative thermal processing equipment solution. The lamp-based RPP system provides short cycle time, reduced exposure and flexibility compared to batch-type furnaces. Allowable thermal budget has decreased as device dimensions. Strong demand in thermal budget reduction and cycle time reduction made RTP becomes a very popular thermal processing method in recent years [1,3,15]. Schematic diagram of a rapid photothermal processing system with a vacuum loadlock used in this study is shown in Fig. 3 [3].

As formed anodic oxide films contain strained Si–O bonds, Si–OH and Si–H groups, absorbed water, glycol oxidation products [4,12], and ionic impurities (e.g., Na ions). The capacitance–voltage curves of such MOS structures with as formed anodic oxide shown unstable behavior and were irregular, and the surface charge density is very high (greater than 5×10^{11} electronic charges/cm², respective) [12,14]. Therefore, anodic grown silicon oxide films must be cleaned with HC1–H₂O₂–H₂O, and annealed in a dry inert ambient at different temperatures and durations, immediately after anodization process, using the lamp based RPP system.

The oxides were processed in a RPP IFO-6 system for 2, 4, 6, 8 and 15 s at temperatures of 100, 200, 350, 400, 450 and 500 °C under 1 atm dry N₂ ambient. The comparison of resulting characteristics and their uniformity after RPP shown that the optimal RPP temperature is 450 °C. Fig. 4 shows a typical wafer temperature profile during processing at 500 °C.

The thickness and refractive index of the oxide film were determined by ellipsometry. The refractive indexes of the anodic oxide grown under UV illumination and without it are in order of 1.45-1.46 and 1.47-1.5, and the error of uniformity is in order of 1'-20' and $1^{\circ}20'-2^{\circ}20'$, respectively. The variations of refractive index *n* value is determined by the modifications in the local atomic structure of oxide films. The decrease of *n* value is explained by the increase in films density and by replacement of Si–Si bonds by Si–O bonds.



Fig. 3. Schematic diagram of the rapid photothermal processing module IFO-6.



Fig. 4. Schematic illustration of wafers temperature profile during a 20 s process in the IFO-6 lamp-based RPP system.

After RPP the Al contacts were deposited by thermal evaporation in vacuum system VUP-4. The MOS capacitor structure has been used for investigating the electrical properties of the oxide and also the characteristics of the Si/SiO₂-interface. The samples were investigated by high-frequency 1 MHz capacitance–voltage (hf-C-V) measurements and by the current–voltage (I-V) measurements.

Fig. 5 plots the comparison of high-frequency C-V characteristics of an *n*-type substrate MOS structure with thermal oxide obtained in dry O₂ + HCl, followed by annealing in N₂, for gate dielectric before and after rapid photothermal processing at 450 °C for 15 s in the inert ambient.

The hf-C-V of the as-grown anodic oxide MOS structure was very irregular due to the high surface states density, and in order to enhance the properties the final voltage value during anodization was maintained (depending on desired thickness value, Fig. 2) till the current decreased to 0.1 mA cm^{-2} .

Fig. 6 shows the high-frequency C-V characteristics of an aluminum/anodic oxide film/*n*-type Si substrate MOS struc-



Fig. 5. Typical hf-C-V curves of MOS structures with thermal grown oxide film (820 Å, growth rate 11.7 Å min⁻¹) on *n*-type silicon: initial (full line) and after RPP at 450 °C for 15 s in N₂ ambient (dotted line).



Fig. 6. Hf-*C*–*V* curves of MOS structures with anodic oxide film on *n*-Si (335 Å, growth rate 5.1 Å min^{-1}): curve 1, initial; curve 2, after RPP at 450 °C for 15 s in N₂ ambient.

ture obtained as described above, initial and after RPP at 450 $^\circ C$ for 15 s in dry N_2 ambient.

3. Results and discussion

From C-V measurements of Al MOS capacitors, it was calculated according to Terman [16] the surface charge density 5×10^{11} electronic charges/cm² in the as grown anodic oxide and 1×10^{11} electronic charges/cm² after rapid photothermal processing for 15 s at 450 °C in dry N₂ ambient. Surface charge density of thermal oxides is 2×10^{11} electronic charges/cm² before and 6.7×10^{10} electronic charges/cm² after RPP.

The interface state density $N_{\rm SS}$ of thermal1 oxide is $3 \times 10^{11} \, {\rm eV^{-1} \, cm^{-2}}$ before and $3 \times 10^{10} \, {\rm eV^{-1} \, cm^{-2}}$ after RPP. For the anodic oxides the interface state density is $2.8 \times 10^{11} \, {\rm eV^{-1} \, cm^{-2}}$ before and $4 \times 10^{10} \, {\rm eV^{-1} \, cm^{-2}}$ after RPP at 450 °C for 15 s in N₂ ambient.

The total amount of interface traps is generally very small in the samples with KNO_2 and KNO_3 ethyleneglycol mixture-anodic oxide used as the MOS structure dielectric. The rapid photothermal processing anneals the traps in the oxide but at the same time they depend on technological history of the samples and the anodic oxide quality. As there is no higher temperatures (>700 °C) process involved and the oxidation was performed in a slow fashion, the number of oxidation induced defects can be minimized.

The breakdown field strength of the oxide was determined from the voltage required for catastrophic breakdown of the studied MOS structure. Breakdown of the SiO₂ was measured for positive bias voltage such that the surface of the *n*-type silicon immediately under the gate was in accumulation. The breakdown field strength of thermal oxide can be as high as $7 \times 10^6 \text{ V cm}^{-1}$, whereas the breakdown field of anodic oxide prepared using mixture of KNO₂ and KNO₃ in ethyleneglycol and UV light assistance is about $4 \times 10^6 \text{ V cm}^{-1}$.



Fig. 7. Breakdown voltage of anodic oxide films as a function of the oxide thickness, initial and after RPP at 450 °C for 15 s in inert ambient.

After RPP of the oxides for 15 s at 450 °C in N₂ ambient the breakdown field strength can be enhanced to 1.1×10^7 and 1.0×10^7 V cm⁻¹, respectively. Higher breakdown can be found in thinner anodic oxides, after RPP, about 1.2×10^7 V cm⁻¹ for 320 Å oxide (growth rate 5.1 Å min⁻¹) as shown in Fig. 7.

The reproducible characteristics of the oxide prepared with this approach is well defined even when a very thin oxide is required.

Also oxide quality can be determined by the etching rate of SiO₂. In the chemical etching, the prepared samples were soaked in HF buffer (HF:H₂O 1:50) for a determined period of time. The results for thermal (growth rate 11.7 Å min^{-1}) and anodic oxides (growth rate 5.1 Å min^{-1}) initial and after RPP are shown in Fig. 8 as the oxide thickness function of the etching time. It was found that the etching rate of anodic oxide is higher than that of thermal oxide. For the thermal oxide the etching rate is about 4 Å s^{-1} . while that of anodic oxide is 15 Å s^{-1} . After RPP the slope was reduced to 6 Å s^{-1} . From these observations we can conclude that the stoichiometry of the anodic oxides is not the same as those of thermal oxides prepared in dry O₂.

Rapid photothermal processing can result in the partial restructuring of the oxide.

Further research of the effects of wafer temperature ramp up/down rates, annealing temperatures and anneal-



Fig. 8. Oxide thickness vs. etching time for anodic and thermal oxides.

ing time influence on anodic SiO_2 thin films is under progress.

4. Conclusions

In this work we report that the rapid photothermal processing of silicon oxides in an IFO-6 RPP system improved the electrical and dielectric properties that are comparable to or better that those of furnace oxides. Parameters included in this statement are surface charge densities in oxide, interface state densities and breakdown field strength. Indeed, it has been shown that surface charge density is 6.7×10^{10} electronic charges/cm² after RPP for conventional furnace oxides and 1×10^{11} electronic charges/cm² for anodic oxides. The charge-to-breakdown is directly related to the trapping of electrons that are injected into the oxide. As there is no higher temperature process involved in the anodic deposition the silicon oxides have fewer trapping centers, resulting in better reliability. Since RPP can be performed in the IFO-6 chamber at lower temperatures than in situ furnace annealing, the expected improvement in interface traps can be observed. A comparison of hf-C-Vcurves of the furnace oxides and anodic oxides is shown in Figs. 5 and 6.

As result of the present research can be proposed the anodic oxidation of Si and rapid photothermal processing technique which permit to fabricate SiO₂ films with several enhanced electrical characteristics: such as low interface state density and higher breakdown fields strength. Anodic oxides obtained using this nonconventional technique using the UV assistance and precurrent process can hardly be used in making both simple and complex semiconductor devices, also used for passivation of heat sensitive materials (a-Si:H), high resistivity Si, rough poly Si, passivation of Si structures and gate dielectric in MOS structures. We apply these anodic oxides in thin film transistors with zinc oxide transparent window.

References

- A. Paskaleva, E. Atanassova, G. Beshkov, J. Non-Cryst. Solids 187 (1995) 35.
- [2] T. Shishiyanu, V. Shontya, O. Lupan, I. Pocaznoi, S. Railean, S. Shishiyanu, in: Proceedings of the IVth International Conference on Reliability of Semiconductor Devices and Systems RSDS'96, Chisinau-Moldova, 1996, p. 94.
- [3] S.T. Şişianu, T.S. Şişianu, S.K. Railean, Semiconductors 36 (5) (2002) 581 (Trans.; from Fizika i Tekhnika Poluprovodnikov (J. Phys. Tech. Semicond.), 36 (5) (2002) 611).
- [4] G. Mende, H. Fliether, J. Electrochem. Soc. 140 (1) (1993) 188.
- [5] A.G. Revesz, Phys. Stat. Sol. 24 (1) (1967) 115.
- [6] T. Hori, H. Iwasaki, K. Tsuji, IEEE Trans. Electron. Devices 36 (2) (1989) 340.
- [7] E. Kobeda, M. Kellam, C.M. Osburn, J. Electrochem. Soc. 138 (6) (1991) 1846.
- [8] E. San Andrés, A. del Prado, F.L. Martínez, I. Mártil, D. Bravo, F.J. López, J. Appl. Phys. 87 (3) (2000) 1187.

- [9] W.K. Choi, C.K. Choo, Y.F. Lu, J. Appl. Phys. 80 (10) (1996) 5837.
- [10] J.D.E. Beynon, G.G. Bloodworth, I.M. McLeod, Solid-State Electron. 16 (3) (1973) 309.
- [11] G. Mende, G. Kuster, Thin Solid Films 35 (2) (1976) 215.
- [12] A. Manara, A. Ostidich, G. Pedroli, G. Restelli, Thin Solid Films 8 (1971) 359.
- [13] M. Grecea, C. Rotaru, N. Nastase, G. Craciun, J. Mol. Struct. 480/481 (1999) 607.
- [14] J. Bardwell, K.B. Clark, D.F. Mitchell, D.A. Bisaillion, G.I. Sproule, B. MacDougall, M.J. Graham, J. Electrochem. Soc. 140 (8) (1993) 2135.
- [15] A. Paskaleva, E. Atanassova, G. Beshkov, J. Phys. D: Appl. Phys. 28 (5) (1995) 906.
- [16] L.M. Terman, Solid-State Electron. 5 (1962) 285.