Journal of The Electrochemical Society, **156** (8) H661-H668 (2009)
0013-4651/2009/156(8)/H661/8/$25.00 © The Electrochemical Society

Charge Trapping Related Degradation of Thin $HfAlO/SiO_2$ Gate Dielectric Stack during Constant-Voltage Stress

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Charge carrier generation/trapping and the related degradation of a thin $HfAlO/SiO_2$ stack in n-type metal-oxide-semiconductor capacitors have been investigated under constant gate voltage stress. The results show that dielectric degradation is a composite effect of neutral trap creation, surface state generation at the Si/SiO_2 interface, and positive charge trapping in the bulk. The neutral traps created during stress are homogeneously distributed across the oxide following Poisson's random statistics. A significant amount of border-trapped charges was observed in both as-deposited and poststressed devices. The kinetics of generation of both oxide-trapped positive charges and interface trapped charges are found to be similar. Both these defects are possibly created by the hydrogen-related species. We demonstrate that compared to HfO_2 devices, HfAlO devices with an equal equivalent oxide thickness (EOT) show better performances in memory and logic applications. On the contrary, at a given stress voltage, the threshold voltage degradation ΔV_T and stress-induced leakage current degradation in HfAlO samples are larger, indicating a shorter device lifetime compared to the HfO_2 samples of the same EOT.
 [DOI: 10.1149/1.3148203]

Manuscript submitted March 23, 2009; revised manuscript received May 8, 2009. Published June 18, 2009.

Scaling down the conventional silicon dioxide (SiO_2) film thickness below ~2 nm in complementary metal oxide semiconductor (CMOS) devices leads to excessive leakage current due to the direct tunneling of electrons between the electrodes and device reliability problems. To provide sufficient gate control with reduced gate leakage current, alternative high-κ dielectrics having a permittivity higher than SiO_2 are being extensively investigated for future generation CMOS devices.[1-17] Among the various high-κ dielectrics being studied, hafnium oxide (HfO_2) has emerged as the most promising candidate due to its relatively high dielectric constant (~ 22), large bandgap (~ 5.25 eV), large conduction- and valence-band offsets, and compatibility with the polysilicon gate process.[2,7,17] However, the major drawback of HfO_2 is that pure as-deposited amorphous HfO_2 crystallizes[6,7] at 400–450°C, resulting in a large leakage current and the paths for oxygen or dopant diffusion in the dielectric via grain boundaries, threshold voltage instability, and defect generation.[7,8] Recently, Zhu et al.[6] showed that alloying of HfO_2 and Al_2O_3 increases the crystallization temperature up to 1000°C compatible with the thermal budget in standard CMOS process. In the past few years, considerable progress has been made in understanding the effect of aluminum inclusion on electrical and material properties of hafnium aluminate (HfAlO) films.[6-10] However, little work[11,12] has been done in assessing the reliability of HfAlO films with a tantalum nitride (TaN) gate. We therefore attempt to investigate charge-carrier generation/trapping in HfAlO dielectrics during constant voltage stress (CVS) to gain better physical insights into the generation mechanism of oxide charges.

Experimental

Following the standard RCA cleaning process, (100)-oriented boron-doped p-type Si wafer of 15–25 Ω cm resistivity was thermally oxidized in dry oxygen at 800°C to form an interfacial SiO_2 2 nm thick as measured by spectroscopic ellipsometry. A 2 nm thick HfAlO film was deposited on the SiO_2 layer using atomic layer deposition from a HfO_2–Al_2O_3 combination with a 1:1 weight ratio. After formation of the gate stack, a 100 nm thick TaN metal gate was deposited by reactive sputtering on top of the high-κ layer. All n-type metal-oxide-semiconductor (nMOS) capacitors received postmetallization rapid thermal annealing at 750°C in N_2 gas for 30 s and back side aluminum deposition for ohmic contact. Several identical test capacitors with gate areas of 150 × 150, 100 × 100, and 50 × 50 μm were used in this study. Devices were subjected to dc CVS under negative bias on the TaN gate, keeping the p-type Si in accumulation. Stressing and sensing measurements were done on several identical test structures at room temperature in a dark-shielded chamber using a Keithley 4200 semiconductor characterization system (SCS) and Keithley 236 source measure units. Capacitance–voltage (*C-V*) measurements were done using an Agilent 4284A precision *LCR* meter controlled by SCS via a Keithley 708A switching matrix.

The flatband voltage (V_{FB}), midgap voltage (V_{mg}), and the channel threshold voltage (V_T) were estimated utilizing the measured high frequency (100 kHz) *C-V* data (swept from inversion to accumulation) and theoretical simulation incorporating the quantum mechanical (QM) effect including the wave function penetration in SiO_2.[18] From QM simulation, the extracted equivalent oxide thickness (EOT) of the stack was ≈2.63 nm (within 5% variation in several devices). The capacitance equivalent thickness extracted from the measured capacitance in accumulation was ≈2.83 nm. The calculated dielectric constant of the deposited HfAlO was about 12.4.

Results and Discussion

Device characterization.— The measured *C-V* characteristics with as-deposited HfAlO films exhibit a good saturation behavior in accumulation of p-Si at the ac signal frequencies in the range between 1 and 200 kHz, as shown in Fig. 1a. In Fig. 1a the frequency dispersion in the effective dielectric constant of the HfAlO stack was insignificant, indicating a low series resistance associated with the device structure. This is further supported by the identical values of the capacitances measured in the accumulation regime in both series and parallel mode at a given bias and frequency, as depicted in Fig. 1b. Therefore, hereafter in assessing the dielectric quality during stress, the *C-V* curves were measured in parallel mode at an ac signal frequency of 100 kHz. A low series resistance of the device structure was achieved due to the ohmic contact of the back side of the wafer. The energy band diagram of the nMOS capacitors with a $HfAlO/SiO_2$ stack is shown in Fig. 2a taking the work function of TaN on HfAlO as 4.5 eV.[12] The important energy parameters, viz., conduction- and valence-band offsets, bandgap of HfAlO as depicted in Fig. 2a, were estimated according to the prescriptions by Yu et al.[17] and taking mole fraction of HfO_2 in $(HfO_2)_x$ $(Al_2O_3)_{1-x}$ as 0.5.

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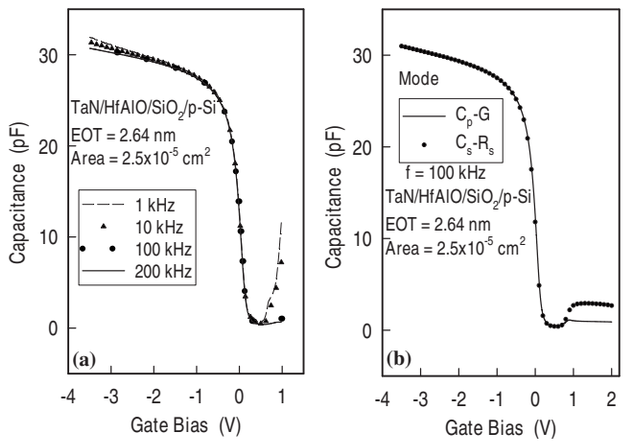

Figure 1. (a) A typical multifrequency capacitance–voltage (*C-V*) plot of an nMOS capacitor with a $HfAlO/SiO_2$ gate stack. (b) *C-V* plot of a HfAlO MOS capacitor in series and parallel modes at an ac signal frequency of 100 kHz. All measurements were recorded by sweeping the gate bias from inversion to accumulation of the p-Si.

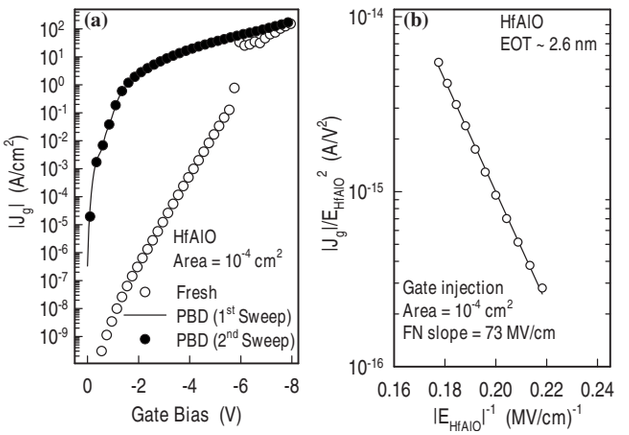

Figure 3. Absolute magnitude of gate tunneling current density J_g as a function of (a) applied gate bias and (b) electric field across the HfAlO layer.

From the full QM simulation of the measured *C-V* results, the estimated V_{FB} of the as-fabricated capacitors was ≈+0.19 V. The positive V_{FB} caused due to incorporation of Al into HfO_2 was also reported by several researchers.[7,9] Considering the work function difference between the p-type Si substrate and TaN metal gate, V_{FB} should be about −0.25 V. Consequently, negative fixed charges were present in the $HfAlO/SiO_2$ stack and its density was estimated to be about 3.5×10^{12} cm^{-2}. As-fabricated HfAlO capacitors exhibit a significant hysteresis during double-bias sweep measurement, as depicted in Fig. 2b. About 138 mV of negative V_{FB} shift was observed after the second sweep, i.e., when going back to inversion from accumulation, as illustrated in Fig. 2b. We believe that the *C-V* hysteresis in the metal-oxide-semiconductor (MOS) capacitor is attributed to electron charging and discharging by direct tunneling through the ultrathin SiO_2 to the substrate. From the above value of V_{FB} shift, the effective density of detrapped electrons was found to be about 1.1×10^{12} cm^{-2}.

Figure 3a shows the tunneling current density J_g as a function of applied gate bias keeping p-Si in accumulation. Multiple breakdowns were not observed in the HfAlO devices up to the voltage range studied here. The overlapping of the postbreakdown sweep *J-V* characteristics in Fig. 3a indicates hard breakdown. At an electric field E_{hk} above 4 MV/cm in the HfAlO layer and before dielectric breakdown, the current through the HfAlO layer is due to Fowler–Nordheim (FN) tunneling,[19] as seen from the straight-line fit to $\ln(J_g/E_{hk}^2)$ vs $1/E_{hk}$ plot of the measurement results illustrated in Fig. 3b. The FN slope during gate injection in as-fabricated HfAlO devices was 73 MV/cm as estimated from numerical fit of the measured data with the well-known FN equation[19] given by

$$J_{FN} = A_{FN}E_{hk}^2 \exp(-B_{FN}/E_{hk}) \quad [1]$$

where A_{FN} and B_{FN} are constants and E_{hk} is the electric field across the HfAlO layer as calculated from

$$E_{hk} = \frac{V_{hk}}{T_{hk}} = \frac{V_{di}}{T_{hk} + \left(\frac{\varepsilon_{hk}}{\varepsilon_{ox}}\right)T_{ox}} \quad [2a]$$

$$V_{di} = V_g - V_{FB} - \psi_{Si} \quad [2b]$$

where V_{hk} is the voltage drop in the high-κ layer, T_{ox} and T_{hk} are the physical thicknesses of SiO_2 (permittivity ε_{ox}) and high-κ dielectric (permittivity ε_{hk}), respectively, and V_{di} is the voltage drop across the dielectric stack. V_g, V_{FB}, and ψ_{Si} are the gate voltage, flatband voltage, and surface potential in silicon, respectively.

To study the wafer level reliability, we have performed the ramped voltage stress (RVS) measurement with a step size of 0.03 V corresponding to a linear voltage ramp rate of about 0.75 MV/cm s in several identical capacitors of various gate areas. The statistics of dielectric breakdown voltage V_{BD} obeys the Weibull distribution given by

$$F(V_{BD}) = 1 - \exp\left\{-\left(\frac{V_{BD}}{\alpha}\right)^{\beta}\right\} \quad [3]$$

where F is the cumulative failure probability, V_{BD} is the random variable for breakdown voltage, α is the breakdown voltage at the failure percentage of 63.2%, and β is the shape factor or Weibull slope. In Fig. 4a, the time-zero dielectric breakdown voltage (V_{BD}) distributions are shown for various capacitor sizes. The gate voltages to breakdown $V_{g,BD}$ were taken from the sweep *I-V* characteristics during RVS. Using Eq. 2b, V_{BD} was estimated from the measured values of $V_{g,BD}$, V_{FB}, and ϕ_{Si} of each individual capacitor. If the breakdown distributions follow Poisson's random statistics, we have[20]

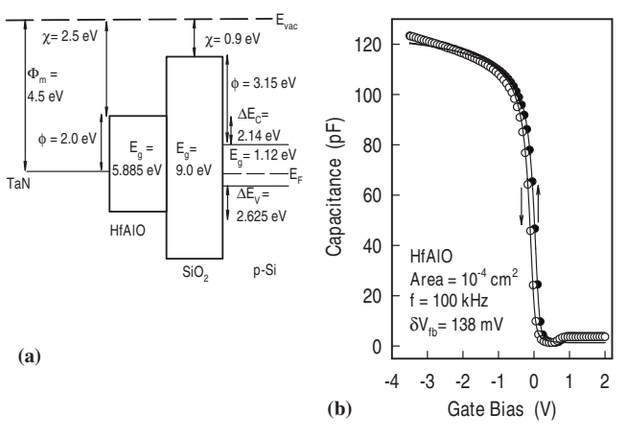

Figure 2. (a) Schematic energy band diagram of nMOS capacitor with $HfAlO/SiO_2$ stack. (b) Bidirectional HFCV characteristics of a virgin nMOS capacitor with a $HfAlO/SiO_2$ stack dielectric. Data were recorded from inversion to accumulation (solid circles) and back to inversion (open circles). Solid lines are from QM simulation.

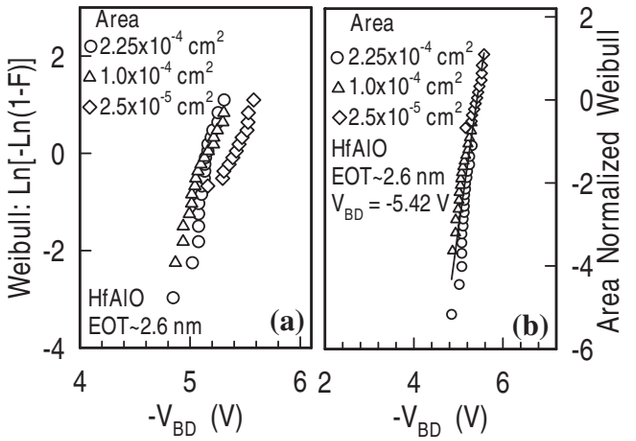

Figure 4. (a) Individual Weibull distributions of breakdown voltage V_{BD} of HfAlO capacitors for different areas. (b) Normalized Weibull plot of V_{BD} with the identical data from (a) by using Eq. 4 at a reference area of 2.5 $\times 10^{-5}$ cm^2. Line is the fit to Weibull statistics. The dielectric breakdown voltage at 63.2% of failure percentile was estimated at 5.42 V.

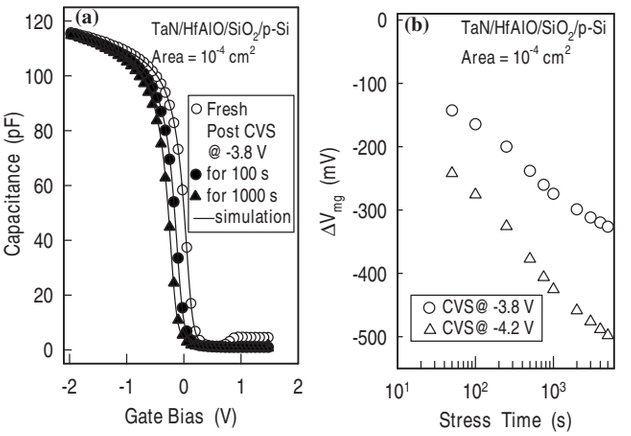

Figure 5. (a) HFCV characteristics of an nMOS capacitor with a HfAlO/SiO_2 stack dielectric measured before and after CVS at −3.8 V for different times. Solid lines are from QM simulation.[16] (b) Stress time dependence of midgap voltage shift during CVS with stress voltage V_g^{stress} as a parameter. Solid lines are from power-law fit.

$$\ln\{-\ln[1-F(V_{BD1})]\} - \ln\{-\ln[1-F(V_{BD2})]\} = \ln\left(\frac{S_1}{S_2}\right) \quad [4]$$

where V_{BD1} and V_{BD2} are the dielectric voltages to breakdown for capacitors with areas S_1 and S_2, respectively. Figure 4b shows area-scaled Weibull $W \equiv \ln[-\ln(1-F)]$, where the individual V_{BD} distributions for different gate areas are normalized to 2.5 $\times 10^{-5}$ cm^2 using Eq. 4. In Fig. 4b the normalized V_{BD} distributions of various capacitor areas merge to a single Weibull breakdown distribution, indicating[20] that the defect-related dielectric breakdown is intrinsic and can be explained by the precolation model.[21] Furthermore, the overlap of the area-scaled Weibulls of capacitors of various sizes, as shown in Fig. 4b, reveals that the defects in the dielectric are homogeneously distributed across the oxide area following Poisson random statistics.[20] From the merged Weibull distribution of V_{BD}, the estimated dielectric breakdown voltage at 63.2% failure percentile was −5.42 V which corresponds to 20.6 and 6.5 MV/cm of the electric fields across the interfacial SiO_2 and HfAlO layers, respectively.

Charge carrier trapping.— To study the stress-induced charge generation/trapping in the gate stack, high frequency capacitance–voltage (HFCV) measurements were performed before and after CVS. In our devices, HFCV curves shifted toward more negative voltage after CVS, as depicted in Fig. 5a, indicating positive charge buildup[22] in the gate dielectric. Positive oxide charge trapping was further confirmed (Fig. 5b) from the negative shift ΔV_{mg} of the midgap voltage after electrical stress relative to the fresh device following the relationship[2,14]

$$\Delta N_{ot} = -\frac{\Delta V_{mg}\varepsilon_{ox}}{qT_{eq}} \quad [5]$$

where q is the magnitude of electronic charge, T_{eq} is the EOT of the gate stack, and ΔN_{ot} is the variation in the density of stress-induced oxide-trapped charges. The variations in the density of stress-induced oxide-trapped positive charges ΔN_{ot}^{+} are shown in Fig. 6 as a function of stress time during CVS at various stress voltages. *C-V* measurement is sensitive to the charges trapped closer to the Si/SiO_2 interface.[22] Consequently, the positive oxide charge is located close to the Si/SiO_2 interface.[13]

The change in the conductance peak value after CVS relative to the virgin device shown in Fig. 7a indicates interface state D_{it} generation during stress.[22] Estimated midgap surface state density D_{it} in as-fabricated devices was (2–3) $\times 10^{10}$ cm^{-2} eV^{-1}. The instantaneous value of D_{it} was calculated from the single high frequency (100 kHz) *C-V* and *G-V* data according to[23]

$$D_{it} = \left\{\frac{2(G_{m,max}/\omega)}{qS}\right\}\left[\left(\frac{G_{m,max}}{\omega C_{ox}}\right)^2 + \left(1-\frac{C_m}{C_{ox}}\right)^2\right]^{-1} \quad [6]$$

where $G_{m,max}$ is the maximum ac conductance with its corresponding capacitance C_m, C_{ox} is the oxide capacitance as measured from the QM simulation,[18] and S and ω are the capacitor area and ac signal frequency in rad/s, respectively. Figure 7b shows the variation in the density of stress-induced interface states ΔD_{it} at various values of V_g^{stress}. Similar to the oxide-trapped positive charges, interface state generation is accelerated with increasing V_g^{stress}, which in turn is related to the electron energy reaching the anode.

SILC.— The gate current density at a given sensing gate voltage V_g^{sense} increases after CVS. This increase ΔJ_g in gate current from its prestress value J_{g0} is called the stress-induced leakage current (SILC) and is often described by the "normalized SILC" defined as $\Delta J_g/J_{g0}$. Figure 8a is a typical plot showing the normalized SILC

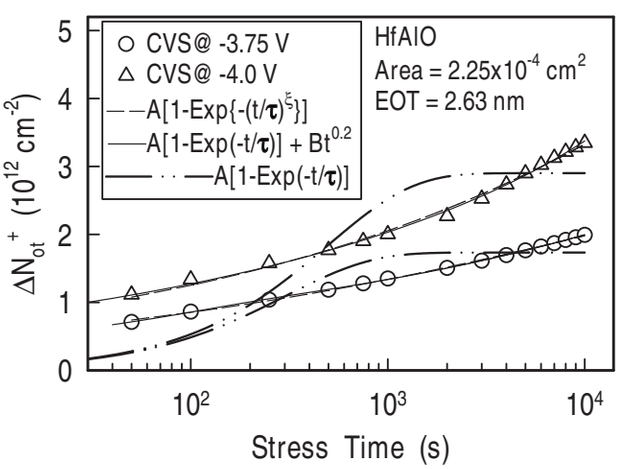

Figure 6. Variation in the density of oxide-trapped positive charges ΔN_{ot}^{+} with stress time during CVS at different voltages. Symbols are from experiment. Curves are fits to various theoretical models.

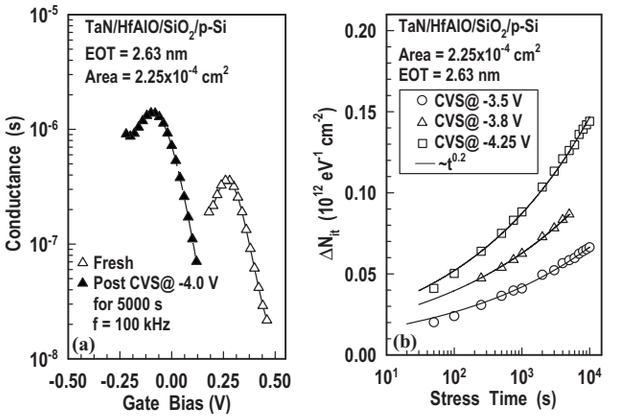

Figure 7. (a) High frequency conductance–voltage characteristics (parallel mode) of an nMOS capacitor with a $HfAlO/SiO_2$ stack dielectric measured before and after CVS at −4.0 V for 5000 s. (b) Variation in the density of surface states ΔD_{it} with stress time during CVS at different voltages. Symbols are from experiment. Curves are from power-law fits.

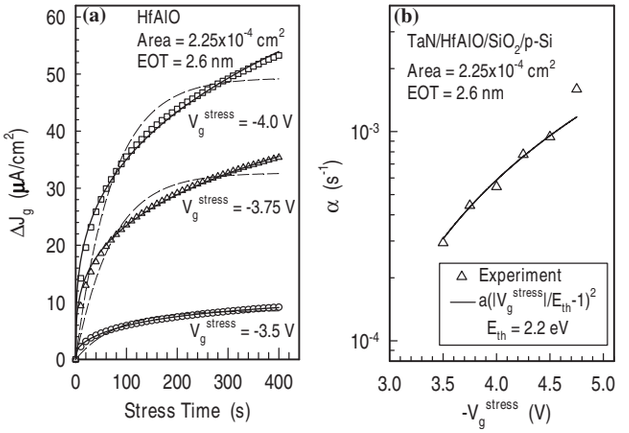

Figure 9. (a) Stress time dependence of the increase in absolute magnitude of tunneling current density J_g relative to the fresh device observed during CVS with stress voltage as a parameter. Solid and dashed lines are fits to Eq. 7 and the first term on right side of Eq. 7, respectively. (b) Normalized trap generation rate per injected electron as a function of stress voltage in a MOS capacitor with a $HfAlO/SiO_2$ stack. Solid line is fit to Eq. 8.

spectra measured immediately after CVS at −4.0 V for different times. The normalized SILC spectra show two distinct peaks at $V_g^{sense} = -2.175$ and −2.625 V, indicating two distinct conducting paths. To explain the SILC conduction mechanism, Ghetti et al.[24] proposed trap-assisted tunneling (TAT) via surface states in control oxide devices. However, although a significant amount of interface states is generated during CVS, TAT via surface states cannot explain the observed SILC in our HfAlO devices as explained below. First, TAT via D_{it} to be the conduction mechanism of SILC, normalized SILC at a given V_g^{sense}, should exhibit a proportionality to the surface state density D_{it} as proposed by Ghetti et al.[24] However, no proportionality between either of the two peak values in the normalized SILC spectrum and D_{it} is observed in our devices, as demonstrated in Fig. 8b. Second, stress-induced interface traps are the trivalent $Si_3 \equiv Si^*$ dangling bonds, so-called P_{b0} centers[4] exhibiting U-shaped distribution[22] in the 1.12 eV bandgap of Si. Therefore, for TAT via interface states to be a possible mechanism of SILC, the normalized SILC spectrum should exhibit several peaks contrary to the observed two peaks shown in Fig. 8a. In view of the above, we propose that stress-induced interface traps do not play a role in the SILC observed beyond V_{FB} through the HfAlO stack deposited on nondegenerately doped Si, contrary to the article[24] dealing in devices on heavily doped Si.

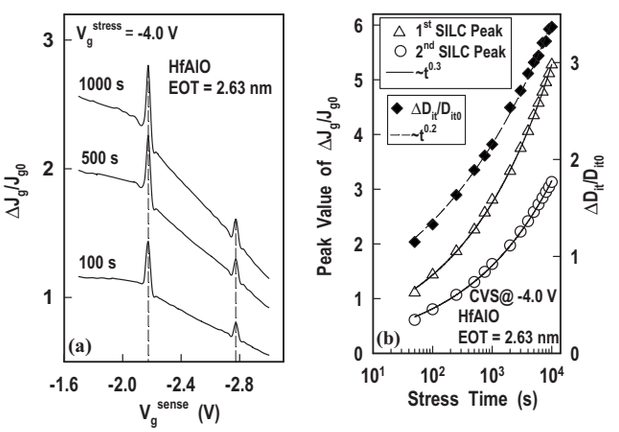

Figure 8. (a) Normalized SILC measured after CVS at −4.0 V for different times as a function of gate sensing voltage in an nMOS capacitor with $HfAlO/SiO_2$ gate stack. (b) Plot of two peaks in the normalized SILC spectrum (open symbols) measured after CVS at −4.0 V (left *y*-axis) and generated surface state density normalized to its initial value D_{it0} (filled symbols) (right *y*-axis) as a function of injected electron fluence Q_{inj}. Curves are from power-law fits.

Stress-induced neutral trap creation in our devices is evident from the nonsaturating behavior of the time evolution of J_g during CVS for different stress voltages, as depicted in Fig. 9a. The nonsaturating behavior of J_g was also observed at a longer stress time up to 10,000 s. This increase in J_g could be due to the enhanced electric field at the cathode (TaN gate) due to the trapped positive oxide charge and/or due to the TAT.[25] Therefore, the increment $\Delta J_g(t)$ in J_g during CVS can be modeled by[3,5]

$$\Delta J_g = A\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] + Bt^{\delta} \qquad [7]$$

where A and τ are constants, δ is a fraction depending on the charge state and atomicity of hydrogen during transport, and B is the trap generation rate during CVS and is a function of electronic energy. The first term on the right side of Eq. 7 takes into account the effect of oxide charge buildup, while the second term takes care of the SILC contribution via TAT. The first term alone cannot explain the observed $\Delta J_g - t$ variations in either of the devices, as evident from the dashed lines in Fig. 9a. Therefore, the increase in J_g is less sensitive to the positive charge buildup in the dielectric. Rather, the time evolution ($t^{0.3}$ dependence) of J_g during CVS can be best explained by the composite effects of the above two mechanisms (solid lines), as illustrated in Fig. 9a. Neutral electron trap creation rate per injected electron in HfAlO capacitors is also shown in Fig. 9b as a function of absolute magnitude of applied gate voltage during CVS. The normalized value of the trap creation rate is $Bt_{stress}^{\delta}/Q_{inj}$, where t_{stress} is the total stress time at which the gate voltage is interrupted[3] and Q_{inj} is the injected electron flux during the electrical stress. Evidently trap creation rate dN_t/dt follows[5]

$$\frac{dN_t}{dt} = C\left(\frac{|V_g^{stress}|}{E_{th}} - 1\right)^2 \qquad [8]$$

where C is a constant and E_{th} is the threshold voltage for trap creation. The estimated value of E_{th} in HfAlO dielectric was found 2.2 eV.

Mechanism of charge carrier generation.— The origin of positive oxide charge in a hafnium-based gate stack remains controversial between trapping of holes[11,12,26,27] and protons.[3-5] The above

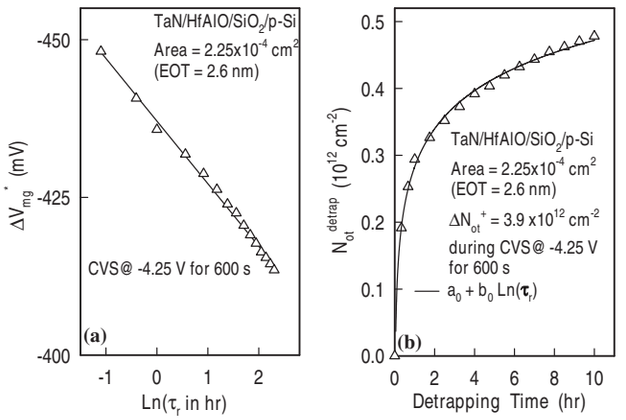

Figure 10. (a) Measured midgap voltage shift ΔV^{*}_{mg} due to detrapping of oxide positive charges at room temperature as a function of logarithmic time τ_r. Oxide positive charges were trapped at room temperature during CVS at −4.25 V for 600 s. (b) Density of detrapped oxide positive charge observed at room temperature as a function of detrapping time τ_r. Zero-field emission of oxide charge was measured (symbols) after CVS at −4.25 V for 600 s at room temperature. Curve is from logarithmic fit.

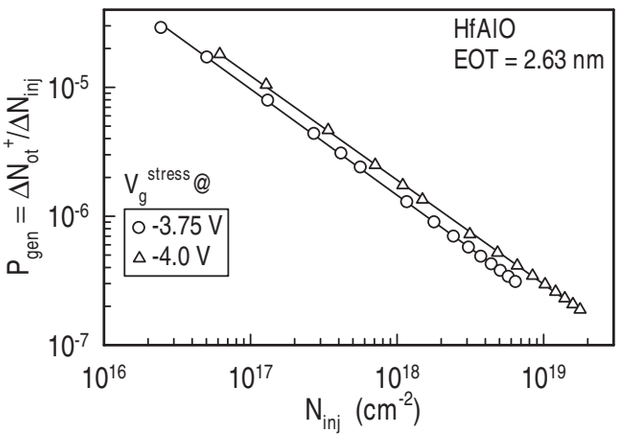

Figure 11. Oxide positive charge trapping probability as a function of number of injected electrons into $HfAlO/SiO_2$ stack during negative-bias CVS with stress voltage as a parameter.

controversy is resolved in this section as follows. Zero-field detrapping of oxide-trapped positive charge is studied, as illustrated in Fig. 10. The straight-line nature of the midgap voltage shift ΔV^{*}_{mg} because of self-detrapping vs logarithmic relaxation time τ_r, as shown in Fig. 10a, indicates the existence of tunnel detrapping[28] of bulk positive oxide charges at room temperature. Tunnel detrapping of proton-induced defects is not physically acceptable, rather it is conformity with holes from as-fabricated traps.[14] Therefore, hole trapping might explain the oxide positive charge buildup in both devices. A plot of the instantaneous zero-field emission rate of N^{+}_{ot} vs reciprocal of detrapping time τ_r yielded a straight line, as evident from Fig. 10b. This means that intrinsic hole traps in the dielectric stacks are uniformly distributed $[D_{ox}(E) = \text{const}]$ in energy[28] in accordance with

$$\frac{dN^{+}_{ot}}{dt} = \frac{k_B T D_{ox}(E)}{t} \qquad [9]$$

where N^{+}_{ot} is the area density of detrapped positive oxide charge with density of states $D_{ox}(E)$ in cm^{-2} eV^{-1}, k_BT is the thermal energy in eV, and t is the detrapping or relaxation time. The constant density of states suggests that the as-fabricated hole traps have a single time constant[28] and therefore can be characterized by a single capture cross section. Our analysis contradicts the observations by Gusev and D'Emic.[29] We explain this in the following way. In their work, the interfacial dielectric was ultrathin silicon oxynitride instead of thermal SiO_2 used in our measurements and the interfacial dielectric plays the role in positive charge and/or hole trapping. Using Eq. 9, the estimated depth of the intrinsic hole traps from the SiO_2 valence bandedge was ≈1.2 eV. This value is close to that reported for intrinsic hole traps in pure SiO_2 devices.[28]

The origin of trapped holes in the dielectric during negative-bias CVS may be either valence band tunneling (VBT)[27,30] or anode hole injection (AHI).[30,31] For the VBT mechanism of holes, the oxide positive charge generation probability $P_{gen} = \Delta N^{+}_{ot}/\Delta N_{inj}$ should not depend on stress voltage. This is because of filling of the preexisting hole traps. P_{gen} is also shown in Fig. 11 as a function of the injected electron density N_{inj} during the negative-bias CVS in both capacitors. As evident in Fig. 11, irrespective of the dielectric stacks, P_{gen} strongly depends on V^{stress}_{g}, which in turn is related to the electron energy reaching the anode. Moreover, for VBT to be a possible mechanism, trapped oxide positive charge buildup should saturate during stress consistent with the filling of pre-existing traps. However, no such saturation in oxide positive charge buildup was observed in either of the devices within the stress time shown in Fig. 6. On the contrary, ΔN^{+}_{ot} monotonically increases with stress time, indicating generation of defects in the dielectric during stress. Therefore, hole trapping via a VBT mechanism during negative-bias CVS seems unlikely in these devices. To model the positive charge buildup in high-κ stacks due to hole trapping, the stretched-exponential $A\{1 - \exp[-(t/\tau)^{\zeta}]\}$ formalism has been made popular by several researchers.[26,27] Stress time dependence of ΔN^{+}_{ot} can be mathematically well reproduced by the stretched exponential with distribution width $\zeta \approx 0.22$, as shown by the filled dots in Fig. 6. However, the stretched-exponential formulation (with $\beta < 1$) is based on the a priori assumption of continuous distribution of capture cross section of the intrinsic hole traps[26,27] contrary to the single time constant, as determined experimentally in Fig. 10b. Furthermore, the distributed capture cross-section model[26] assumes only trap filling without creating additional traps. In view of the above, the distributed capture cross-section model[26,27] is not physically viable to explain the positive charge buildup during CVS in either of the high-κ gate stacks studied here.

Hole trapping into as-fabricated hole traps of single capture cross section obeys the simple charging equation[31] $p(t) = A[1 - \exp(-t/\tau)]$. However, the estimated oxide positive charge density ΔN^{+}_{ot} in either of the devices does not fit with above hole-trapping dynamics, as depicted by the dashed lines in Fig. 6. Rather, $\Delta N^{+}_{ot}(t)$ fits well (the solid lines in Fig. 6) with

$$\Delta N^{+}_{ot} = A[1 - \exp(-t/\tau)] + Bt^{n} \qquad [10]$$

The first term on the right side of Eq. 10 is due to hole trapping in pre-existing neutral traps via AHI, while the second term is due to defect generation. The power-law exponent $n \approx 0.2$ in Eq. 10 reproduces ΔN^{+}_{ot} during CVS, as depicted in Fig. 6. $\delta \approx 0.2$ is consistent with the dispersive transport of proton through the interfacial SiO_2 during negative-bias stress in the stack.[32] Furthermore, the maximum depletion capacitance is observed to decrease during CVS of the capacitors, as depicted in Fig. 12. This decrease can be attributed to the reduction in the density of active boron acceptor impurities in the p-type Si substrate, resulting from the formation of B–H complexes.[33] Such complexes are induced by the transport of hydrogen in the Si substrate, consistent with the picture involving the release of hydrogen during CVS. We therefore propose that bulk oxide positive charges in the HfAlO dielectric stack are attributed to holes and proton-induced defects. However, the contribution of proton-related defects is significantly larger than that of holes in oxide positive charge buildup. Recently, from the bias temperature

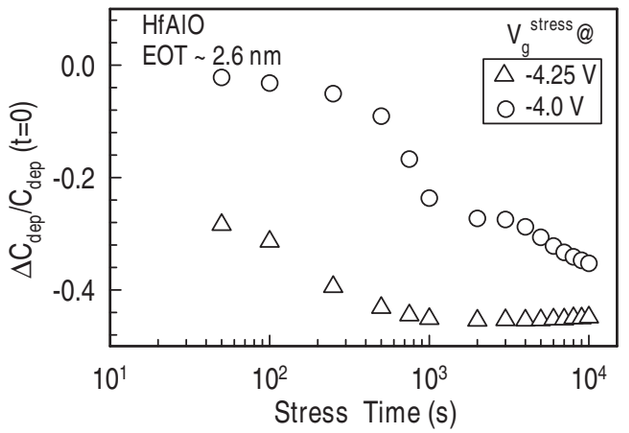

Figure 12. Relative maximum depletion capacitance $[C_{dep} - C_{dep}(0)]/C_{dep}(0)$ of an nMOS capacitor as a function of stress time during CVS.

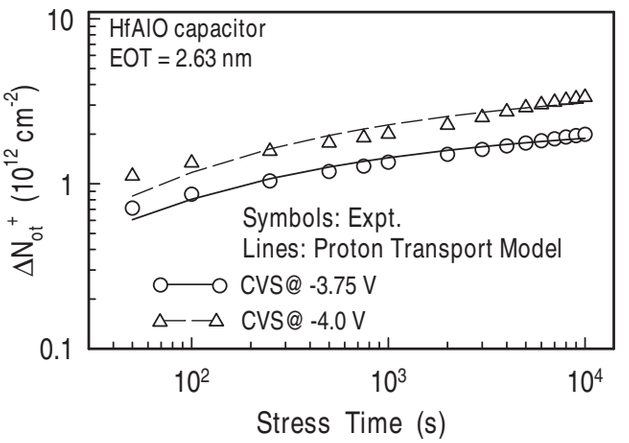

Figure 13. Variation in trapped oxide positive charge density in HfAlO capacitors with stress time during CVS at various voltages. Symbols are from measurements and curves are from dispersive proton transport model.

stress measurements in HfO_2 and SiO_2 devices, we have identified these proton-related defects as the overcoordinated $[Si_2 = OH]^+$ centers.[13] Both ΔN_{ot}^+ and ΔD_{it} follow a t^n ($n \approx 0.2$) power law for both devices (Fig. 6 and 7), indicating the similar generation kinetics for these two types of defects.[14]

Model.— During negative-bias stress, the injected electrons are transported toward the Si/SiO_2 interface (anode) under the electric field in the dielectric stack. These electrons acquiring energy above the threshold energy for the liberation of hydrogen (proton) at the Si/SiO_2 interface depassivate $Si_3 \equiv SiH$ centers, leading to the generation of trivalent $Si_3 \equiv Si^*$ dangling bonds acting as the interface states and the subsequent release of hydrogen (proton).[4] These liberated protons are then accelerated toward the cathode (TaN gate) under the oxide electric field E_{ox}, leading to the breaking of the bridging oxygen bonds and subsequent trapping of H^+ by the strained Si–O–Si bonds[5,13] forming oxide positive charges. A fraction of the liberated hydrogen, while accelerated toward the cathode, generates neutral traps in the high-κ layer.[3-5] In the framework of the dispersive proton transport model,[4,28] one can model positive oxide charge buildup by

$$\Delta N_{ot}^+(t) = N_{oxT}\{1 - \exp[-\sigma(H_{bulk}^+)(t)]\} \quad [11a]$$

$$[H_{bulk}^+] = [H_{int}^+]\left[1 - \int_0^{l(t)} G(y)dy\right] \quad [11b]$$

$$[H_{int}^+] = [Si_3 \equiv SiH][1 - \exp(-\sigma_H^+ N_{inj})] \quad [11c]$$

where N_{oxT} is the total density of strained bonds in the SiO_2 layer, σ is their mean trapping cross section, and $[H_{bulk}^+]$ is the bulk concentration of proton at a time t and is related to the instantaneous hydrogen concentration at the interface $[H_{int}^+]$ by the transport equation (Eq. 11b). $G(y)$ is a trial function related to the probability of finding a proton at a given distance from the interface at a given time t and $\ell(t)$ is related to the dispersiveness of proton transport.[34] $[Si_3 \equiv SiH]$ is the initial concentration of passivated SiH bonds that after depassivation yields H^+ with a liberation cross section σ_{H^+} and N_{inj} is the number of injected electrons per unit area. Figure 13 shows that the above proton transport model can well reproduce the measured density of oxide-trapped positive charges during CVS in HfAlO capacitors.

Comparison between HfAlO and HfO_2 devices.— To compare the carrier trapping related deterioration of the gate stack and device performances, HfAlO and HfO_2 capacitors of equal EOT were used here. The process flow of the HfO_2 devices can be found elsewhere.[35] Al incorporation in HfO_2 introduces more oxide fixed charge and border trap in as-fabricated HfAlO samples when compared with the virgin HfO_2 devices of same EOT (not shown here). Like in HfAlO devices, HfO_2 devices exhibit positive oxide charge trapping during negative-bias CVS. A relative comparison of oxide positive charge buildup rate in both devices is shown in Fig. 14a at various equal stress voltages. The principle of operation of charge trapping memory devices is closely related to the oxide charge buildup in MOS capacitors.[35] Therefore, the larger value of ΔN_{ot}^+ at a given stress voltage, as depicted in Fig. 14a, indicates better performance of charge trapping memory devices with HfAlO dielectric when compared with HfO_2/SiO_2 stack of same EOT. Unlike the variation in ΔN_{ot}^+ with stress time during CVS at an identical V_g^{stress}, the amount of ΔD_{it} is more in HfO_2 capacitors compared to the HfAlO capacitors, as illustrated in Fig. 14b. Nearly an equal number $[(2 - 3) \times 10^{10}\ eV^{-1}\ cm^{-2}]$ of D_{it} was observed in both as-fabricated devices. Results shown in Fig. 14b indicate that addition of Al increases the Si/SiO_2 interface stability in HfAlO devices during CVS. Coulombic scattering due to interface-trapped charges plays a vital role in channel carrier mobility degradation.[36] In view of this, stress-induced channel carrier mobility degradation and

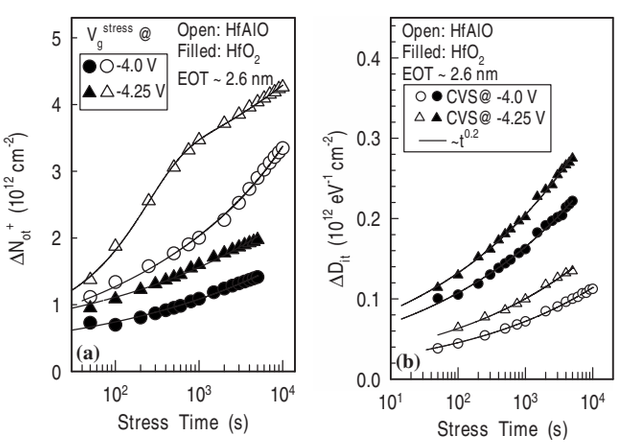

Figure 14. Number of stress-induced (a) positive oxide-trapped charges ΔN_{ot}^+ and (b) interface states ΔD_{it} as a function of stress time in $HfAlO/SiO_2$ (open symbols) and HfO_2/SiO_2 (solid symbols) stacks during CVS. Results are shown relative to the fresh devices.

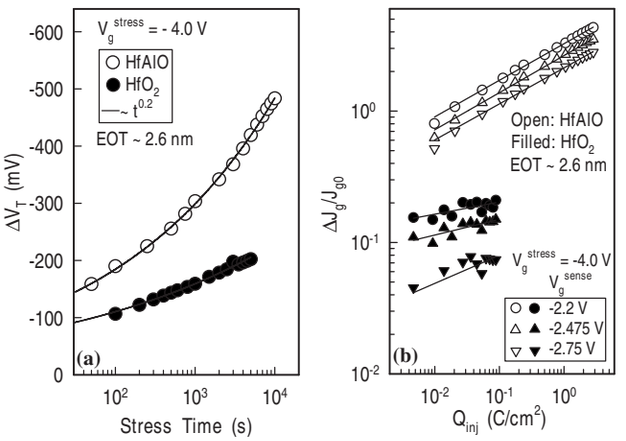

Figure 15. (a) Threshold voltage shift ΔV_T relative to the fresh device as a function of stress time and (b) normalized SILC as a function of injected electron fluence Q_{inj} in $HfAlO/SiO_2$ (open symbols) and HfO_2/SiO_2 (solid symbols) stacks after CVS at −4.0 V with sensing voltage V_g^{sense} as a parameter.

transconductance (g_m) degradation in metal oxide semiconducton field-effect transistor (MOSFETs) with HfAlO gate dielectric are lower than that with HfO_2 of an equal EOT. Similar observations were experimentally observed by Joo et al.[7] in their MOSFET devices.

At a given operating voltage, the higher V_T degradation in HfAlO capacitors, as depicted in Fig. 15a, shortens the device lifetime compared to the devices with HfO_2/SiO_2 stack of same EOT. In other words, for a given projected lifetime within a given tolerance of V_T shift, the operating voltage of the HfAlO devices would be lower than that of the HfO_2 devices with an identical EOT. ΔV_T comprises of ΔN_{ot}^+ and ΔD_{it}.[35] Therefore, comparing the results shown in Fig. 14 and 15a, ΔN_{ot}^+ significantly contributes in V_T degradation. Similar to V_T degradation, SILC degradation in HfAlO devices is also higher than that of HfO_2 devices of equal EOT, as shown in Fig. 15b. It is discussed above that SILC is due to assisted tunneling via neutral traps generated in the high-κ layer during CVS. Therefore, from the results shown in Fig. 15b we propose that at a given V_g^{stress}, the neutral trap creation rate is higher in HfAlO devices relative to the HfO_2 devices of an equal EOT. Neutral electron traps originated from nonbridging oxygen centers.[8] Al acts as a network modifier[6] by breaking of Al–O–Al bonds which produce nonbridging oxygen centers.[8] Therefore, the higher trap creation in HfAlO stack might be due to larger concentration of nonbridging oxygen centers originated from breaking of Al–O–Al bonds compared to Hf–O–Hf bonds. This argument is further supported from the lower bonding energy of the Al–O bonds (~ 118.5 eV)[37] than that of the Hf–O bonds (~ 213.1 eV).[38] Moreover, gate dielectric breakdown occurs due to the formation of conducting path between the electrodes when the neutral trap density reaches a critical value.[21] In view of this, the results shown in Fig. 15b immediately imply that at a given applied voltage, the dielectric breakdown triggered by neutral trap creation is facilitated in HfAlO capacitors relative to the HfO_2 ones of an equal EOT.

Under negative-bias stress, the stress-induced oxide positive charge buildup is closely related to the electric field E_{ox} across the 2 nm thick interfacial SiO_2 layer and the trap creation is related to the electric field in the high-κ layer in either of the capacitors. For a given V_g^{stress}, voltage drop V_{ox} across the interfacial SiO_2 in HfAlO capacitors is higher than that in HfO_2 capacitors, resulting $E_{ox}(HfAlO) > E_{ox}(HfO_2)$. Therefore, the density of ΔN_{ot}^+ is larger in HfAlO capacitors compared to the HfO_2 capacitors, as illustrated in Fig. 14a. For a given V_g^{stress}, voltage drop across the HfAlO layer is approximately equal to voltage drop across the HfO_2 layer, while $E_{HfAlO} > E_{HfO_2}$ because of the larger physical thickness of the HfO_2 layer. Therefore, at a given stress voltage, neutral trap creation rate in the high-κ layer is higher for HfAlO capacitors when compared with HfO_2 capacitors of same EOT.

Conclusions

A systematic experimental investigation on the electrical stress-induced degradation of gate dielectrics and device performances with HfAlO gate dielectric is presented. We propose that dielectric degradation is a composite effect of neutral trap creation, surface-state generation at the Si/SiO_2 interface, and positive charge trapping in the bulk. Significant amount of border-trapped charges was observed in both as-deposited and poststressed devices. Similar kinetics of generation of both oxide-trapped charges and interface-trapped charges was observed. Both these defects are possibly related to hydrogen-related species. Furthermore, the results demonstrate that HfAlO samples are superior to HfO_2 samples of equal EOT in charge trapping memory and CMOS logic applications at the cost of shorter device lifetime and enhanced gate dielectric deterioration due to excess oxide charge buildup and neutral trap creation in HfAlO capacitors at a given V_g^{stress}. The present study gives an important message that bypassing the leakage current benefit due to Al incorporation in HfO_2, a trade-off between the device performance and dielectric degradation assessing the oxide reliability must be made in selecting the appropriate gate stack of a given EOT.

Acknowledgment

P.S. thanks Dr. Souvik Mahapatra at Microelectronics Division, IIT, Bombay, for providing the measurement facilities. The authors thank the National Science Council of Taiwan for the financial support under contract no. NSC 97-2221-E-150-072. Technical support from National Nano Device Laboratories (NDL) of Taiwan is also acknowledged.

National Formosa University assisted in meeting the publication costs of this article.

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