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Thermal stability of polycrystalline silicon electrodes on ZrO_2 gate dielectrics

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Thermal stability of gate stack structures composed of ZrO_2 gate dielectrics and silicon electrodes was investigated. The ZrO_2 films were deposited by atomic layer deposition, while the polycrystalline silicon electrodes were deposited using different variants of chemical (CVD) and physical vapor deposition (PVD). Zirconium silicide formation was noted in all CVD-electroded samples after subsequent annealing treatments at temperatures above 750 °C, but not in the room temperature PVD-electroded samples, even after gate annealing at 1050 °C. The dependence of zirconium silicide formation on the Si deposition process was explained using thermodynamic arguments which explicitly include the effects of oxygen deficiency of the metal oxide films. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1499513]

High-κ metal oxides have been extensively studied as alternative gate dielectric materials to SiO_2 in metal–oxide–semiconductor devices beyond the 100 nm technology node.[1] Because dual metal gate electrode replacements impose additional processing complexities and limitations on operating voltages,[2] conventional polycrystalline silicon (poly-Si) remains an interesting gate electrode material. Recently, HfO_2 has emerged as a promising gate dielectric replacement due to its high dielectric constant and superior thermal stability in contact with Si-based electrodes.[3] Similar stability has been reported for ZrO_2 in certain special cases; for example, with a diffusion barrier between the ZrO_2 and silicon electrode.[4] In this letter, we demonstrate the thermal stability of the $Si/SiO_2/ZrO_2/Si$ system under conventional dopant activation conditions without a barrier layer and show how stability of the poly-Si/ZrO_2 interface depends on the temperature and oxygen activity of the poly-Si growth process.

Uniform ultrathin (~50 Å) zirconium oxide films were deposited on 200 mm p-epi/p^+ silicon test wafers by atomic layer deposition (ALD) at ASM America Inc., using alternating surface-saturating reactions of $ZrCl_4$ and H_2O at 300 °C. The ZrO_2 films in the first two of three test groups were deposited directly onto the original chemical silicon oxide of the as-received wafers. Films in the third test group were deposited onto an ultrathin (~15 Å) SiO_2 film grown by rapid thermal oxidation. The first test group utilized atmospheric chemical vapor deposition (CVD) to grow 1500 Å silicon films on the ZrO_2 films using SiH_4 and H_2 carrier gas (>10 SLM) at 620 °C. Deposition times were approximately 1–2 min. Low-pressure CVD was performed in a vertical furnace for samples in the second test group to deposit 500 Å silicon films using pure SiH_4 or Si_2H_6 at 510 and 440 °C, respectively, at a pressure of a few Torr. Deposition times were 60 to 90 min. Samples from the third test group were capped by 800 Å poly-Si films deposited by room temperature physical vapor deposition (PVD). The sputtering process utilized a lightly boron-doped silicon target and a base pressure of approximately 10^{-7} Torr. Deposition times were several minutes with a 3–4 h pump down period.

After depositing the poly-Si films, the atmospheric CVD samples were annealed in a horizontal furnace using reagent grade N_2 gas. Temperatures ranged from 700 to 1000 °C while dwell times were kept constant at 1 h. Annealing of the low-pressure CVD and PVD samples utilized a rapid thermal annealer (RTA) and reagent grade N_2 gas. Temperatures were varied between 700 and 1050 °C with the dwell times of 5 s to 3 min. Cross sections of the gate stacks were examined by high-resolution transmission electron microscopy (TEM) using a Philips CM20 microscope operating at 200 kV. Crystalline phases within the gate stack were also monitored and indexed by selected area electron diffraction (SAD) of plan view samples.

Figure 1 shows high-resolution cross-sectional TEM images of a $Si/SiO_x/ZrO_2/Si$ gate stack with a top silicon electrode deposited by atmospheric CVD using SiH_4 at 620 °C. Fast Fourier transforms were performed on both cross-sectional micrographs to determine the interplanar spacings of the different polycrystalline regions. The majority of the ZrO_2 film was indexed as tetragonal while a small percentage of the film exhibited diffraction features characteristic of the monoclinic phase. The silicide grains in both images were indexed as the orthorhombic $ZrSi_2$ phase. To analyze a more statistically significant sample area, SAD patterns were recorded using a SAD aperture that included a diffracting area of ~2 μm^2. A representative electron diffraction ring pattern of the as-deposited sample is shown in Fig. 2(a). The only rings not indexed to tetragonal ZrO_2 interplanar spacings were indexed to the $ZrSi_2$ phase. The most intense (131)

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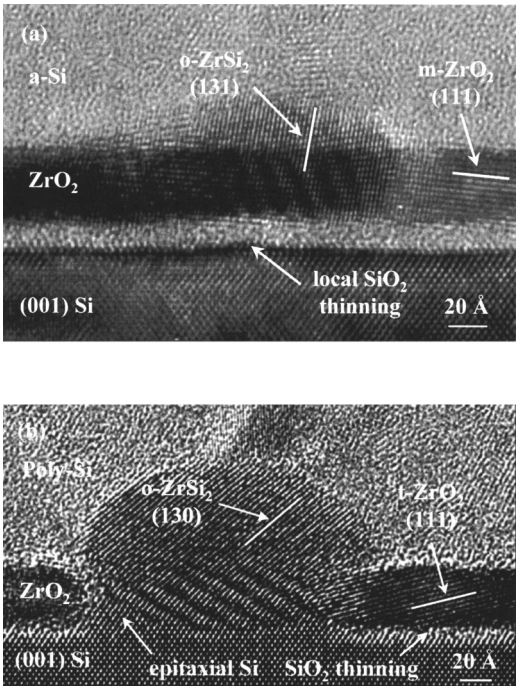

FIG. 1. Cross-sectional TEM images of a $Si/SiO_x/ZrO_2/Si$ gate stack utilizing a 620 °C SiH_4 CVD process (a) as-deposited and (b) after a subsequent 1 h N_2 furnace anneal at 850 °C.

$ZrSi_2$ reflection was used to determine the occurrence of silicide formation in all samples in this study. The cross-sectional micrograph of the as-deposited gate stack also shows a local thinning of the SiO_2-based interfacial layer beneath the silicide grain. The degree of thinning increased and was observed to spread to regions that were not in the immediate vicinity of a silicide particle during the subsequent high-temperature anneal. Epitaxial growth of silicon at the Si (100) wafer interface is also evident in the annealed sample around the sides of the silicide grain in Fig. 1(b), suggesting diffusion of silicon from the decomposing SiO_2 into the Si wafer during the anneal. It should be noted that high temperature N_2 annealing of bare (unelectroded) ZrO_2 films did not result in detectable $ZrSi_2$ formation.

A second set of CVD poly-Si deposition experiments explored the effects of lower thermal budgets and different silicon precursors on $ZrSi_2$ formation. Figure 2(b) is a representative SAD pattern of the as-deposited Si_2H_6 sample. As with the as-deposited low temperature SiH_4 samples, no silicide diffraction signatures were observed; all detected rings were indexed to tetragonal ZrO_2. Cross-sectional TEM images corroborated these results, showing no zirconium silicide particles or detectable thinning of the SiO_2 layer. Upon subsequent annealing, the Si_2H_6 samples exhibited the best thermal stability, as silicide diffraction signatures were not observed below 800 °C. As illustrated in Fig. 3 for a low-temperature SiH_4 sample annealed at 1050 °C, higher temperature post-deposition anneals were again found to significantly thin the interfacial layer and cause silicon to diffuse to the base of the silicide grains.

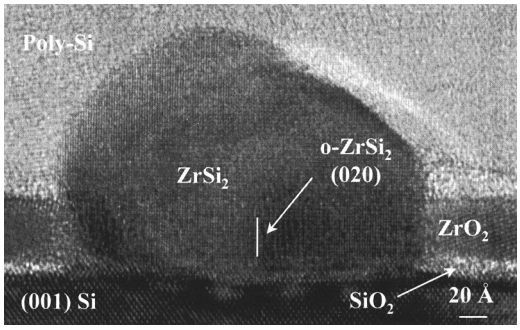

FIG. 3. Cross-sectional TEM micrograph illustrates a $ZrSi_2$ grain in a 510 °C SiH_4 CVD sample after a 1050 °C N_2 anneal.

The extent of silicide growth depended upon the post-electrode annealing temperature. Recent x-ray photoelectron spectroscopy studies reported thermal stability up to 900 °C for the $Si/SiO_2/ZrO_2/Si$ system.[5,6] Because the initial onset of silicidation is a sparse and localized phenomenon, this technique may not be sensitive enough to detect the initial precipitates until their volume fraction in the gate stack reaches a few atomic percent. As a result, the onset of thermal instability in these previous studies[5,6] actually may have occurred at lower temperatures, similar to those reported in this paper.

A third set of samples was fabricated using a room temperature sputtering process to deposit the poly-Si gate electrode (Fig. 4). Unlike the samples made using CVD methods, the PVD material was stable with respect to $ZrSi_2$ formation at temperatures up to those of conventional dopant activation anneals. Thinning of the interfacial layer was observed after the anneal.

Several groups have suggested that the observed silicidation during vacuum annealing of uncapped ZrO_2 films results from SiO evaporation which decomposes the SiO_2 layer and removes oxygen from the ZrO_2.[5,7] Oxygen loss by SiO evaporation is well established for thin SiO_2 films for temperatures between 700 and 1000 °C.[8,9] Reduction of the zirconia films to form oxygen-deficient ZrO_{2-x} by loss of molecular oxygen during the early stages of poly-Si deposition

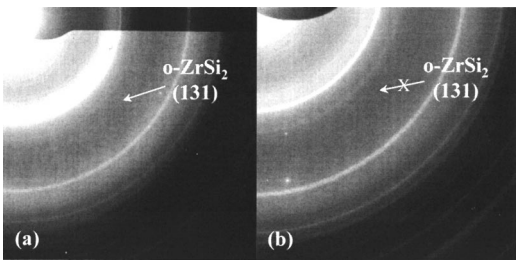

FIG. 2. SAD patterns of as-deposited samples show (a) $ZrSi_2$ diffraction signatures with the 620 °C SiH_4 CVD process and (b) thermal stability of the 510 °C SiH_4 CVD sample.

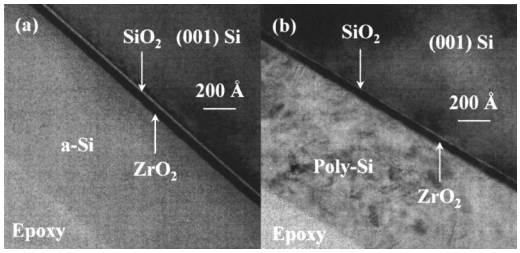

FIG. 4. Cross-sectional TEM micrographs of a $Si/SiO_x/ZrO_2/Si$ gate stack utilizing a room temperature PVD process in both the (a) as-deposited condition and (b) after a 10 s N_2 RTA step at 1050 °C.

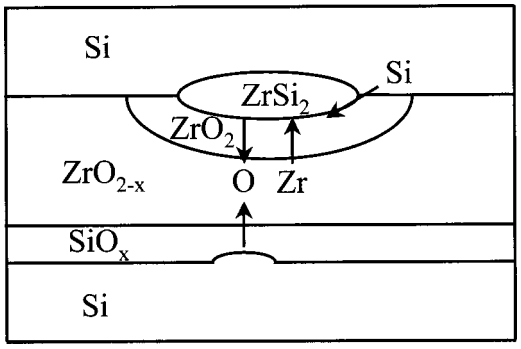

FIG. 5. The proposed process of silicidation involves (1) decomposition of ZrO_2, (2) Zr diffusion and reaction with Si to form $ZrSi_2$, and (3) O diffusion and filling of oxygen vacancies in ZrO_{2-x} regions. Note concurrent O diffusion from the SiO_2 layer.

is also possible. The poly-Si CVD precursor ambients (e.g., H_2/SiH_4) are expected to have extremely low oxygen activity. As a result, it is reasonable that oxygen loss should occur (perhaps involving SiO) during the initial phases of silicon deposition given the tendency of ZrO_2 to become oxygen deficient.[12] In this study, thinning of the interfacial layer was not observed in the lower temperature (440–510 °C) CVD and the PVD samples until after post-electrode annealing. Once a thick Si layer caps the ZrO_2 film, exchange of oxygen between the sample and the ambient is kinetically inhibited. Therefore, continual SiO evaporation[5,7] cannot account for the observed silicidation and SiO_2 thinning during post-electrode anneals.

The elevated temperatures and low oxygen activity of conventional CVD silicon deposition may create oxygen vacancies in the ZrO_2, in addition to oxygen vacancies present in the as-deposited metal oxide films. Reported thermodynamic data suggest that there is a driving force for oxygen exchange between oxygen deficient ZrO_2 and SiO_2 via the following reaction (using Kröger-Vink notation)[12]

$$4e^- + 2V_{\ddot{O}} + SiO_2(s) \rightarrow Si(s) + 2O_O^x,$$

where the individual processes can be thought off as: (1) decomposition of SiO_2 into its elemental constituents and (2) filling of oxygen vacancies in ZrO_2. The enthalpy change of the combined process is predicted to be large and negative (~ -230 kJ/mol).[10,11] As this is a solid state reaction, the entropy change is relatively small and the enthalpy change should accurately represent the total driving force for thinning of the interfacial SiO_2 layer.

We propose that the process of silicidation is also dependent on the oxygen stoichiometry of the ZrO_2 layer after silicon deposition. Oxygen deficiency of the ZrO_2 films may cause $ZrSi_2$ formation to become energetically favorable. This is summarized (see Fig. 5) by the reaction

$$ZrO_2 + 4e^- + 2V_{\ddot{O}} + 2Si(s) \rightarrow ZrSi_2(s) + 2O_O^x,$$

which can be thought of as to the summation of three processes: (1) decomposition of ZrO_2 into its elemental constituents, (2) reaction between the resulting metallic Zr and Si to form $ZrSi_2$, and (3) filling of two oxygen vacancies in a nonstoichiometric area of the ZrO_2 film. The enthalpy change of the combined process is also large and negative (~ -190 kJ/mol),[10–12] indicating a large driving force for zirconium silicide formation from oxygen deficient ZrO_2 via this solid state reaction.

Although the predicted driving forces for SiO_2 decomposition and $ZrSi_2$ formation at the ZrO_{2-x}/SiO_{2-x} and Si/ZrO_{2-x} interfaces, respectively, are not dissimilar, our annealing experiments on PVD poly-Si electroded samples showed a complete absence of silicidation but a detectable SiO_2 thinning. This suggests that the ALD ZrO_2 films were somewhat oxygen deficient as-deposited and that the PVD poly-Si deposition process did not add to this initial oxygen nonstoichiometry. Furthermore, one expects a substantial kinetic barrier to nucleation of the silicide particles associated with formation of $Si/ZrSi_2$ and $ZrSi_2/ZrO_2$ interfaces. No new interfaces are needed for SiO_2 thinning to take place. The elevated temperature of the CVD processes may promote formation of $ZrSi_2$ nuclei at the poly-Si/ZrO_2 interface. These nuclei would then grow during post-electrode anneals, consistent with the observed particle formation during annealing of the CVD samples.

In summary, we have demonstrated a correlation between poly-Si gate electrode deposition conditions and the silicidation of ZrO_2 gate dielectrics, whereby high deposition temperatures and reducing CVD ambients encourage formation of $ZrSi_2$ particles. We have also shown that $ZrSi_2$ formation occurs during postelectrode annealing of ZrO_2 samples that are capped by a thick, continuous poly-Si electrode layer, when the electrode deposition occurs under typical CVD conditions. These results are consistent with thermodynamically favored processes in which oxygen vacancies present in the ZrO_2 dielectric are annihilated through SiO_2 decomposition and $ZrSi_2$ formation.

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