Journal of The Electrochemical Society, **151** (12) F283-F287 (2004)
0013-4651/2004/151(12)/F283/5/$7.00 © The Electrochemical Society, Inc.

Evaluation of Thermal Stability for CMOS Gate Metal Materials

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We present an evaluation of the thermal stability for various elemental metals and binary/ternary conducting compounds on gate dielectrics. The continued scaling of polysilicon gated complementary metal oxide semiconductor (CMOS) devices may face limitations such as polydepletion, incompatibility with some high-*k* dielectrics, high series resistance, and boron penetration. In this study, 24 different elemental metals and metallic compounds with work functions ranging from 4.0 to 5.2 eV covering n-type field effect transistor (nFET), midgap, and pFET gate electrodes were examined. The films were characterized during rapid thermal annealing in a forming gas ambient up to 1000°C. Three techniques, *in situ* X-ray diffraction, resistance, and elastic light scattering analysis were used simultaneously during annealing. It was found that many of the elemental materials, especially those with nFET work functions, undergo reactions with the SiO_2 and Al_2O_3 gate dielectrics, while others became unstable because of melting (Al) or agglomeration (Co, Ni, Pd and $CoSi_2$). Two binary compounds, W_2N and RuO_2, underwent dissociation in the hydrogen-containing ambient. Materials stable above 700°C include Mo, W, Re, Ru, Co, Rh, Ir, Pd, Pt, W_2N, TaN, TaSiN, and $CoSi_2$, making them possible choices for integration involving higher temperature processing.
 [DOI: 10.1149/1.1811592]

Manuscript submitted January 9, 2004; revised manuscript received May 12, 2004. Available electronically October 28, 2004.

Continued scaling of the gate length and gate oxide thickness of complementary metal oxide semiconductor (CMOS) transistors for higher performance and increased circuit density has reached a point where a number of issues have arisen. The potentially major issues include high gate tunneling leakage current,[1,2] polysilicon (poly-Si) gate depletion,[3] high gate resistance,[3] boron diffusion into the dielectric for pFETs,[4] poly-Si incompatibility with some high-*k* dielectrics,[5] and reliability.

Many of these issues may be lessened or eliminated by replacing the poly-Si gate with a metal gate. Current state-of-the-art ultrathin gate oxynitride dielectrics show a continued increase in leakage current even though additional nitrogen incorporation has mitigated this to some extent.[6] Thinning the gate oxide further may not be practical, but there is an additional way to decrease the electrical thickness and thus increase CMOS performance. Three components make up the electrical thickness (capacitance) of the gate stack: the contribution from the Si substrate (due to the quantum mechanical effect), the dielectric layer itself, and the carrier depletion layer in the poly-Si formed when the field effect transistor (FET) device is turned on.[7] Replacement of the poly-Si gate with a metal gate eliminates the depletion and thus decreases the electrical thickness by the SiO_2 equivalent of 0.3-0.5 nm, without a substantial increase in leakage.[3] This also decreases the gate resistivity (the decrease depends on the choice of material) from that of 1-3 m Ω cm typical for the doped poly-Si.[8] For example, a $CoSi_2$ gate has a resistivity of 15-20 μΩ cm, about two orders of magnitude less than that of doped poly-Si.[9] Without boron-doped poly-Si we have an additional advantage because there is no longer a concern about boron penetration into the dielectric. Likewise, without poly-Si on the gate, there is no longer a concern about a poly-Si interaction with high-*k* materials.

There are many advantages to the implementation of metal gates. The choice of material depends on several criteria. The most important property, the work function, is defined as the energy needed to remove an electron from the Fermi level to the vacuum level. As with poly-Si it is necessary to have an nFET metal material with a work function from 4.1-4.3 eV and a pFET material with a work function from 5.0 to 5.2 eV, both about 0.2 eV from the Si bandedges.[10] For some specific device designs (like FinFET or FDSOI) a midgap, 4.6-4.8 eV, work function metal gate material may be appropriate.[11]

The metal gate material then must be stable in contact with the dielectric at temperatures relevant to CMOS processing. The processing temperatures depend on the integration scheme used to implement the gate metal material. A "gate last" integration scheme would be the least aggressive with maximum processing temperatures of less than 600°C,[12] whereas a conventional integration scheme would be the most aggressive because the gate would be in place during the 1000°C several second anneal to activate the dopants in the source/drain regions. Other important criteria in the choice of a gate metal material include the ease of hydrogen diffusion through the material for dielectric interface passivation[13,14] and the deposition method. In order to minimize damage to the gate dielectric, a plasma-free deposition process like chemical vapor deposition (CVD), atomic layer deposition (ALD), or thermal deposition is preferred.[15,16]

In this paper we have investigated the thermal stability of 24 different metal gate materials deposited on SiO_2 and Al_2O_3 dielectrics. Anneals were completed at a constant ramp rate of 3°C/s up to 1000°C in forming gas, while *in situ* X-ray diffraction (XRD), elastic light scattering, and sheet resistance measurements were performed. From this analysis we determined the temperature at which the material thermally degrades and hence, the appropriate CMOS integration scheme. Materials stable above 700°C include Mo, W, Re, Ru, Co, Rh, Ir, Pd, Pt, W_2N, TaN, TaSiN, and $CoSi_2$, making them possible choices for integration involving higher temperature processing.

Experimental

Metal gate films for this study were deposited by both physical vapor deposition (PVD) and CVD methods. The materials studied, deposition method, and thickness/composition as determined by Rutherford backscattering (RBS) analysis are shown in Table I. The majority of the films are single-component materials, 24-37 nm thick, sputter deposited from 7.6 cm diam targets using magnetron sputtering sources in an ultrahigh vacuum (UHV) deposition system. The films were deposited at target power levels ranging from 200 to 600 W (direct current) with an argon deposition pressure of 4 mTorr and system vacuum base pressures of 5.0-9.0 $\times$ 10^{-10} Torr. Several of the films were reactively sputter deposited in the same system in

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Table I. Evaluated metal gate materials.

Gate metal material	Deposition method	Thickness (nm)
Titanium	PVD sputtering	33 nm Ti (20% O)
Zirconium	PVD sputtering	33 nm Zr (34% O)
Hafnium	PVD sputtering	37 nm Hf (25% O)
Vanadium	PVD sputtering	39 nm V (16% O)
Niobium	PVD sputtering	30 nm Nb (14% O)
Molybdenum	PVD sputtering	32 nm Mo (11% O)
Tantalum	PVD sputtering	25 nm Ta (10% O)
Tungsten	PVD sputtering	31 nm W (2% O)
Manganese	PVD sputtering	33 nm Mn (30% O)
Rhenium	PVD sputtering	31 nm Re (2% O)
Ruthenium	PVD sputtering	33 nm Ru (3% O)
Cobalt	PVD sputtering	30 nm Co (7% O)
Rhodium	PVD sputtering	31 nm Rh (0.8% O)
Iridium	PVD sputtering	32 nm Ir (0% O)
Nickel	PVD sputtering	27 nm Ni (4% O)
Palladium	PVD sputtering	33 nm Pd (0% O)
Platinum	PVD sputtering	29 nm Pt (0% O)
Aluminum	PVD sputtering	24 nm Al (27% O)
Tungsten two nitrogen	CVD $W(CO)_6 + NH_3$	25 nm W:N:C:O-58:36:5:1
Tantalum two nitrogen	CVD $TaF_5 + NH_3$	39 nm Ta:N:F-71:28:0.6
Tantalum nitride	PVD reactive sputtering	38 nm Ta:N:O-42:51:7
Tantalum silicon nitride	PVD reactive sputtering	50-55 nm Ta:Si:N:O (23-37):(14-39):(35-52):4
Ruthenium dioxide	PVD reactive sputtering	195 nm Ru:O-33:67
Cobalt disilicide	PVD sputtering/ salicide	77 nm Co:Si-33:67

the presence of 2-10% N_2 (38 nm TaN, 50-55 nm TaSiN) or 2% O_2 (195 nm RuO_2) with Ar, for a total deposition gas pressure of 4 mTorr. For the deposition of the TaSiN film, Ta and Si were codeposited in the presence of N_2. The 77 nm $CoSi_2$ film was formed by sputter depositing 22 nm of Co on 80 nm of low-pressure chemical vapor deposited (LPCVD) polycrystalline Si and annealing the film in forming gas (FG) to form the $CoSi_2$ phase. Thermal CVD was used to deposit two of the films. A 25 nm W_2N film was deposited using a $W(CO)_6$ precursor in the presence of NH_3, whereas a 39 nm Ta_2N film was deposited using a TaF_5 precursor also in the presence of NH_3.

RBS analysis was used to determine the level of impurities in the films by depositing the material on carbon substrates. The most prevalent contaminant in all the films, as determined by RBS analysis, is oxygen. In the thin, highly reactive films, like Ti, the oxygen is not uniformly distributed throughout the film but rather peaks at the surface due to air exposure over a period of days, making the overall level high. The CVD films show low levels of either carbon (W_2N-5 atom % C) or fluorine (Ta_2N-0.6 atom % F) contaminants arising from the precursors used. It is understood that impurities can effect thin-film properties like resistivity, stress, thermal stability, and work function.

The metal gate materials were evaluated on two dielectrics, SiO_2 and Al_2O_3. In order to amplify the effects of an interaction between the gate metal and dielectric, for *in situ* evaluation, the dielectrics were thick. It is expected that the interactions between the metal gate materials and thinner dielectrics are similar. The SiO_2 was grown by thermal annealing to a thickness of 500 nm. The 300 nm thick Al_2O_3 was sputter deposited in a high-vacuum (HV) magnetron system with a base vacuum pressure of 2×10^{-7} Torr from an Al_2O_3 target using a power density of 3.3 W/cm^2 and a total pressure of 10 mTorr ($Ar + O_2$) in the presence of 6% O_2. The interactions of the dielectric materials with the gate metal materials, described previously, were studied using three different *in situ* techniques, conducted simultaneously, while the samples were annealed in FG at a temperature ramp rate of 3°C/s from 100 to 1000°C. The analysis was completed at the National Synchrotron Light Source, Brookhaven National Laboratory, on beamline X20C.[17] The first technique, XRD, consists of passing the incident X-ray beam through a wide-bandpass, artificial multilayer monochromator for an energy resolution of 1.5% at 6.9 keV ($\lambda = 0.1797$ nm) with an approximate flux of 1×10^{13} photons/s. A set of beam-defining slits provides an X-ray spot size of 2×2 mm on the sample surface. The trade-off of maximum X-ray flux for bandpass leads to peaks that are 1-1.5° in width. Geometric considerations lead to peak location accuracy of $\pm 0.3°$ in 2θ. As the samples are annealed, the diffracted X-ray intensity is monitored using a linear position-sensitive detector. The detector covers a 2θ range of $\sim 10°$, from which data is collected every 0.5 s (1.5°C). The 2θ range was chosen such that the main diffraction peaks from the material under study were present. Temperature was monitored using a k-type thermocouple, which was calibrated using eutectic melting points of Au, Ag, and Al in contact with Si for an accuracy of ± 3°C.

The second *in situ* technique, elastic light scattering, consists of using a HeNe laser to determine changes in sample surface roughness or index of refraction. A HeNe laser beam is brought into the annealing chamber through a fiber optic cable and is then focused through a lens onto the sample surface at an incidence angle of 65°, forming a spot size of 1×2 mm. The scattered intensities are measured using two bare fibers positioned at 50° and $-20°$ allowing for measurement of roughness on lateral length scales of approximately 5 and 0.5 μm, respectively. For detection of only the HeNe light scattered from the sample surface, a chopper and lock-in amplifiers are used with Si photodiodes and interference filters, which remove background light at other wavelengths during the high-temperature anneal. This optical scattering technique detects changes in scattered intensity from surface roughness and also changes in index of refraction that a reaction between the gate metal and dielectric may cause.

The last technique, *in situ* sheet resistance, is a four-point probe measurement as a function of temperature. Four spring-loaded Ta probes arranged in an approximate square geometry maintain contact with the sample surface while 25 mA of current passes through two of the probes, and voltage is measured across the other two. This allows for a relative sheet resistance measurement, which may be scaled using a room-temperature absolute measurement made with fixed in-line four-point probe geometry.

The procedure used for annealing the samples during the *in situ* measurements is as follows. The approximately 1.5 cm^2 sample, held in place by the Ta probes, makes contact with a molybdenum block which in turn contacts a pyrolytic boron nitride, resistive heater. It is annealed at a constant heating rate of 3°C/s from 100 to 1000°C. Readying the sample for analysis consists of evacuating the analysis chamber twice ($< 5 \times 10^{-6}$ Torr) and backfilling with FG (FG-95% N_2 and 5% H_2) to a pressure slightly more than atmospheric at a flow rate of 1 L/min. The FG has a purity of 99.999%. Several anneals were conducted in 99.999% pure He to compare the effects of either H_2 and/or N_2 during the anneal treatment.

Results and Discussion

The methods described, *in situ* XRD, optical scattering, and sheet resistance analysis, were used to investigate the thermal stability of 24 gate metal materials in contact with the SiO_2 dielectric.[18] Figure 1 summarizes the thermal stability of the materials using a periodic table representation. The work functions (WFs) of the materials in bulk form, as determined by internal photoemission, are also shown.[19] Each highlighted material has a superscript indicating the type of the work function: "n" nFET $<$ 4.6 eV, "m" midgap 4.6-4.8 eV, and "p" pFET $>$ 4.8 eV. The thermal stability of each material is indicated by the crosshatched pattern. The materials are separated into two groups, those materials stable at temperatures less than 700°C indicated by the vertical stripes and those materials

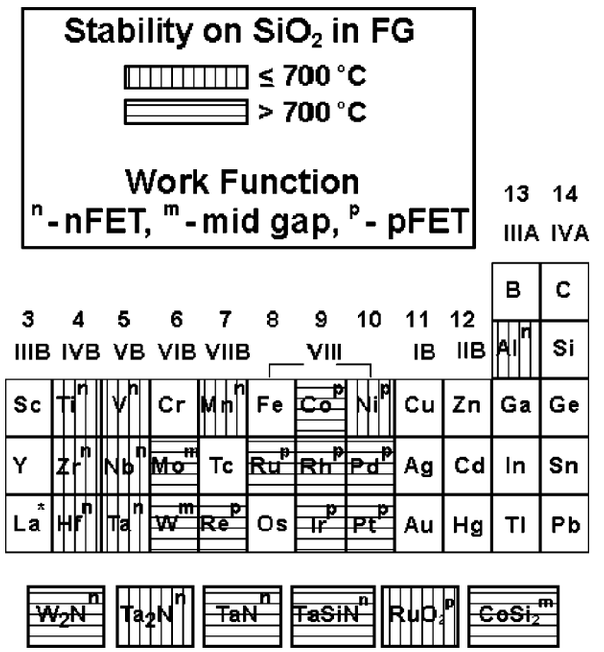

Figure 1. Periodic table indicating the thermal stability of 18 elemental metals and 6 metallic compounds on SiO_2 evaluated using *in situ* XRD, resistance, and optical scattering analysis techniques. Superscripts just after the chemical symbols indicate the type of WF, ^{n}—nFET, ^{m}—mid gap, and ^{p}—pFET. The stripe pattern indicates whether the thermal stability is less than (vertical stripe pattern) or greater than (horizontal stripe pattern) 700°C.

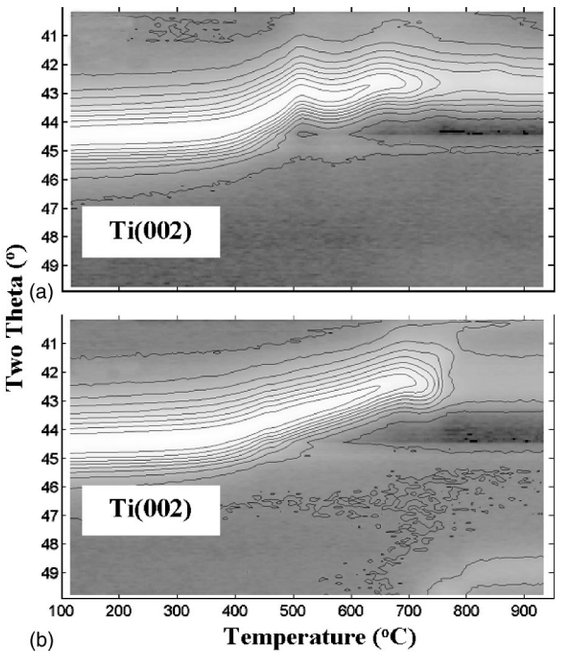

Figure 2. *In situ* XRD contour plots showing diffraction angle (2θ) as a function of temperature (°C) for a 30 nm sputtered Ti film on SiO_2 annealed at a heating ramp rate of 3°C/s up to 1000°C in a (a) forming gas ambient and (b) He ambient. X-ray intensity is indicated by a gray scale with white as the highest intensity and black the lowest.

stable above 700°C indicated by the horizontal stripes. A material is considered not thermally stable if the *in situ* XRD analysis shows a deviation from the typical linear decrease in diffraction angle (2θ) as a function of temperature. The decrease in diffraction angle is a result of the lattice expansion with increased temperature. If the sheet resistance shows a deviation from the typical linear increase as a function of temperature (this linear increase is due to increased phonon vibrations at higher temperatures) or the optical scattering shows a large increase indicating roughening or agglomeration, the material is also considered thermally unstable. As shown in the periodic table of Fig. 1, all the single-component elemental materials with nFET WFs are thermally unstable above 700°C. These materials (columns IVB and VB of the periodic table) tend to react with the dielectric, making it necessary to consider binary or ternary conducting compounds. Such nFET compounds which are stable above 700°C include W_2N, TaN, and TaSiN. There are several thermally stable single elemental component materials with pFET WFs. These pFET materials stable above 700°C include Re, Ru, Co, Rh, Ir, Pd, and Pt.

As a first example of using the *in situ* XRD technique to determine thermal stability, a 33 nm Ti film deposited on a 500 nm SiO_2 film annealed at 3°C/s to 1000°C in FG and He is shown in Fig. 2. 2θ diffraction angle and X-ray intensity is plotted as a function of temperature with intensity indicated by a gray scale and contour lines. Figure 2a shows the anneal completed in an FG ambient were the 2θ decrease in the Ti(002) peak as a function of temperature deviates from linearity at about 400°C. This deviation could be caused by the reaction of the Ti with the underlying SiO_2, the reaction with the N_2 in the FG, or the diffusion of oxygen from the surface of the Ti film to the interior. To eliminate the possible effect of N_2, the film was annealed again using the same thermal treatment in an inert He ambient, shown in Fig. 2b. The deviation from linearity at ~400°C was still present. Electrical and X-ray reflectivity measurements have substantiated that the Ti does react with SiO_2 at 400°C, as indicated here by *in situ* XRD analysis. In summary, Ti is not an adequate choice for a metal gate material because even in the lower temperature ''gate last'' process the thermal stability is insufficient.

In a second example, shown in Fig. 3, a 195 nm RuO_2 film was deposited on the 500 nm thermal SiO_2. Figure 3a shows an anneal of the film at 3°C/s to 1000°C in an FG ambient while *in situ* XRD was monitored. The X-ray contour plot shows the disappearance of the RuO_2(110) diffraction line at approximately 150°C. To determine the role of H_2 in the FG ambient on the dissociation of the RuO_2 film, a second anneal was performed in a He ambient, shown in Fig. 3b. The film likewise dissociated in He but the temperature stability of the RuO_2(110) was substantially higher, up to approximately 870°C. Because the passivation anneal of any gate dielectric must be completed in a H_2-containing ambient, the dissociation of RuO_2 at ~150°C makes it an unacceptable gate metal choice even for the ''gate last'' process. A better choice is W_2N that was found to dissociate in an FG ambient at temperatures above 700°C.

As a last example, a 29 nm Pt film was deposited on SiO_2 and annealed to 1000°C in FG while being monitored using the *in situ* techniques. Results are presented in Fig. 4. Figure 4a shows *in situ* normalized optical scattering (0.5 and 5 μm length scales) and normalized sheet resistance as a function of temperature. The optical scattering indicates no substantial roughening because only the background noise is evident. Typical roughening observed for thermal degradation of other films shows increases of 1000 times. The resistance curve deviates from linearity at about 300°C. The decrease/flattening of the curve indicates that the film may be undergoing grain growth.

The *in situ* XRD contour plot, shown in Fig. 4b, indicates the expected linear decrease with 2θ for the Pt(111) peak with an increase in intensity as temperature increases. This increase in intensity is also an indication that the film may be undergoing grain growth. From the three techniques there is no indication that the film is unstable up to 1000°C, making Pt a viable metal gate material even in a conventional CMOS integration scheme.

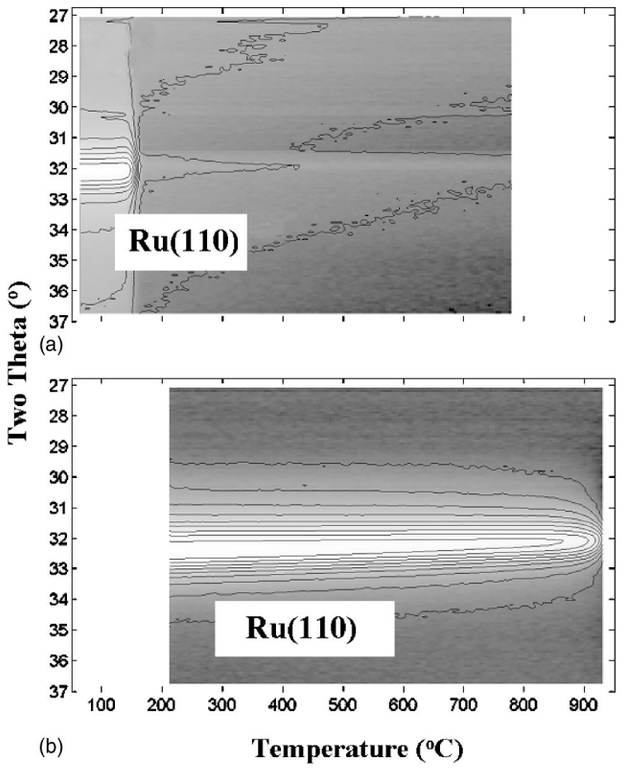

Figure 3. *In situ* XRD contour plots showing diffraction angle (2θ) as a function of temperature (°C) for a 30 nm sputtered RuO_2 film on SiO_2 annealed at a heating ramp rate of 3°C/s up to 1000°C in (a) FG ambient and (b) He ambient. X-ray intensity is indicated by a gray scale with white as the highest intensity and black the lowest.

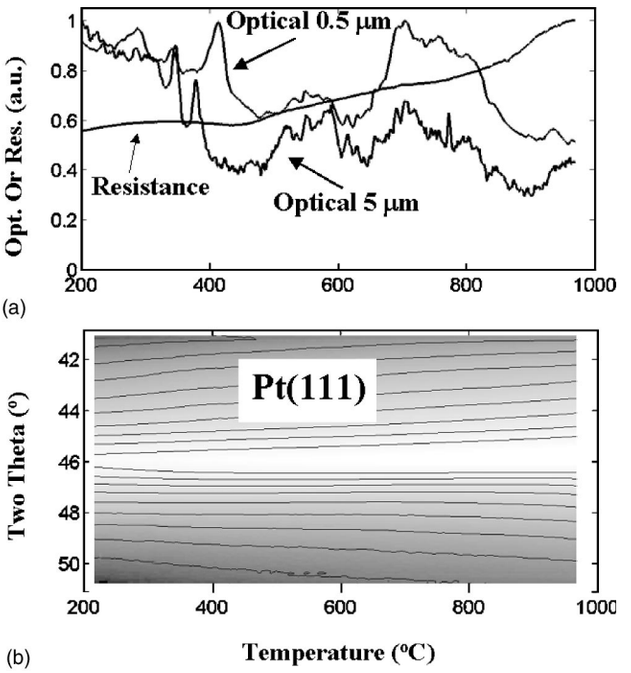

Figure 4. (a) *In situ* resistance and optical scattering plot showing normalized sheet resistance and optical scattered intensity as a function of temperature (°C) for a 30 nm sputtered Pt film on SiO_2. The film was annealed at a heating ramp rate of 3°C/s up to 1000°C in an FG ambient. (b) XRD contour plot showing diffraction angle (2θ) as a function of temperature (°C) run simultaneously. XRD intensity is indicated by a gray scale with white as the highest intensity and black the lowest.

The thermal stability of 18 gate metal materials in contact with an Al_2O_3 dielectric was also investigated. Figure 5 summarizes the thermal stability of the materials using a periodic table representation. Each highlighted material has a superscript indicating the type of WF: "n" nFET $<$ 4.6 eV, "m" midgap 4.6-4.8 eV, and "p" pFET $>$ 4.8 eV. The thermal stability of each material is again indicated by the crosshatched pattern. The materials are separated into two groups, those materials stable at temperatures less than 700°C indicated by the vertical stripes and those materials stable above 700°C indicated by the horizontal stripes. The same criteria as used to determine thermal stability on SiO_2 were used here. As shown in the periodic table, all of the single-component elemental materials with nFET WFs are not thermally stable above 700°C. As on SiO_2, these materials tend to react with Al_2O_3, making it necessary to consider binary or ternary conducting compounds. There are several thermally stable single elemental component materials with pFET WFs. These pFET materials stable above 700°C include Re, Ru, Co, Rh, Ir, Ni, Pd, and Pt.

Theoretically the stability of the various gate metal materials can be determined by considering enthalpies of formation for their oxides and their melting points. A comparison between the enthalpies of formation for the most stable metal oxides (per mole of oxygen), for the gate metal materials evaluated, is shown in Fig. 6. The SiO_2 and Al_2O_3 dielectric enthalpies of formation are also indicated within ranges of ±10%. This is a first-order comparison because if a reaction does occur a simple binary oxide compound may not form but rather a ternary oxide may result. The gate metals that are thermodynamically unstable on SiO_2, having enthalpies within the SiO_2 range indicated, include Ti, Zr, Hf, V, Nb, and Ta. Experimentally these metal gate materials were shown to interact with SiO_2 (Fig. 1). Those materials that are thermodynamically and experimentally (Fig. 5) unstable on Al_2O_3 are Ti, Zr, and Hf.

The melting points of the various gate metal materials studied are shown in Fig. 7. For a conventional CMOS process these materials

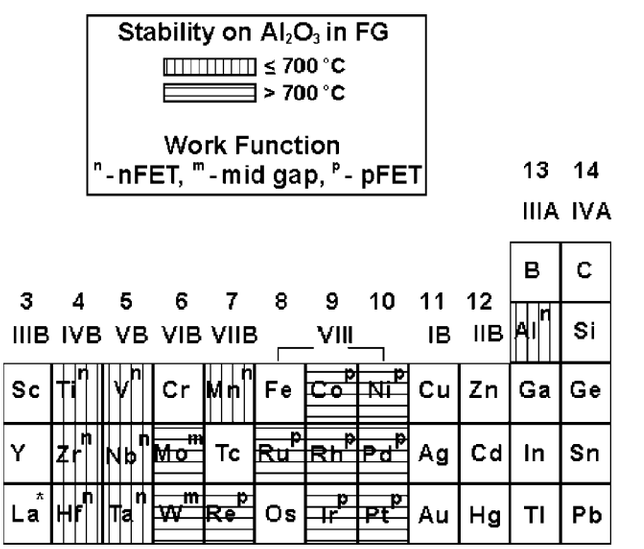

Figure 5. Periodic table indicating the thermal stability of 18 elemental metals on Al_2O_3 evaluated using *in situ* XRD, resistance, and optical scattering analysis techniques. Superscripts just after the chemical symbols indicate the type of WF, ^{n}—nFET, ^{m}—mid gap, and ^{p}—pFET. The stripe pattern indicates whether the thermal stability is less than (vertical stripe pattern) or greater than (horizontal stripe pattern) 700°C.

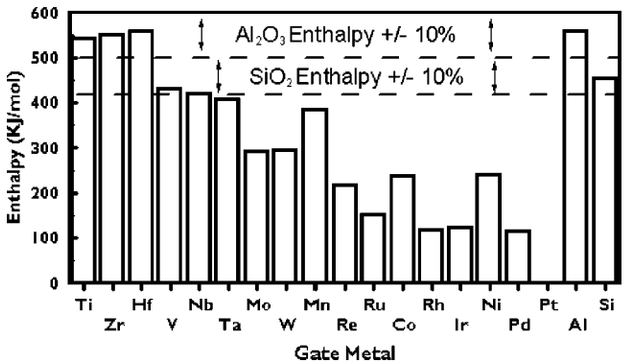

Figure 6. Enthalpies per mole of oxygen for the most stable oxides for seventeen gate metal materials. Ranges (±10%) for the enthalpies of SiO_2 and Al_2O_3 are indicated for comparison.

would have to withstand 1000°C, several second anneals on the dielectrics during the S/D dopant activation. At such high processing temperatures the materials can agglomerate. Agglomeration occurs when grain boundary energies overcome surface or interface energies, leading to roughening of the thin films. It can be decreased by keeping the grains small (lower processing temperatures), increasing the film thickness, decreasing grain boundary energies (adding impurities), or increasing surface and/or interface energies with respect to grain boundary energies, thus reducing diffusivities (adding a capping layer).[20] Agglomeration of the materials can be expected if the homologous temperature (anneal temperature divided by the melting point) gets close to 2/3. Therefore, those materials with melting points less than about 1500°C can be expected to be thermally unstable during the 1000°C activation anneal. The thermally unstable materials include Mn, Co, Ni, and Al (melting point of 660°C). Experimentally (Fig. 1 and 5), Mn and Al are indeed thermally unstable, with Co and Ni being on the edge (Ni on SiO_2 was unstable).

Combining the enthalpy data from Fig. 6 and the melting point data from Fig. 7, the most stable gate metal materials can be determined. The most stable gate metal materials are expected to be Mo, W, Re, Ru, Rh, Ir, Pd, and Pt. The *in situ* analysis techniques employed in this study showed the previously listed metal materials to be stable on SiO_2 and Al_2O_3 dielectrics. These stable materials can now be integrated into capacitor or FET structures for electrical evaluation, which is more sensitive to interface interactions involving several monolayers of material or the formation of amorphous materials.

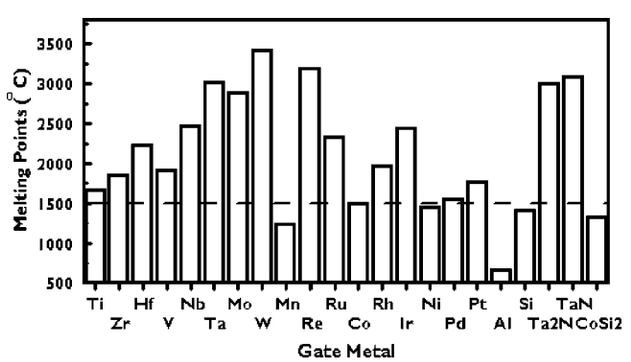

Figure 7. Melting points (°C) for 17 elemental gate metal materials, Ta_2N, TaN, and $CoSi_2$.

Conclusion

We have evaluated the thermal stability of 24 different elemental metals and binary/ternary conducting compounds on SiO_2 and Al_2O_3 gate dielectrics. The motivation for the study was to determine the appropriate integration scheme for each material. This integration scheme dictates the maximum processing temperature for the gate metal material. It was found that many of the elemental materials, especially those with nFET WFs, undergo reactions with the SiO_2 and Al_2O_3 gate dielectrics while others became unstable because of melting (Al) or agglomeration (Co, Ni, Pd, and $CoSi_2$). Two binary compounds, W_2N and RuO_2, underwent dissociation in the hydrogen-containing ambient. Materials stable above 700°C include Mo, W, Re, Ru, Co, Rh, Ir, Pd, Pt, W_2N, TaN, TaSiN, and $CoSi_2$, making them possible choices for integration involving higher temperature processing.

Acknowledgments

The authors thank R. A. Carruthers for thin-film sputter depositions, H. Kim for CVD W_2N depositions, E. T. Eisenbraun for CVD Ta_2N depositions, and A. Kellock for RBS. The work completed at the National Synchrotron Light Source, Brookhaven National Laboratory, was conducted under DOE contract DE-AC02-76CH-00016.

IBM T. J. Watson Research Center assisted in meeting the publication costs of this article.

References

1. G. D. Wilk, R. M. Wallace, and J. M. Anthony, *J. Appl. Phys.*, **89**, 5243 (2001).
2. D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, *Nature (London)*, **399**, 758 (1999).
3. International Technology Roadmap for Semiconductors 2002 Update, 2001 ed., ITRS Home Page, http:/public.itrs.net/files/2002update/2002update.pdf
4. D.-G. Park, H.-J. Cho, I.-S. Yeo, J.-S. Roh, and J.-M. Hwang, *Appl. Phys. Lett.*, **77**, 2207 (2000).
5. C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.*, **2000**, 27.
6. M. L. Green, E. P. Gusev, R. Degraeve, and E. L. Garfunkel, *J. Appl. Phys.*, **90**, 2057 (2001).
7. R. Rios and N. D. Arora, *Tech. Dig. - Int. Electron Devices Meet.*, **1994**, 613.
8. W. R. Thurber, R. L. Mattis, and Y. M. Liu, National Bureau of Standards Special Publication 400-464, p. 42 (1981).
9. K. Maex and M. Van Rossum, *Properties of Metal Silicides*, p. 192, Inspec, London (1995).
10. I. De, D. Johri, A. Srivastava, and C. M. Osburn, *Solid-State Electron.*, **44**, 1077 (2000).
11. S. Murtaza, J. Hu, S. Unnikrishnan, M. Rodder, and I.-C. Chen, *Proc. SPIE*, **3506**, 49 (1998).
12. A. Chatterjee, R. Chapman, K. Joyner, M. Otobe, S. Hattangady, M. Bevan, G. Brown, H. Yang, Q. He, D. Rogers, S. Fang, R. Kraft, A. Rotondaro, M. Terry, K. Brennan, S. Aur, J. C. Hu, H. Tsai, P. Jones, G. Wilk, M. Aoki, M. Rodder, and I. Chen, *Tech. Dig. - Int. Electron Devices Meet.*, **1998**, 777.
13. E. Cartier, J. H. Stathis, and D. A. Buchanan, *Appl. Phys. Lett.*, **63**, 1510 (1993).
14. J. H. Stathis, D. A. Buchanan, D. L. Quinlan, and A. H. Parsons, *Appl. Phys. Lett.*, **62**, 2682 (1993).
15. D. A. Buchanan and G. Fortuno-Wiltshire, *J. Vac. Sci. Technol. A*, **9**, 804 (1991).
16. N. A. Bojarczuk, *J. Vac. Sci. Technol.*, **18**, 890 (1981).
17. G. B. Stephenson, K. F. Ludwig, Jr., J. L. Jordan-Sweet, S. Brauer, J. Mainville, Y. S. Yang, and M. Sutton, *Rev. Sci. Instrum.*, **60**, 1537 (1989).
18. C. Lavoie, C. Cabral, Jr., F. M. d'Heurle, and J. M. E. Harper, *Defect Diffus. Forum*, **194-199**, 1477 (2001).
19. H. B. Michaelson, *J. Appl. Phys.*, **48**, 4729 (1977).
20. T. P. Nolan, R. Sinclair, and R. Beyers, *J. Appl. Phys.*, **71**, 720 (1992).