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Impact of atomic-layer-deposited TiN on the gate oxide quality of W/TiN/SiO_2/Si metal–oxide–semiconductor structures

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We demonstrate the impact of atomic-layer-deposited TiN gate on the characteristics of W/TiN/SiO_2/*p*-Si metal–oxide–semiconductor (MOS) systems. Damage-free gate oxide quality was attained with atomic-layer-deposition (ALD)–TiN as manifested by an excellent interface trap density (D_{it}) as low as $\sim 4\times10^{10}$ eV^{-1} cm^{-2} near the Si midgap. ALD–TiN improved the D_{it} level of MOS systems on both thin SiO_2 and high-permittivity (high-*k*) gate dielectrics. The leakage current of a MOS capacitor gated with ALD–TiN is remarkably lower than that with sputter-deposited TiN and poly-Si gate at the similar capacitance equivalent thickness (CET). Less chlorine content in ALD–TiN films appears to be pivotal in minimizing the CET increase against postmetal anneal and improving gate oxide reliability, paving a way for the direct metal gate process. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1468273]

Direct metal gate has been studied to overcome the obstacles of polycrystalline-Si (poly-Si) gate structures such as gate depletion, boron penetration, and high resistance in narrow gate line.[1–16] Because of good thermal stability and midgap work function, refractory metals such as W and TiN have attracted lots of attention for sub-100 nm metal–oxide–semiconductor (MOS) device applications.[2–4,8–13] Unfortunately, direct metal gate prepared by physical vapor deposition (PVD) method can create defects such as metal penetration and plasma damages which lead to reliability problems of gate dielectrics.[5–8] To circumvent these obstacles, chemical vapor deposition (CVD)–TiN process was recently employed.[8–12] However, CVD–TiN prepared by metalorganic precursors introduced high carbon impurity and reliability problems,[10] while the film by $TiCl_4$ and NH_3 generated unstable capacitance equivalent thickness (CET) variation and reliability degradation due to high chlorine ([Cl]) content.[8,12] In order to prevent aforementioned hurdles, we approached a process, atomic-layer deposition (ALD), for TiN. The ALD approach may minimize impurity incorporation as well as remove the metal and/or plasma damages. In this letter, we present a damage-free direct metal gate using ALD–TiN process as confirmed by an excellent interface trap density (D_{it}) with reduced gate leakage current. Further, improved reliability characteristics in combination with stable CET variation are demonstrated.

MOS capacitors composed of W/TiN/SiO_2/*p*-Si were fabricated using 8 in., *p*-type Si (100) wafers with a resistivity of 8–10 Ω cm. After formation of field oxide, a standard pregate cleaning was employed and followed by the growth of controlled oxide (3 nm) in wet ambient at 750 °C. In addition, the MOS capacitors comprised of ZrO_2(5 nm)/SiO_2($\sim$0.7 nm)/*p*-Si structure were also fabricated to investigate the effect of TiN deposition method on the high-*k* gate dielectrics. The ultrathin interfacial SiO_2 was grown by rapid thermal oxidation at 750 °C and ZrO_2 films were prepared by ALD using $ZrCl_4$ and H_2O at 350 °C followed by dielectric improvement anneal at 600 °C in O_2. As a direct metal gate, TiN films (30 nm) were prepared by PVD, CVD, and ALD methods. PVD–TiN films were reactive sputtered under the power density of 1–7 W/cm^2 at 300 °C and CVD–TiN films prepared at 650 °C using $TiCl_4$ and NH_3. For ALD–TiN deposition, we used a traveling wave reactor by the cyclic dosing of $TiCl_4$ and NH_3 sources at the substrate temperature (T_s) of 450 °C. PVD–W (70 nm) was then deposited at 200 °C, followed by the patterning of square shape electrodes with various active areas of 4×10^{-6}–4×10^{-4} cm^2. Postmetal anneal (PMA) was carried out by furnace anneal at 450 °C in forming gas (10% H_2/90% N_2) or at 800 °C in N_2 for 30 min or by rapid thermal anneal (RTA) at 950 °C in N_2 for 20 s.

Electrical characterization of the W/TiN/SiO_2/Si MOS capacitor was performed in a light-free probe station. To scrutinize the level of interface traps with deposition method and PMA, capacitance–voltage (C–V) and conductance measurements were carried out using a HP4284A LCR meter.[8,17,18] The gate current density–voltage (J–V) and time-dependent dielectric breakdown measurements of the W/TiN/SiO_2/*p*-Si MOS capacitors were performed using a HP4156B. The chlorine content in the TiN/SiO_2 was probed by a PHI-6300 secondary ion mass spectrometer using a Cs^+ primary ion source of $\sim$3 keV beam energy.

Shown in Table I are typical characteristics of various TiN (30 nm) films we used. PVD–TiN showed relatively low

TABLE I. Typical characteristics of TiN (30 nm) films prepared by various deposition methods.

TiN (30 nm)	T_s (°C)	Crystal orientation	Resistivity ($\mu\Omega$ cm)	[Cl] (1×10^{18} atoms/cm^3)
PVD–TiN	300	(111)	110–120	~2
CVD–TiN	650	(200)	~150	~250
ALD–TiN	450	(111)/(200)	~80	~52

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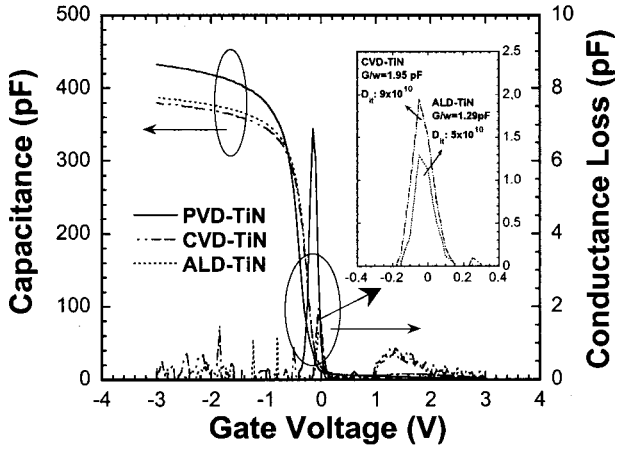

FIG. 1. High-frequency $C-V$ and $G/\omega-V$ characteristics of W/TiN/SiO_2 ($\sim$3 nm)/p-Si MOS structures after FGA at 450 °C for 30 min. The inset displays $G/\omega-V$ curves of CVD– and ALD–TiN films. The square electrode area is 4×10^{-4} cm^{-2}.

resistivity and negligible chlorine content. In particular, CVD–TiN displayed relatively high [Cl] ($\sim2.5\times10^{20}$ atoms/cm^3) and a resistivity (ρ) of $\sim$150 $\mu\Omega$ cm, whereas ALD–TiN exhibited the [Cl] as small as $\sim5.2\times10^{19}$ atoms/cm^3 and a resistivity of $\sim$80 $\mu\Omega$ cm. The lower ρ of ALD–TiN than that of CVD–TiN is attributed to the lower [Cl], consistent with earlier results.[19] We also note that the lower ρ of ALD–TiN over PVD–TiN is related with larger grain size as observed by transmission electron microscopy (not shown).

Figure 1 shows high-frequency $C-V$ and conductance loss $(G/\omega)-V$ characteristics of various TiN/SiO_2(3 nm)/p-Si MOS capacitors after forming gas anneal (FGA) at 450 °C. The conductance loss peaks shown in the inset describe the evolutionary changes of D_{it} with deposition method.[17,18] The loss values of $\sim$7 pF for PVD–TiN, 1.95 pF for CVD–TiN, and 1.29 pF for ALD–TiN correspond to the D_{it} values of $\sim4\times10^{11}$, $\sim8\times10^{10}$, and $\sim5.9\times10^{10}$ eV^{-1} cm^{-2}, respectively.

For more accurate D_{it} extraction, the $G/\omega-\log\omega$ characteristics of the W/TiN/SiO_2(3 nm)/p-Si MOS capacitors after FGA were explored for a given surface potential (Fig. 2), and extracted D_{it} values with various PMA are summarized in Fig. 3. There are several important features. First, the D_{it} of ALD–TiN gate structure was the lowest. The D_{it} level

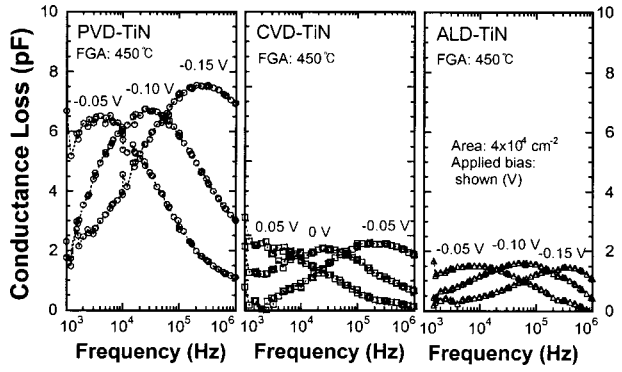

FIG. 2. The measured conductance loss (G/ω)-$\log\omega$ plots of various TiN/SiO_2($\sim$3 nm)/p-Si MOS capacitor as a function of gate voltage and PMA. The PMA was carried out by FGA at 450 °C. The applied gate voltages or surface potentials are also shown.

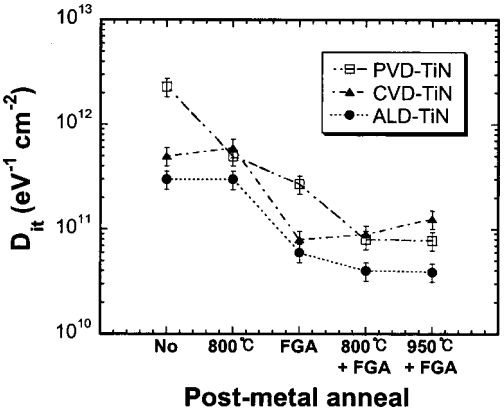

FIG. 3. Interface trap density (D_{it}) of W/TiN/SiO_2/p-Si MOS capacitors as a function of PMA.

of $\sim5.4\times10^{10}$ eV^{-1} cm^{-2} near the Si midgap after FGA and $\sim4\times10^{10}$ eV^{-1} cm^{-2} after furnace anneal over 800 °C and FGA were obtained. The present D_{it} value attained with ALD–TiN is comparable to the level of poly-Si gate, indicating that damage-free direct metal gate process can be realized using ALD approach. Second, the D_{it} of PVD–TiN decreases from $\sim2.7\times10^{11}$ eV^{-1} cm^{-2} (FGA only) to $\sim7.8\times10^{10}$ eV^{-1} cm^{-2} (furnace anneal at 800 °C and FGA), suggesting that the high temperature anneal in combination with FGA is essential to anneal out the damages introduced during the PVD process. On the other hand, the D_{it} with CVD–TiN was $\sim8\times10^{10}$ eV^{-1} cm^{-2} after FGA and this has slightly increased to $\sim1.2\times10^{11}$ eV cm^{-2} after PMA at >800 °C and FGA (Fig. 3), which is under investigation. The lower D_{it} values with ALD– and CVD–TiN after FGA are ascribed to both the damage-free deposition and Cl passivation at the dangling bonds of SiO_2/Si interfaces.[8,20]

Figure 4 exhibits CET variation of the W/TiN/SiO_2(3 nm)/p-Si MOS capacitors with deposition scheme and PMA. The CET increases in the order of PVD–TiN, ALD–TiN, and CVD–TiN. The lowest CET ($\sim$3.08 nm) was attained with PVD–TiN after FGA, while a slight CET increase ($\sim$0.12 nm) was observed after RTA at 950 °C and FGA. The CET of MOS capacitor gated with ALD–TiN was $\sim$3.45 nm and negligible CET change ($\sim$0.03 nm) was

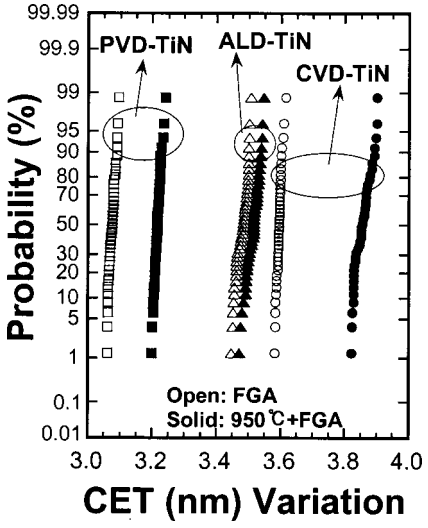

FIG. 4. CET variation of W/TiN/SiO_2/p-Si MOS capacitors with PMA.

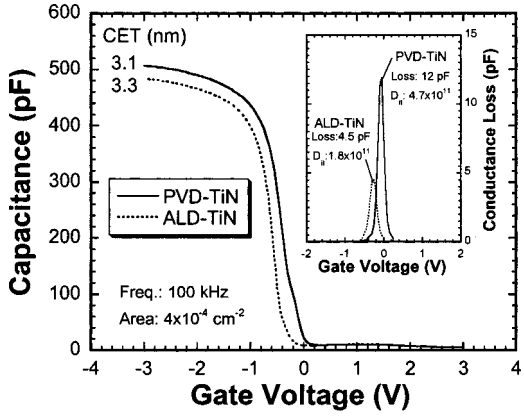

FIG. 5. $C-V$ characteristics of TiN/ZrO_2(5 nm)/SiO_2(0.7 nm)/p-Si MOS capacitors as a function of TiN deposition method at 100 kHz. The conductance loss $(G/\omega)-V$ characteristics are displayed in the inset. Those capacitors were experienced a PMA of furnace anneal at 600 °C and FGA.

achieved against high thermal budget at 950 °C; however, noticeable CET increase of ~0.35 nm was observed with CVD–TiN. We also observed that ALD–TiN films deposited at low T_s (<350 °C) showed higher [Cl] incorporation, so higher resistivity films and CET increase with PMA.[21]

The effects of TiN deposition method on the high-k gate dielectrics are depicted in Fig. 5, displaying $C-V$ curves of the TiN/ZrO_2(5 nm)/SiO_2(~0.7 nm)/p-Si MOS capacitors. The $G/\omega-V$ characteristics are shown in the inset. The CET value with ALD–TiN is slightly higher than that with PVD–TiN. The conductance loss or D_{it} value gated with ALD–TiN is ~4.5 pF or $\sim 1.8\times 10^{11}\ \mathrm{eV}^{-1}\ \mathrm{cm}^{-2}$, a factor of three lower than the D_{it} of PVD–TiN. Similar trends were observed for other high-k gate dielectrics like Ta_2O_5 (not shown), corroborating the necessity of damage-free direct metal gate process on the high-k gate dielectrics as well.

Figure 6 highlights $J-V$ and reliability characteristics of W/TiN/SiO_2(3 nm)/p-Si MOS capacitors with PMA (800 °C+FGA). The gate leakage current of MOS capacitor

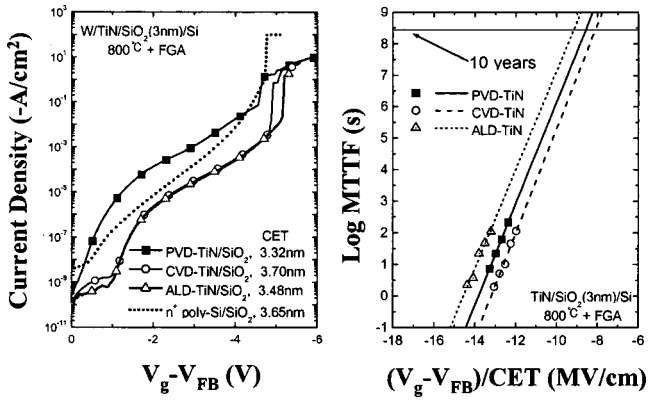

FIG. 6. (a) $J-V$ curves and (b) a 10 year lifetime of W/TiN/SiO_2(3 nm)/p-Si MOS structures with PMA (furnace anneal at 800 °C and FGA) measured at room temperature. The n^+ poly-Si/SiO_2/p-Si MOS structure having the similar CET was also compared in Fig. 6(a). Each data point in Fig. 6(b) represents mean time to failure of 40 data points on the 8 in. wafers. The $E_{ox,critical}$ of over-9.2 MV/cm (−3.38 V at CET=3.5 mm) may be used with ALD–TiN at room temperature, while the $E_{ox,critical}$ of −8.6 MV/cm (−3.02 V at CET=3.32 nm) and −8.2 MV/cm (−3.14 V at CET=3.8 nm) can be used for PVD– and CVD–TiN, respectively.

using ALD–TiN is about 2–3 orders of magnitude lower than that using PVD–TiN. In particular, the low-field leakage current level in the ALD–TiN gate case is distinctly lower than that with poly-Si at the similar CET, possibly due to the physically thicker SiO_2. A projected 10 year lifetime as measured by the constant voltage stress is shown in Fig. 6(b). MOS capacitors gated with ALD–TiN exhibited the highest critical electric field ($E_{ox,critical}$) over PVD– and CVD–TiN, demonstrating reliable gate oxide integrity. The lowest $E_{ox,critical}$ for CVD–TiN electrode case is attributed to the high residual Cl in TiN which can diffuse to the gate oxide, resulting in the formation of Cl-related trap site.[12]

In summary, we explored an unique damage-free direct metal gate process using ALD–TiN with low D_{it}, negligible CET variation, reduced gate leakage current, and robust reliability characteristics. The lower level of Cl content by ALD process was pivotal in achieving negligible CET variation against PMA and better gate oxide reliability. Selection of pertinent precursors for impurity control would be critical for future metal gate technology using ALD.

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