



Application of photodeposited Cd to Schottky barrier diode and transistor fabrication on InP and In0.53Ga0.47As substrates

Thomas J. Licata, Michael T. Schmidt, Richard M. Osgood Jr., Winston K. Chan, and Rajaram Bhat

Citation: Applied Physics Letters **58**, 845 (1991); doi: 10.1063/1.104508 View online: http://dx.doi.org/10.1063/1.104508 View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/58/8?ver=pdfcov Published by the AIP Publishing

Articles you may be interested in

Structure of Ga0.47In0.53As epitaxial layers grown on InP substrates at different temperatures Appl. Phys. Lett. **63**, 2809 (1993); 10.1063/1.110294

Barrier height enhancement of Schottky diodes on nIn0.53Ga0.47As by cryogenic processing Appl. Phys. Lett. **63**, 1939 (1993); 10.1063/1.110607

Dependence of electrical characteristics of MBE Ga0.47In0.53As planar doped barriers on InP substrates J. Vac. Sci. Technol. B **2**, 194 (1984); 10.1116/1.582777

QuasiSchottky barrier diode on nGa0.47In0.53As using a fully depleted p +Ga0.47In0.53As layer grown by molecular beam epitaxy Appl. Phys. Lett. **40**, 401 (1982); 10.1063/1.93117

Electron mobility and energy gap of In0.53Ga0.47As on InP substrate J. Appl. Phys. **47**, 5405 (1976); 10.1063/1.322570



Application of photodeposited Cd to Schottky barrier diode and transistor fabrication on InP and $In_{0.53}Ga_{0.47}As$ substrates

Thomas J. Licata, Michael T. Schmidt, and Richard M. Osgood, Jr. Microelectronics Sciences Laboratories, Columbia University, New York, New York 10027

Winston K. Chan and Rajaram Bhat Bellcore, Red Bank, New Jersey 07701

(Received 16 July 1990; accepted for publication 26 November 1990)

We report on using a thin (~200 Å) layer of photodeposited Cd to form high Schottky barrier height contacts to InP and In_{0.53}Ga_{0.47}As. Current-voltage measurements of the Schottky diodes yield barrier heights of 0.70 and 0.55 eV to InP and In_{0.53}Ga_{0.47}As, respectively. The photodeposition process has been integrated with conventional clean room processing to fabricate Au/Cd/In_{0.53}Ga_{0.47}As transistors with high transconductances (~200 mS/mm) and operating frequencies (f_{max} ~30 GHz). X-ray photoelectron spectroscopy of thin Cd photodeposits on InP shows that the process produces an interfacial (~10 Å thick) Cd-InP reaction zone covered by metallic Cd.

Efforts to elevate the Schottky barrier heights to InP and In_{0.53}Ga_{0.47}As have generally been based on interposing a high band-gap layer or a *pn* junction between a metal contact layer and the semiconductors.^{1–10} However, recent work has demonstrated that there are metals that exhibit intrinsically high barrier heights with InP. Specifically, Sa and Meiners found barrier heights of 0.62 and 0.92 eV for electroplated cadmium and mercury point contacts with InP.¹¹ Electroplated cadmium-based metal-semiconductor field-effect transistors (MESFETs) were soon fabricated, albeit with 100 μ m gate lengths.¹² As electroplating of Cd is not well suited to forming micrometer-scale device structures, and evaporation of uniform Cd layers is difficult, alternative deposition techniques for Cd films are drawing new attention.^{13,14}

Here, we present a single-step, potentially metallorganic chemical vapor deposition (MOCVD) and metallorganic molecular beam epitaxy (MOMBE)-compatible method for the fabrication of Cd/InP and Cd/ $In_{0.53}Ga_{0.47}As$ interfaces and demonstrate its applicability to the formation of micrometer-scale electronic devices. Specifically, a thin Cd layer is photodeposited on the semiconductor surface prior to evaporation of a thicker Au contact layer. In this technique, which has been described in detail elsewhere,¹⁵ low-power ultraviolet (UV) photons irradiate the sample in a dimethylcadmium (DMCd) ambient. Dissociation of the gas and surface phase DMCd molecules occurs through a purely photolytic mechanism. Note that in all the experiments reported here, laser heating of the semiconductor surface was sufficiently small to preclude pyrolytic dissociation of DMCd or diffusion of Cd into the semiconductor.15

We have applied the photodeposition process to the formation of Schottky barrier diodes on InP and In_{0.53}Ga_{0.47}As, and In_{0.53}Ga_{0.47}As MESFETs. For the Schottky diodes, a nonlithographic, shadow-mask process was used to fabricate large-area (0.015 cm²) Au/InP, Au/Cd/InP, Au/In_{0.53}Ga_{0.47}As, and Au/Cd/In_{0.53}Ga_{0.47}As contacts for determination of the Schottky barrier heights through current-voltage [I(V)] measurements. Blanket

AuGeNi ohmic back contacts were formed on bulk 5×10^{17} /cm³ Te-doped semiconductor samples. The samples were degreased and then deoxidized for one minute using an NH₄OH/H₂O solution (1:1 for InP, 1:10 for In_{0.53}Ga_{0.47}As).¹⁶ The samples were then loaded within 2 min into a cryopumped stainless-steel high-vacuum cell having a base pressure of 1×10^{-7} Torr.

For Cd depositions, the vacuum cell was statically filled to 1 Torr of DMCd. The $\lambda = 248$ nm beam of a KrF excimer laser was attenuated to 3 mJ/cm² per pulse. Blanket depositions of Cd were accomplished using 2000 laser pulses (10 Hz for 200 s), which resulted in the formation of visible Cd films on the samples and cell window. Based on Auger electron spectrocopy (AES) depth profiling of our Cd films (Fig. 1), we estimate a thickness of ~200 Å.

After a 2 min exposure to air during transit, the Cdcoated samples were mounted next to control samples in a conventional thermal evaporator. A 1500-Å-thick Au film was evaporated through a Mo shadow mask to form the diode structures. Before I(V) measurements, all samples were submerged in 25% HCl for 2 min to etch away all exposed Cd, since failure to do this resulted in large shortcircuit currents carried by the Cd blanket film to the ohmic back contact. Control samples not coated with Cd showed no such shorting.

The Schottky barrier heights and ideality factors (n) were obtained from I(V) characteristics. The values of ϕ_b determined from these experiments are 0.70 eV for Au/Cd/InP (n = 1.03) and 0.55 eV for Au/Cd/In_{0.53}Ga_{0.47}As (n = 1.08). These barrier heights are significantly higher than the barrier heights formed between Au and InP or In_{0.53}Ga_{0.47}As $(0.43 \text{ eV}^{17} \text{ and } 0.25 \text{ eV}, ^{18}$ respectively), thereby making fabrication of FETs on both substrates feasible.

As a demonstration of the applicability of this process to the fabrication of micrometer-scale devices, *n*-channel depletion-mode $In_{0.53}Ga_{0.47}As$ field-effect transistors with Au/Cd gates were fabricated using conventional photolithographic techniques. MOCVD was used to grow the various epitaxial layers on a semi-insulating InP substrate.

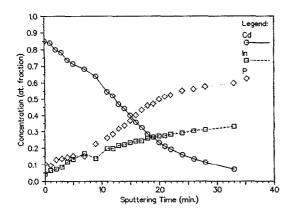


FIG. 1. Auger electron spectroscopy (AES) depth profile for Cd photodeposited on InP using 2000 pulses (10 Hz for 200 s) of 248 nm radiation in 1 Torr DMCd. The sputtering rate was ~ 15 Å/min.

A 2500-Å-thick, 6×10^{16} /cm³ Te-doped In_{0.53}Ga_{0.47}As channel was chosen to provide a high transconductance and a low pinchoff voltage, whereas the 1000-Å-thick, 6×10^{18} /cm³ Te-doped cap layer was used to facilitate formation of the ohmic contacts. Isolation mesas to the InP substrate were formed by Ar-ion milling followed by a 1 min etch in H₃PO₄:H₂O₂:H₂O (1:1:38). AuGeNi ohmic contacts were used for the source and drain contacts. The source resistance was measured to be 1.06 Ω mm. Photoresist was patterned with openings for the $1.2-\mu$ m-long gates. The photoresist served as a mask both for the gate recess etch and for the subsequent gate metal liftoff. After the gate recess etch, the samples were deoxidized in dilute NH₄OH, and loaded into the Cd deposition cell. After Cd deposition, as above, and evaporation of a Au blanket film, a liftoff in acetone was used to define the 1.2 μ m gate. We note that the photodeposition process produced a uniform Cd layer over the $\sim 1 \text{ cm}^2$ samples used in these experiments and did not limit the device yield.

The drain current-voltage characteristics for our 1.2 μ m gate length, 100 μ m gate width Au/Cd/ In_{0.53}Ga_{0.47}As MESFETs have been shown previously.¹⁵ Our devices showed $I_{\rm DSS}$ values of ~300 mA/mm at $V_{\rm DS} = 1.0$ V and pinchoff voltages of ~ -1.5 V. The best device exhibited an extrinsic transconductance of 230 mS/mm (250 mS/mm intrinsic transconductance). Figure 2 shows our results for high-frequency operation. Specifically, we measured a best power gain cutoff frequency $f_{\rm max}$ of 31.1 GHz ($f_T = 22.3$ GHz), demonstrating that there was no significant potential drop across the metal/semiconductor interface at high frequencies.

XPS analysis was used to investigate *in situ* prepared Cd/InP interfaces. In these experiments, a monochromatized Al $K\alpha$ line (1486.6 eV) was used to monitor the In and Cd $3d_{5/2}$ peaks, the C and O 1s peaks, and the P 2p peak. Exposure of chemically cleaned surfaces to the standard deposition ambient of 1 Torr DMCd for 5 min without irradiation produced a slight elevation of the C peak and the appearance of the broad, slightly asymmetric Cd peak shown in Fig. 3. Due to the peak's breadth and pre-

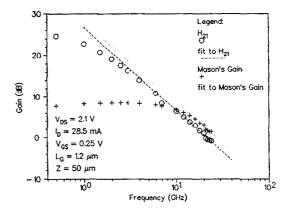


FIG. 2. Power gain cutoff measurements for Au/Cd/In_{0.53}Ga_{0.47}As 1.2 μ m gate length MESFET. The gate bias and current were -1 V and 0.3 mA, respectively.

vious work,¹⁹ we used three components to fit this feature. The lowest binding energy component (405.0 eV) corresponds to metallic Cd, whereas the higher binding energy components correspond to reacted Cd species. Note that in all our data analysis, the 0.5 eV peak separations were kept constant. The absolute positions of the peaks, however, were allowed to move in order to account for Fermi level shifts and matrix effects.

Although the peaks at 405.5 and 406.0 eV have been attributed to an adsorbed layer of partially and undissociated DMCd on other substrates,¹⁹ changes in the peak areas after heat treatment and as a function of the amount of deposited Cd¹⁵ argue that for DMCd on InP, these peaks correspond to reacted Cd compounds. In one such experiment, ~ 30 Å of Cd was photodeposited on a chemically cleaned surface [Fig. 4(a)] which was then heated to 300 °C *in vacuum* for 5 min [Fig. 4(b)]. Figure 4(b) shows that the heat treatment caused the high-energy peaks from reacted Cd to increase at the expense of the metallic Cd peak under conditions where no physisorption of DMCd was possible. Note that the high-energy side of the as-

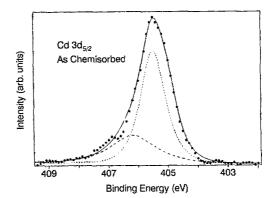


FIG. 3. Cd $3d_{5/2}$ peak from monochromatic Al K α XPS of chemically cleaned InP exposed to 1 Torr of DMCd for 5 min with no irradiation (as-chemisorbed). The peak was fitted with three components corresponding to metallic Cc (405.0 eV), a spontaneously formed interfacial InP-reacted cadmium compound (405.5 eV), and oxidized Cd (406.0 eV).

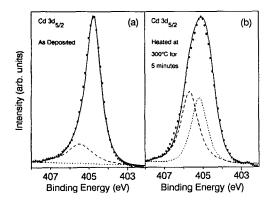


FIG. 4. Cd $3d_{5/2}$ XPS peak for 30 Å of photodeposited Cd (a) before and (b) after heating to 300 °C in vacuum for 5 min. Upon heating, the higher binding energy peaks increase at the expense of the peak at 405.0 eV. Note that desorption of the Cd upon heating resulted in a drop in the measured Cd 3d intensity before normalization to yield this plot. However, the absolute intensity of the reacted Cd peaks increased by $\sim 50\%$.

deposited spectrum [Fig. 4(a)] was fitted using only one component, since the attenuated high-energy peaks from the buried reacted layer were too weak to fit unambiguously with two components.

Separate experiments on UHV-prepared surfaces indicate that the component at 405.5 eV corresponds to a Cd-P compound, and the component at 406.0 eV corresponds to oxidized Cd. Thus, dark adsorption of DMCd onto chemically cleaned InP results in spontaneous dissociation of the DMCd to form metallic Cd, a Cd-P compound (from reaction with the substrate) and a Cd-O compound (from reaction with the monolayer-scale native oxide). After the reacted interfacial layer has formed, photodeposition of Cd produces a clean metallic layer with no elevation of C over the as-chemisorbed levels.

Attenuation of substrate peaks and reacted Cd peaks as a function of the amount of Cd photodeposited on the surface shows that the extent of the spontaneously formed reacted layer and any associated disruption of the interface is only ~ 10 Å or so at room temperature. Our measurements of In and P core level spectra did not allow us to determine the stoichiometry of the substrate-reacted Cd compound. However, based on the lack of a measurable shift in our In peak (which would indicate segregated In), and thermodynamic considerations presented elsewhere,¹⁵ we believe the interfacial compound to be a $Cd_xIn_yP_z$ compound.

To conclude, we have shown that Cd interlayers on InP and In_{0.53}Ga_{0.47}As substrates can be photodeposited

from DMCd using deep-UV radiation. The resulting Schottky barrier heights for ideal diodes are larger than those measured for more commonly applied metals and are high enough to be useful for electronic devices. XPS analysis indicates that a reacted interfacial layer spontaneously forms upon exposure of InP to DMCd, and photodeposition produces a clean Cd overlayer. The photodeposition step is easily integrated into conventional clean-room processing and yields high-performance transistors with micrometer-sized gates. To date, there are no obvious obstacles limiting the application of this technique to smaller, i.e., submicron, gate lengths.

The authors would like to thank Dragan Podlesnik and Ping Shaw for many useful discussions and suggestions. In addition, we gratefully acknowledge Hermann Schumacher for transistor gain cutoff measurements. This work was supported by grants from DARPA/AFOSR, ONR and the IBM Materials and Processing Science Grant Program.

- ¹T. Y. Chang, R. F. Leheny, R. E. Nahory, E. Silberg, A. A. Ballman, E. A. Caridi, and C. J. Harrold, IEEE Electron Device Lett. EDL-3, 56 (1982).
- ²K. Steiner, U. Seiler, and K. Heime, Appl. Phys. Lett. 53, 2513 (1988).
- ³O. Wada and A. Majerfeld, Electron. Lett. 14, 125 (1978).
- ⁴D. V. Morgan and J. Frey, Electron. Lett. 14, 737 (1978).
- ⁵H. Morkoc, T. J. Drummond, and C. M. Stanchak, IEEE Trans. Electron Devices ED-28, 1 (1981).
- ⁶P. D. Gardner, S. G. Liu, S. Y. Narayan, S. D. Colvin, J. P. Paczkowski, and D. R. Capewell, IEEE Electron Device Lett. EDL-7, 363 (1986).
- ⁷S. Loualiche, H. L'Haridon, A. Le Corre, D. Lecrosnier, M. Salvi, and P. N. Favennec, Appl. Phys. Lett. 52, 540 (1988).
- ⁸S. Loualiche, A. Ginoudi, H. L'Haridon, M. Salvi, A. Le Corre, D. Lecrosnier, and P. N. Favennec, Appl. Phys. Lett. 54, 1238 (1989).
- ⁹K. Hirose, K. Ohata, T. Mizutani, T. Itoh, and M. Ogawa, Gallium Arsenide and Related Compounds 1985 (Adam Hilger, Bristol, 1985), pp. 529-534. ¹⁰C. K. Peng, M. I. Aksun, A. A. Ketterson, H. Morkoc, and K. R.
- Gleason, IEEE Electron Device Lett. EDL-8, 24 (1987).
- ¹¹C. J. Sa and L. G. Meiners, Appl. Phys. Lett. 48, 1796 (1986).
- ¹²L. G. Meiners, A. R. Clawson, and R. Nguyen, Appl. Phys. Lett. 49, 340 (1986).
- ¹³W. K. Chan, H. M. Cox, J. H. Abeles, and S. P. Kelty, Electron. Lett. 23, 1346 (1987).
- ¹⁴W. K. Chan, G. Chang, R. Bhat, and N. E. Schlotter, IEEE Electron Device Lett. EDL-9, 220 (1988).
- ¹⁵T. J. Licata, M. T. Schmidt, D. V. Podlesnik, V. Liberman, R. M. Osgood, Jr., W. K. Chan, and R. Bhat, J. Electron. Mater. 16, 1239 (1990).
- ¹⁶D. E. Aspnes and A. A. Studna, Appl. Phys. Lett. 39, 316 (1981).
- ¹⁷N. Newman, T. Kendelewicz, L. Bowman, and W. E. Spicer, Appl. Phys. Lett. 46, 1176 (1985).
- ¹⁸K. Kajiyama, Y. Mizushima, and S. Sakata, Appl. Phys. Lett. 23, 458 (1973).
- ¹⁹C. D. Stinespring and A. Freedman, Chem. Phys. Lett. 143, 584 (1988).