Selective Tungsten CVD in a Hot Walled Reactor by Silane Reduction of WF_6

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As circuit dimensions decrease, junctions become shallower with a corresponding increase in active area sheet resistance. Selective chemical vapor deposition of tungsten on exposed Si areas has been investigated as a means of increasing both active area and polysilicon gate conductivity. However, H_2 reduction of WF_6 has been typified by encroachment or other attack of the Si during deposition (1). Experiments using SiH_4 reduction of WF_6 have shown that such damage can be eliminated (2-6). The reactors used in these processes have typically been of the cold wall type which confine the bulk of heated areas to the wafers but can accomodate only a small number of wafers. We report here on the results of SiH_4 reduction of WF_6 in a modified hot-walled low pressure CVD tube.

Figure 1 shows a schematic of the LPCVD system used. A 155mm ID, 205cm long quartz tube was externally heated by a 3-zone resistance element with temperatures controlled to ±2°C. Slotted quartz wafer boats were placed on a cantilever which positioned them midway down the tube. The wafers were mounted vertically and placed back to back in the same boat slot to shield their backside from deposition. WF_6 and H_2 were introduced through separate lines into the loading end of the reactor while SiH_4 was injected through a quartz tube inserted through the pumping end. The injector tube, sealed at one end, was perforated with a series of holes across 51cm of its length directly under the wafer boats. Earlier experiments had demonstrated that when SiH_4 was introduced from the loading end of the tube, the reaction with WF_6 rapidly coated the tube wall and cantilever near the gas entry area. This depleted the downstream reactant supply resulting in low deposition rates on the wafers. The deposit on the tube walls also had poor adherence, causing flaking and particulate problems.

The wafers used in this study were 100mm diam <100> oriented single crystal Si. Test wafers were coated with 3wt% P-doped low temperature oxide, and patterned with $1cm^2$ area openings down to Si to occupy ≈11% of the wafer area - approximating the amount of Si exposed on device wafers. The test wafers were then implanted with either BF_2 (4E15 at 40Kev) or As (5E15 at 90Kev), representative of actual device implants, and annealed at 850°C in N_2 for 6 hours. Active areas on device wafers that contained structures for measuring N+/P and P+/N diode leakage and sheet resistance were defined by standard field isolation techniques.

Prior to tungsten deposition the wafers were given a standard wet chemical clean and a short HF dip and deionized water rinse. The tube temperature at loading was less than 120°C, and after a series of H_2 purges and evacuations, was ramped to a set point of 250°C. After a short tungsten deposition in a flow of WF_6 and H_2, SiH_4 was introduced for a length of time required to achieve the desired film thickness. This sequence was necessary to achieve good selectivity and adhesion of the tungsten film to silicon. Following deposition, the reactor was again evacuated and backfilled with N_2 to atmospheric pressure.

Periodic cleaning of the tube to remove tungsten nucleation sites was done with an in-situ etch using NF_3 at 600°C (7). Following cool down, the tube was conditioned with a short deposition from SiH_4/WF_6.

Figure 2 shows tungsten deposition rate and bulk resistivity for different SiH_4/WF_6 flow ratios at a deposition temperature of 250°C, tube pressure of 150 mTorr, with constant WF_6 and H_2 flows of 10 sccm and 200 sccm respectively. Tungsten deposition rate increases with increasing SiH_4 flow, reaching a plateau at a SiH_4/WF_6 gas flow ratio of 0.4. Increasing the ratio above this point has little effect on either the deposition rate or film resistivity. The slightly lower deposition rate seen on P+ silicon is believed to be due to a delay in the start of W deposition on this material, as reported elsewhere (6). The thinner tungsten films generally were found to have a slightly higher bulk resistivity.

Selectivity of tungsten deposition on test samples over the flow ratios studied is acceptable up to at least 2000Å thickness. No loss of selectivity was observed when the amount of exposed silicon on the wafers was increased. Deposition rate, however, was found to be inversely proportional to the total amount of silicon exposed on the wafers. Run to run and wafer to wafer reproducibility of ± 10% can be obtained by attempting to maintain constant exposed area. Across the wafer uniformity using these conditions was typically better than ± 6%.

Figure 3 compares current leakage histograms of 5.25E-04cm^2 diodes strapped with tungsten using either the SiH_4 or H_2 reduction process. A SiH_4/WF_6 ratio of 0.6 was used for the SiH_4 reduction process which deposited 1000Å of W having a sheet resistance of 4 ohms/*square*. The films deposited by H_2 reduction were 500Å thick and had a sheet resistance of 3.5 ohms/*square*. Leakage measurements were obtained at a reverse bias of 5 volts. The results for diodes coated from SiH_4 reduced WF_6 show a very narrow distribution with the bulk of the samples having leakage of less than one picoamp. This distribution was similar to that found in control wafers not coated with tungsten. Diodes processed with H_2 reduced WF_6 show a much broader leakage distribution, the median value of which is 2 orders of magnitude higher than that obtained with the SiH_4 reduction process. The high leakage associated with the H_2 reduction process indicates degradation of the shallow

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junctions and would not be acceptable in submicron geometry devices.

In summary, a SiH_4 reduced WF_6 selective tungsten deposition process using a hot-walled low pressure tube has been developed. Film properties and and current leakage results for N+ and P+ diodes are acceptable for typical submicron CMOS applications and are similar to those reported elsewhere using cold-walled equipment (2,3,6). Further investigations presently underway include studies of the effects of deposition temperatures, SiH_4/WF_6 ratios, and H_2 reduction time on film properties and device leakage.

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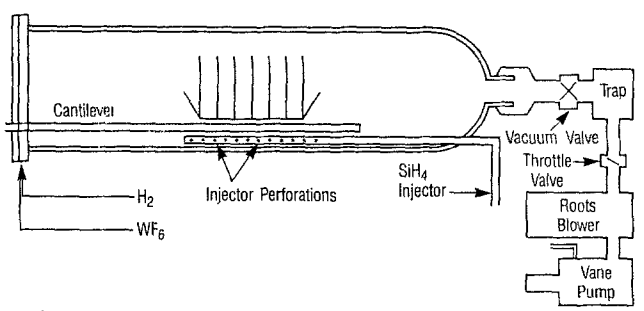

Fig. 1. Schematic diagram of hot-walled tungsten deposition system.

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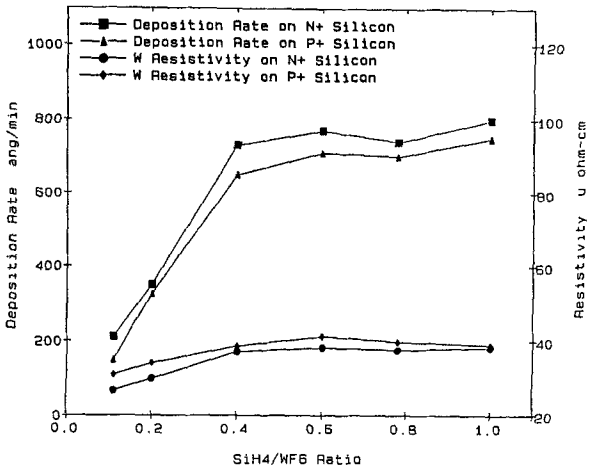

Fig. 2. Tungsten Deposition rate and film resistivity on N+ and P+ silicon for different SiH4/WF6 flow ratios.

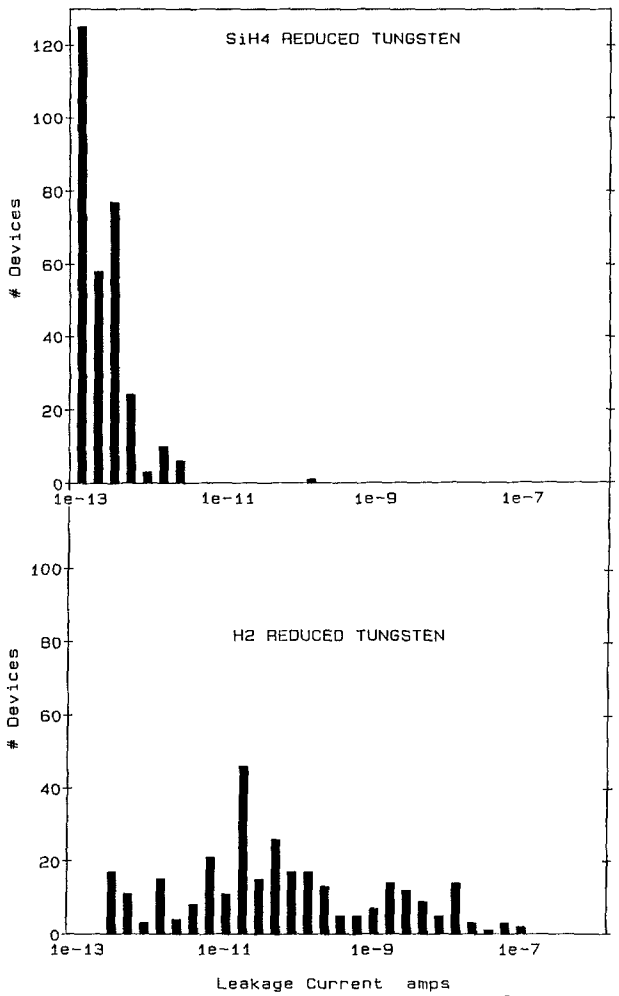

Fig. 3. Leakage current at 5V for 5.25E-04cm^2 N+/P and P+/N diodes strapped with (a) 1000A of SiH_4 reduced tungsten or (b) 500A of H_2 reduced tungsten.