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Citation: Applied Physics Letters **78**, 2357 (2001); doi: 10.1063/1.1362331
View online: http://dx.doi.org/10.1063/1.1362331
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/78/16?ver=pdfcov
Published by the AIP Publishing

Electrical and materials properties of ZrO_2 gate dielectrics grown by atomic layer chemical vapor deposition

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(Received 12 September 2000; accepted for publication 12 February 2001)

Structural and electrical properties of gate stack structures containing ZrO_2 dielectrics were investigated. The ZrO_2 films were deposited by atomic layer chemical vapor deposition (ALCVD) after different substrate preparations. The structure, composition, and interfacial characteristics of these gate stacks were examined using cross-sectional transmission electron microscopy and x-ray photoelectron spectroscopy. The ZrO_2 films were polycrystalline with either a cubic or tetragonal crystal structure. An amorphous interfacial layer with a moderate dielectric constant formed between the ZrO_2 layer and the substrate during ALCVD growth on chemical oxide-terminated silicon. Gate stacks with a measured equivalent oxide thickness (EOT) of 1.3 nm showed leakage values of 10^{-5} A/cm^2 at a bias of -1 V from flatband, which is significantly less than that seen with SiO_2 dielectrics of similar EOT. A hysteresis of 8–10 mV was seen for ± 2 V sweeps while a midgap interface state density (D_{it}) of $\sim 3\times 10^{11}$ states/cm eV was determined from comparisons of measured and ideal capacitance curves. © *2001 American Institute of Physics.*
[DOI: 10.1063/1.1362331]

Due to increasing levels of direct tunneling current and reliability problems, SiO_2 thinner than approximately 1.5 nm cannot be used as the gate dielectric for complementary metal oxide semiconductor technology.[1] Many of the conventional high-K candidates studied for capacitor applications, such as TiO_2, Ta_2O_5, and BST, require a barrier layer to prevent interdiffusion with the substrate and possible interfacial reactions. With gate applications, however, a single-layered structure is preferred for process simplicity and minimization of equivalent oxide thickness (EOT). One of the most promising material replacements for SiO_2 that has been shown to be thermodynamically stable with respect to solid state reaction with silicon is ZrO_2.[1–3] Its stability, along with its large band gap and dielectric constant of 20–25, make it an excellent candidate for gate dielectric applications.[4,5] In this letter, we present preliminary results on ZrO_2-based gate stacks deposited by atomic layer chemical vapor deposition (ALCVD).

Ultrathin zirconium oxide films were deposited on 200 mm p-epi/p^+ silicon test wafers using ALCVD at ASM Microchemistry. The deposition process was performed at 300 °C using alternating surface-saturating reactions of $ZrCl_4$ and H_2O. The first set of samples was patterned before dielectric deposition to create local oxidation-defined metal-oxide-semiconductor capacitor (MOSCAP) structures. Prior to dielectric deposition, the substrates for these samples were nitrided by a rapid thermal nitridation in NH_3 at a temperature of 700 °C. The second set of samples was not patterned before ZrO_2 deposition. With this set, the ZrO_2 films were deposited directly onto the original chemical silicon oxide of the as-received wafers. An Al/TiN top electrode was deposited by CVD on all samples and patterned to create 85×85 μm^2 capacitors for electrical testing. No postdeposition anneals were performed.

High-resolution transmission electron microscopy (TEM) micrographs and electron diffraction patterns were obtained using a Phillips EM430 microscope operating at a 300 kV accelerating voltage, which offers a point-to-point spatial resolution of 2.0 Å. The cross-sectional TEM micrograph in Fig. 1(a) shows the structure of the TiN/ZrO_2/p-Si MOS capacitor. The micrograph reveals the polycrystalline nature of the 50 Å film, in addition to the 15 Å interfacial layer between the ZrO_2 and the silicon substrate. From electrical measurements, the EOT of the gate stack is measured to be 13 Å, which is less than the thickness of the interfacial layer. This observation supports the proposal that the amorphous interfacial layer has a dielectric constant greater than

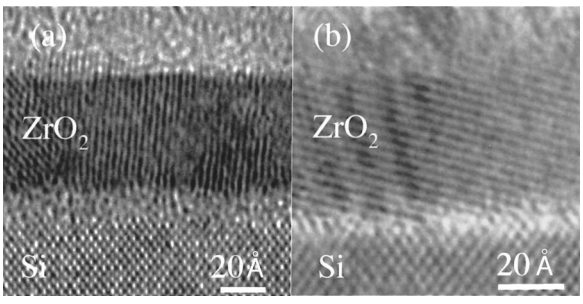

FIG. 1. Cross-sectional TEM micrographs show the morphology of the TiN/ZrO_2/p-Si gate stack structure on (a) chemical oxide-terminated silicon and (b) HF-last silicon.

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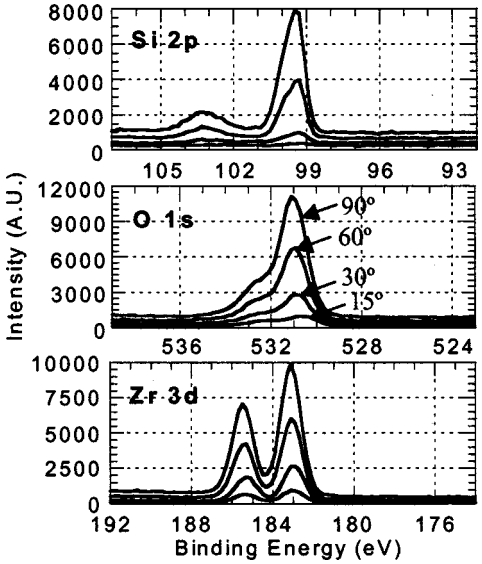

FIG. 2. XPS spectra show typical ZrO_2 bonding in the bulk dielectric film and SiO_2 bonding in the interfacial layer. Scans are stacked in increasing angle from 15° on bottom to 90° on top.

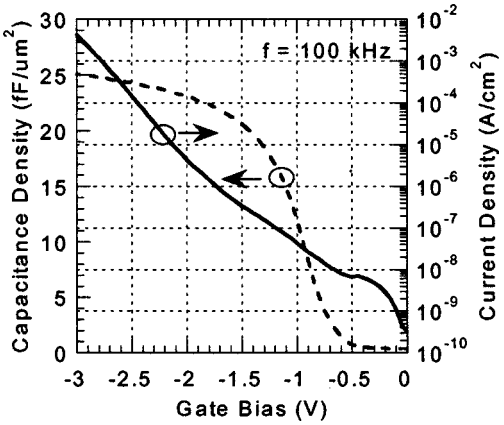

FIG. 3. *CV* curve of 50 Å ZrO_2 film atop a 13 Å nitrided layer reveals EOT value of 13.8 Å, while *JV* characteristics show extremely low leakage levels up to −3 V.

that of SiO_2. Preliminary electron diffraction studies show the 30 and 50 Å as-deposited ZrO_2 layers to have a cubic crystal structure. The thickness of the interfacial layer was found to be largely determined by the pre-deposition Si surface preparation, and not by the ALCVD processing conditions. TEM micrographs of ZrO_2 deposited onto HF-last Si surfaces showed <5 Å of amorphous interfacial layer [Fig. 1(b)]. However, interfacial quality in terms of film roughness and leakage properties of the MOSCAP structures was poor. Copel and co-workers have noted similar results and have suggested that nonuniform hydrogen desorption from the HF-last surface causes uneven nucleation of ZrO_2 during film deposition.[6]

X-ray photoelectron spectroscopy (XPS) profiles were measured with a Surface Science Instruments S-Probe (Al K_α x-ray source). Angle-resolved scans at 15°, 30°, 60°, and 90° in relation to the film surface are shown in Fig. 2 for a 3 nm ZrO_2 film on a 1.4 nm chemical silicon oxide. The 15° scan shows strong signatures of typical ZrO_2 bonding, namely the shifted Zr 3*d* oxide doublet at ~183 and 185 eV and the O 1*s* peak at ~531 eV. The scans at steeper angles show increasing percentages of oxygen bound to Si from both the O 1*s* peak at ~533 eV and the shifted Si 2*p* peak at ~103 eV, signifying a silica-based interfacial layer as seen with TEM. No Si–Zr bonding was noted, suggesting a lack of silicide formation at the substrate interface and Si–Zr bonding within the interfacial layer. True silicate bonding within the interfacial layer was not detectable from any of the scans (i.e., shift to lower binding energy with Si peaks and shifts to higher energies with Zr and O peaks). High resolution electron energy loss spectroscopy scans also show little or no Zr incorporation across the interfacial layer.[7]

Sputter depth profiling XPS was also performed with these samples. Top surface scans showed similar ZrO_2 bonding, however profiles of the interfacial layer showed both Si–O and Zr–O bonding suggesting a silicate or Zr-doped silica layer. This mixed bonding arrangement is possibly the result of nonuniform sputtering during the etching steps, further study is needed. Scans of the substrate also showed considerable Si–Zr bonding. We believe this latter signature to be an artifact of the Ar sputtering process considering the excellent electrical characteristics of the dielectrics, the lack of observed zirconium silicide formation during inert ambient anneals at temperatures up to 1000 °C, and the lack of silicide signatures in similar samples studied by medium energy ion spectroscopy (MEIS).[6]

Capacitance–voltage (*CV*) and leakage–voltage (*JV*) measurements were performed on 85×85 μm^2 capacitors using an HP4284A and HP4140B, respectively. The EOT values for the MOSCAP structures were calculated from the accumulation capacitance at −3 V without accounting for the quantum mechanical effect. Linear extrapolations were made to leakage as a function of EOT data for sets of ZrO_2 and SiO_2 samples, both with the same TiN/Al electrode. The resulting trends show an approximate five orders of magnitude improvement in the leakage between capacitors using SiO_2 and ZrO_2 at EOT values of 14–15 Å. Similar trends have been observed with ZrO_2 films deposited by reactive sputtering.[8] Figure 3 shows the 100 kHz *CV* and accumulation *JV* curves for a 50 Å ZrO_2 film deposited atop a 13 Å nitrided layer. These plots revealed an EOT value of 13.8 Å, along with a leakage current of approximately 10^{-5} A/cm^2 at 1 V less than flatband. The same film gave D_{it} values of $\sim1\times10^{12}$ states/cm^2 eV. Similar 50 Å ZrO_2 films deposited on a chemical oxide resulted in slightly higher EOT values due to the smaller permittivity and larger physical thickness of the interfacial layer. While the leakage values were similar to those samples deposited on the nitride layer, films deposited on the chemical oxide showed considerable improvements in D_{it} and hysteresis, as discussed shortly. The D_{it} value of $\sim3.1\times10^{11}$ states/cm^2 eV seen with the chemical oxide samples is expected to improve through use of conventional wet surface preparations and high-quality thermal oxidations. No significant frequency dispersion was seen with any of the samples.

The dielectric deposition was also scaled back to produce thinner ZrO_2 layers. Figure 4 shows the resulting electrical properties of gate stacks with 20, 35, and 50 Å ZrO_2 films. Extrapolating the EOT versus nominal ZrO_2 thickness function to zero suggests a dielectric constant for the interfacial layer of 6–7, which agrees with other ZrO_2 studies

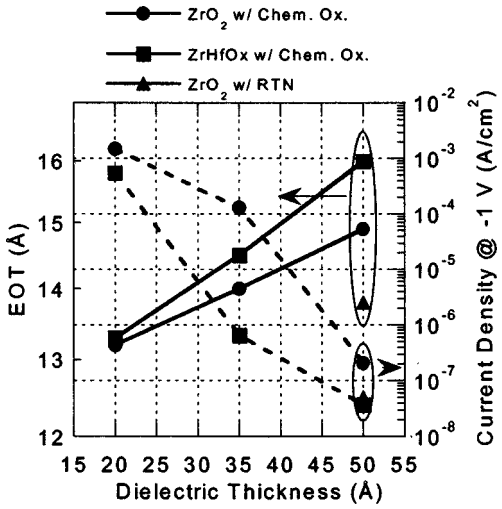

FIG. 4. Scaled EOT and leakage values for ZrO_2 and $ZrHfO_x$ films of varying nominal dielectric thickness.

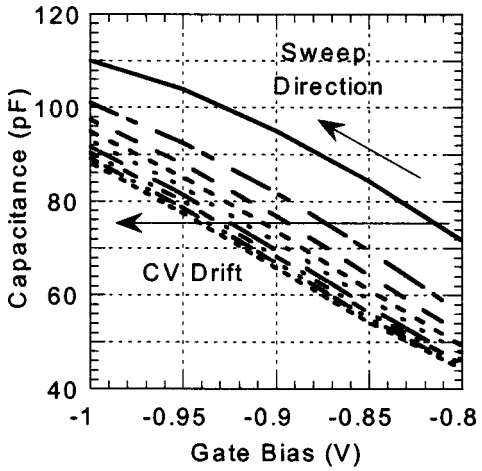

FIG. 5. Ten successive ±2 V sweeps show monotonic flatband shift (reverse sweeps not shown).

concluding the existence of a moderate *K*-valued interfacial layer.[8] This analysis of the data shown in Fig. 4 assumes that the interfacial layer is the same for all samples. Subject to this assumption, the dielectric constant of the ZrO_2 layer was estimated to be between 25 and 35. In a recent study of reactively sputtered ZrO_2, Busch *et al.* report that only 6 Å of the 10 Å interfacial layer in their samples can be attributed to pure SiO_2. These authors then mention that some intermixing (silicate) is likely present in their amorphous interfacial layer.[9] At this time, it is unclear how this layer achieves a moderate dielectric constant. However, the ability to produce a higher dielectric constant interfacial layer, while maintaining excellent electrical characteristics, is a key enabler of continued scaling of the gate dielectric.

Behavior similar to that of ZrO_2 was also shown for an oxide alloy of Hf and Zr, produced by alternating the metal precursor steps of $ZrCl_4$ and $HfCl_4$. The similarities of the two metal atoms and metal oxide crystal structures make possible crystalline ZrO_2–HfO_2 alloys. These films had slightly higher EOT values and lower leakage currents than non-alloyed ALCVD-grown ZrO_2 counterparts. Alloying may allow further optimization of future dielectric films, possibly in terms of crystallinity and leakage current minimization.

Hysteresis and stress-related ΔV_G shifts were measured to determine gate stack stability. Hysteresis in the *CV* curve is a primary indicator of flatband and threshold voltage stability due to trapping and/or detrapping of charge in the dielectric. The hysteresis is voltage dependent, with higher values resulting for larger voltage range sweeps. When the gate bias was swept between ±3 V, the hysteresis was approximately 70–90 mV for the samples with the chemical oxide layer. For ±2 V sweeps, the hysteresis decreased to 8–10 mV. Samples with the nitride layer produced similar trends with much larger values. The ±2 V sweeps resulted in hysteresis values of approximately 130 mV. We believe these high hysteresis values for samples with NH_3 RTN Si surface preparation were caused by elevated fixed charge and trapping resulting from the relatively large nitrogen content near the dielectric/substrate interface.[10] The stress-related ΔV_G shift is a measure of the drift in the *CV* characteristics after successive bias sweeps. As shown in Fig. 5 for a 20 Å ZrO_2 film deposited atop a chemical oxide, a shift of 120 mV is observed after 10 successive ±2 V sweeps (reverse sweeps not included for clarity purposes). This phenomenon may result from several factors such as chemical contamination, stress-induced defect formation, or mobile-ion transport. The last possibility seems unlikely since positive-voltage stressing does not shift the *CV* curves back in the positive-voltage direction. It is our belief that the ΔV_G shift is a strong function of the electrode used, and that it indicates a possible instability of the TiN/Al interface in contact with ZrO_2.

The authors would like to thank E. Garfunkel, M. Kelly, and P. Pianetta for helpful discussions. This work was supported in part by the NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing and Intel Corporation. One of the authors (C.P.) acknowledges the support of the Semiconductor Research Corporation through a graduate fellowship.

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