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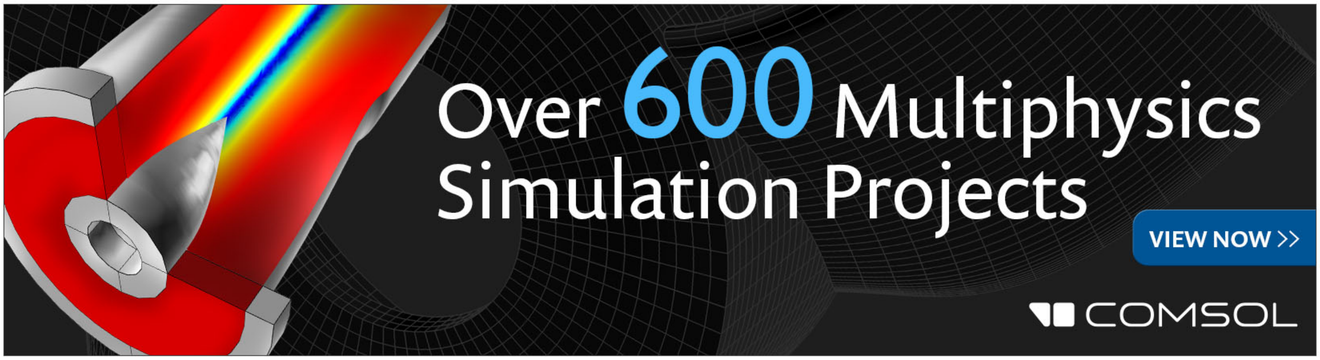

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Atomic-layer deposition of ZrO_2 with a Si nitride barrier layer

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ZrO_2 thin films for gate dielectrics have been formed at low temperatures (200 °C) by an atomic-layer deposition (ALD) technique using $Zr(t\text{-}OC_4H_9)_4$ and H_2O source gases. An ultrathin (physical thickness T_{phy} of ~0.5 nm) Si nitride layer was deposited on a Si substrate by ALD before the deposition of ZrO_2. Transmission electron microscopy showed that the Si nitride barrier layer successfully suppressed the formation of a SiO_2 interfacial layer. Because of the extremely uniform thickness control capability in the ultrathin region and the low thermal budget of the ALD process, the ALD process for the ZrO_2/Si nitride stack structure is a promising candidate for fabricating the ultrathin gate dielectrics for sub-0.1-μm complementary metal–oxide–semiconductor transistors. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1510584]

Recently, the substitution of conventional SiO_2 with a high-dielectric-constant thin film as the gate dielectrics for sub-0.1-μm metal–oxide–semiconductor field-effect transistors (MOSFETs) has received extensive attention.[1–9] The major reason is that the scaling down of the SiO_2 thickness is reaching its limit from the viewpoint of gate leakage current. One of the most promising candidates for the replacement of SiO_2 is ZrO_2, due to its high relative dielectric constant value ($\varepsilon_r = 20–25$),[4] its thermodynamic stability in contact with Si,[5] its large energy band gap (5.2 eV),[6] and small lattice mismatch of 2.1% with Si (100).[4]

Various methods have been proposed for the formation of ZrO_2 gate dielectrics such as sputtering[7,8] and chemical vapor deposition methods.[6,9] Recently, in view of film uniformity, thickness control capability in the small thickness region, and low thermal budget, the application of self-limiting atomic-layer deposition (ALD) is accelerating with apparently significant benefits in the fabrication of various gate dielectrics.[10–14] For the ALD of ZrO_2 gate dielectrics, the alternating exposure of $ZrCl_4$ and H_2O gases has most commonly been applied to date.[15,16] However, in the ALD using these source gases, ZrO_2 shows island-like growth when deposited directly on Si.[15] There is also a risk of Cl contamination and particle adhesion to the substrate surface because $ZrCl_4$ is in a solid state at room temperature. Zirconium tertiary-butoxide $[Zr(t\text{-}OC_4H_9)_4, (ZTB)]$ is one of the alternative Zr precursors with the highest vapor pressure, allowing evaporation at low temperatures. However, only a few reports[17] have been published regarding the ALD of ZrO_2 using ZTB as a gas source. In particular, the growth in the ultrathin region has not yet been examined.

On the other hand, it is well known that a chemical reaction between ZrO_2 and the Si substrate occurs during film deposition in oxygen ambient or oxygen-containing source gas ambient.[9,15] The growth of the interfacial oxide layer increases equivalent oxide thickness (EOT). To prevent this growth, it is efficient to form a thin barrier layer for oxygen indiffusion. In this study, we have formed an ultrathin ZrO_2 layer by ALD using ZTB and H_2O as source gases, and we report its structural characterization. We have also formed an ultrathin Si nitride layer by ALD between ZrO_2 and the Si substrate and found that it acts as an effective barrier against oxygen indiffusion.

The ALD of ZrO_2 layers was carried out by alternately supplying ZTB and H_2O gases on *p*-type Si (001) wafers (~10 Ω cm). The wafers were cleaned with an $NH_4OH:H_2O_2:H_2O = 0.15:3:7$ solution at 80 °C for 10 min and were terminated with hydrogen in a 0.5% HF solution, in order to suppress native oxidation before the ALD. ZTB exposure followed by H_2O exposure was cyclically repeated 2–15 times at the substrate temperature (T_{sub}) of 200 °C. The H_2O exposure time was 60 s. The vapor pressures of ZTB and H_2O during the deposition were controlled to 0.04 and 0.13–1.05 kPa, respectively. Just after the ALD, *in-situ* N_2 annealing was carried out for 5 min at 400 °C. In the ALD–ZrO_2/ALD–Si–nitride stack structure, about 0.5-nm-thick Si nitride was deposited by the ALD process using $SiCl_4$ and NH_3 gases.[13,14] The microstructure and thickness of the deposited film were investigated using transmission electron microscopy (TEM), employing a Hitachi HF-2100 field emission TEM operating at 200 keV.

Figure 1 shows the self-limiting properties of the film growth with ZTB exposure time. Vapor pressure of H_2O was 0.70 kPa. A ZrO_2 film thickness with five deposition cycles tends to saturate at ZTB exposure times longer than 60 s. The film thickness was measured by ellipsometry, under the assumption that the refractive index of ZrO_2 was 2.05.[4]

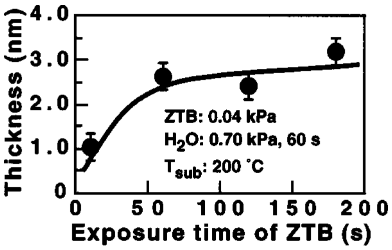

FIG. 1. Dependence of the ALD ZrO_2 film thickness on the ZTB exposure times after five deposition cycles. Vapor pressure of H_2O was 0.70 kPa.

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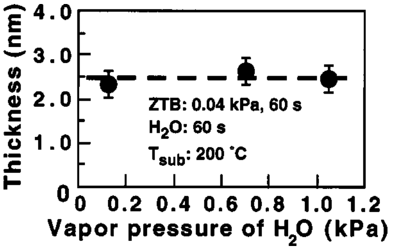

FIG. 2. Dependence of the ALD ZrO_2 film thickness on the H_2O vapor pressure after five deposition cycles. ZTB exposure time was 60 s.

Figure 2 also shows the self-limiting properties of the film growth with vapor pressure of H_2O. A saturated film thickness of about 2.5 nm was achieved with five deposition cycles from around 0.1 to 1.05 kPa, which is consistent with the result for ZTB exposure time of 60 s shown in Fig. 1.

Figure 3 shows the thickness of the ALD ZrO_2 as a function of the number of deposition cycles. The deposited thickness is in linear relation with the number of deposition cycles although some offset thickness occurred. This offset thickness is about 1.5 nm and is considered to be due to the presence of the interfacial oxidized Si layer. The interfacial layer is also observed by TEM measurements [Fig. 5(a)]. From the slope of the linear line in the figure, the growth rate is estimated to be about 0.2 nm/cycle. One monolayer of amorphous ZrO_2 is estimated to be ~0.2 nm thick since the Zr–O distance is obtained to be 0.22 nm from the ionic radius.[18,19] Therefore, it is indicated that the layer-by-layer growth of ZrO_2 takes place in our experiment.

Figure 4(a) shows the x-ray photoelectron spectroscopy (XPS) spectra of the Zr_{3d} core level for ALD ZrO_2 deposited under 0.70 kPa H_2O vapor pressure. It shows a strong signature of typical ZrO_2 bonding, namely, the shifted Zr_{3d} oxide doublet at 182.3 and 184.7 eV.[9,20] Figure 4(b) shows the Si_{2p} signal of the film. The Si_{2p} peak at 102.4 eV indicates the existence of Si–O bonds in the interfacial layer. The separation between oxidized and unoxidized Si signals is 2.9 eV, which is lower than the ~4 eV measured for SiO_2 on Si.[21] This indicates that the interfacial Si oxide is substoichiometric.

Figure 5 shows a high-resolution cross-sectional TEM micrograph of the formed films. It is shown in Fig. 5(a) that ALD ZrO_2 has an amorphous structure even after annealing at 400 °C. Uniform thickness of ALD ZrO_2 is observed. The thickness of the interfacial layer is observed to be ~1.2 nm. Considering the ambiguity of the boundary between the interfacial layer and ZrO_2 in the TEM micrograph, the observed interfacial layer thickness is consistent with the offset thickness in Fig. 3. Figure 5(b) shows the ALD–ZrO_2/ALD–Si-nitride stack structure. In this sample, annealing at 850 °C for 3 min in N_2 ambient was added to 400 °C annealing. For the 850 °C-annealed sample, crystallized ZrO_2 is observed. With this crystallization, the surface of the ZrO_2 becomes rough. A noteworthy feature is that a smooth interface was observed between the ZrO_2 and Si nitride layers. The growth of the interfacial Si oxide layer is observed to be suppressed. This is understood from the fact that the thickness of the interfacial amorphous layer (~0.5 nm) coincides with that of the initially deposited ALD Si nitride.

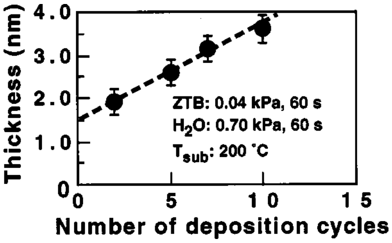

FIG. 3. Thickness of ALD ZrO_2 versus number of deposition cycles. The thickness of ZrO_2 was measured by ellipsometry. ZTB exposure time was 60 s. H_2O vapor pressure was 0.70 kPa.

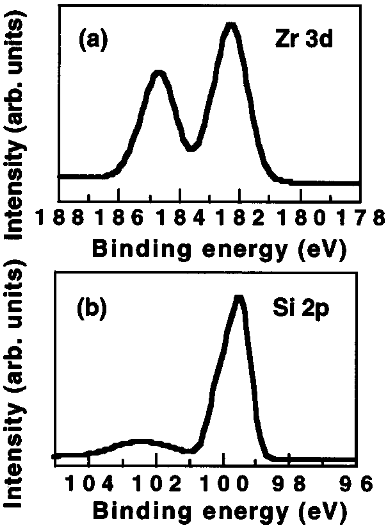

FIG. 4. XPS spectra of the (a) Zr_{3d} and (b) Si_{2p} core levels for the ALD ZrO_2. Number of deposition cycles was 5. ZTB exposure time was 60 s. H_2O vapor pressure was 0.70 kPa. Take-off angle was 90°.

Figure 6 shows the capacitance–voltage ($C-V$) curve of

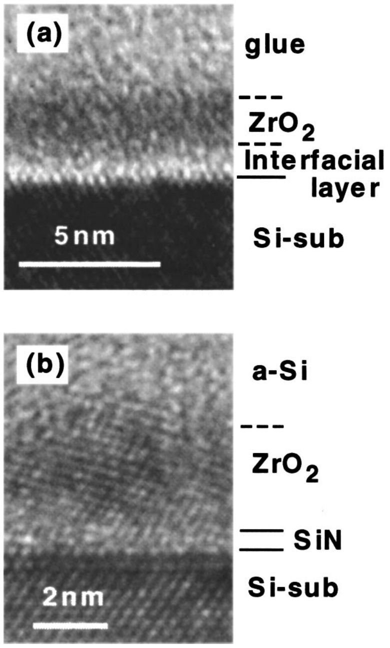

FIG. 5. High-resolution cross-sectional TEM micrograph of (a) ALD ZrO_2 and (b) ALD–ZrO_2/ALD–Si-nitride stack films. ZTB exposure time was 60 s. H_2O vapor pressure was 0.70 kPa. For the stack film, 850 °C annealing was added for 3 min after the ALD and the annealing (400 °C for 5 min) of ZrO_2. Number of deposition cycles of underlying ALD Si nitride was 2 ($T_{phy} = \sim 0.5$ nm).

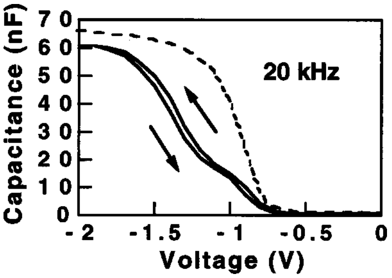

FIG. 6. $C-V$ characteristics at 20 kHz for ALD–ZrO_2/ALD–Si–nitride capacitor (solid lines). Number of deposition cycles was 15 and 2 for ZrO_2 and Si nitride, respectively. ZTB exposure time was 60 s. H_2O vapor pressure was 0.70 kPa. The calculated $C-V$ curve (broken line) is also shown using the doping level of the Si substrate and the work function of the Al gate.

an Al/ALD–ZrO_2/ALD–Si–nitride capacitor measured at 20 kHz. The number of deposition cycles of ZrO_2 was 15. The observed hysteresis ($\Delta V_{FB} = 50$ mV) is considered to be due to charge trapping in ZrO_2 and/or the ZrO_2/Si–nitride interface. The damage that occurred during Al sputtering for electrode formation is also a possible reason because we did not carry out postmetallization annealing after sputtering. The EOT value of the stack dielectrics is obtained to be 1.6 nm from the comparison with the calculated capacitance (broken line) for SiO_2 dielectrics. The physical thickness (T_{phy}) is observed to be 4.7 nm from TEM for the stack film. T_{phy} consists of the ZrO_2 layer ($T_{phy} = 4.2$ nm) and the underlying Si nitride layer ($T_{phy} = 0.5$ nm). Taking these T_{phy} values into account, the ϵ_r value of the ALD ZrO_2 layer is obtained to be 12. In comparison with the calculated curve (broken curve), the interface trap density D_{it} was estimated to be about $5 \sim 4 \times 10^{12}$ cm^{-2} eV^{-1} between 0.1 and 0.3 eV above the valence band edge. Also, the density of the positive fixed charge was estimated to be 5×10^{12} cm^{-2} from the flatband voltage shift. Details of the electrical properties including leakage current will be reported elsewhere.

In summary, ultrathin ZrO_2 films were successfully formed by alternately supplying ZTB and H_2O gases. Self-limiting properties of film growth with ZTB exposure time and H_2O vapor pressure were achieved at a growth temperature of 200 °C. The deposited ZrO_2 was amorphous when annealed at 400 °C in the N_2 ambient. Good smoothness at the surface of ALD ZrO_2 was obtained. XPS spectra showed that the formed film consists of ZrO_2. TEM observation showed that the Si nitride barrier layer successfully suppressed the formation of the Si oxide interfacial layer. Because of an extremely uniform thickness control capability in the ultrathin region and the low thermal budget of the ALD process, the ZrO_2/Si–nitride stack structure formed by the ALD process is a promising candidate for the ultrathin gate dielectrics of sub-0.1-μm complementary metal–oxide–semiconductor transistors.

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