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Metal nanocrystals synthesized with a micellar template based on a diblock copolymer for three-dimensional nonvolatile memory

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Metal nanocrystals synthesized with a micellar template were applied for three-dimensional vertical floating gate memory devices. Using a highly ordered micellar template formed with a diblock copolymer, we produced cobalt (Co) nanocrystals with a uniform size and spatial distribution on a planar surface and a sidewall surface. The hydrogen annealing effects were investigated in terms of memory performance. The fabricated vertical floating gate memory with Co nanocrystals annealed with hydrogen showed a memory window with a voltage greater than 1 V and a retention time characteristic that preserves more than 60% of the initial charge after ten years. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2969051]

On behalf of the rapid growing nonvolatile memory (NVM) technology, flash memory device is in great demand on account of their high density memory. This demand has been accelerated by the advent of mobile device and the increase of multimedia data amount. As the scaling down of device becomes accelerated, some critical issues are unavoidable, such as limitations in the downscaling of a tunneling oxide thickness and cell-to-cell crosstalk. To break through the innate limitations of conventional flash memory with a continuous polycrystalline silicon layer, profound research on nanocrystal (NC)-embedded memory has been proposed,[1] and the latest research is concentrated on metal NC. Metal NC has many advantages over Si NCs, which were mainly studied in the early stage of NC-embedded memory research.[2] Recently, polymeric template-assisted methods have been proposed for the formation of metal NCs. Based on self-assembled porous template using phase separation, these methods aim to circumvent the variation problem with the cell-to-cell threshold voltage (V_T). The variation problem is due to the nonuniform size and distribution of NCs at the time of the scaling down.[3–5]

In spite of such advanced methods of NC formation, the fundamental physical limitations on effective gate length, tunnel oxide thickness, and drive current are not eliminated in a conventional memory cell that uses a planar structure.[6,7] One way of overcoming these limitations is to use three-dimensional (3D) devices that can suppress short-channel effects through structural change.[7–10] Because conventional methods of NC formation are unsuitable for 3D devices with a double gate and triple gate structure, few studies have examined silicon NCs formation, and there appears to be no research on the controlled formation of single-layered metal NCs with a vertical sidewall structure.[11,12] Finding a method that can make uniformly distributed metal NCs on a sidewall surface and on the top surface is crucial for achieving 3D multiple-gate NVM for ultimate scaling.

Thus, the fabrication and characterization of 3D vertical floating gate memory with metal NCs are presented in this work for ultimately scaled NVM. The aforementioned polymeric template assisted method is suitable only for a planar structure. However, in our dipping method, we use a micellar structure based on a diblock copolymer as a sacrificial template. Through adjustment of the dip coating condition, reversed micelles based on a block copolymer can be coated as a Langmuir–Blodgett monolayer film on any preferred region of the substrate, and these reversed micelles are rearranged in a hexagonal-ordered form due to the equal size of each micelle. Moreover, we can easily and precisely manipulate the NC diameter and NC-to-NC space by modulating the molecular weight in a core block and in the shell block that surrounds the core block.[13] Note also that we investigated how hydrogen annealing for metal reduction affects memory performance.

Figure 1 shows a schematic diagram of the fabrication of a single-layered array of Co NCs on a 3D vertical floating gate memory cell with utilization of block copolymer micelles. Polystyrene-block-poly(4-vinyl pyridine) (PS-PVP) copolymers were purchased from Polymer Source, Inc. The average molecular weight was 32 900 g/mol for the PS and 8000 g/mol for the PVP. The polydispersity index was 1.08. The PS-PVP copolymers were dissolved in toluene at 75 °C to yield a 0.5 wt % micellar solution, which was then cooled down to room temperature [Fig. 1(a)]. In the toluene, which is a strongly selective solvent for the PS block, the PS-b-PVP copolymers spontaneously associated into spherical reverse micelles of a nonpolar PS corona and a polar PVP core. To synthesize the Co NCs, we selectively loaded the precursor cobalt chloride into the PVP core [where the molar ratio of $CoCl_2$/vinyl pyridine was 0.5, Fig. 1(b)] because cobalt chloride, a transition metal salt, can be coordinated to the lone-pair electron of the pyridine unit in the PVP block.[14,15] From the PS-PVP micellar solution with $CoCl_2$, a single layer of the micelles in hexagonal order was coated on the vertical floating gate memory cell by dip coating at a rate of 20 mm/min. As shown in the schematic diagram of Fig. 1(c), a

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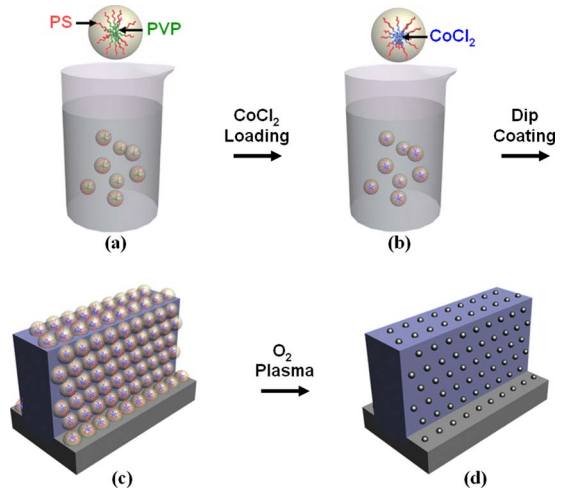

FIG. 1. (Color online) A schematic illustration of NCs fabrication on the sidewall and top of the vertical floating gate memory. (a) PS-PVP micellar solution. (b) PS-PVP micellar solution with $CoCl_2$ in the PVP core. (c) Monolayer of PS-PVP micelles coated on the sidewall and top. (d) Array of NCs on the sidewall and top surface.

single layer of PS-PVP micelles with $CoCl_2$ was covered not only on the top surface but also on the sidewall of the pattern because the dip coating of the block copolymer micelles allowed a conformal coating on every surface of the patterned substrate. The monolayer of micelles coated on the pattern was treated with oxygen plasma for 10 min, resulting in the formation of a single-layered array of cobalt oxide NCs on the top and on the sidewall. During the formation process, the micellar arrangement was preserved and the organic copolymer micelles were removed [Fig. 1(d)]. Because pure metallic Co has a higher charging efficiency than Co oxide, we conducted hydrogen annealing at 400 °C for 1 h to reduce the Co NCs.[15,16]

For the device fabrication, we used a ⟨100⟩ *p*-type silicon-on-insulator wafer. The wafer has a top silicon layer of 230 nm with a resistivity of 10–20 Ω cm on the 380 nm thick buried oxide layer. Initially, we deposited a 100 nm thick hardmask layer of high density plasma (HDP) oxide to investigate the effect of the NCs on the sidewall only without effect of the NCs on the top. The active region was defined by anisotropic reactive ion etching (RIE) to obtain a vertical sidewall profile with the hardmask. To alleviate the surface of the sidewall damaged by the RIE, we used diluted hydrogen fluoride (HF) for the iterative sacrificial oxidation and etching. Then, a 4.5 nm layer of tunneling oxide was thermally grown. For the storage node, the Co NCs were synthesized on the tunneling oxide according to the micellar processes. A 30 nm thick layer of HfO_2, a control oxide, was then deposited by plasma-enhanced atomic layer deposition and a 300 nm thick layer of Cr was deposited as a gate electrode by means of dc sputtering. The Cr gate and the control oxide were wet etched in sequence. To make a source/drain region and minimize the lateral straggle of dopants, we used RIE to remove the revealed HDP hardmask after the control oxide etching. Instead of using a conventional ion implant, we used a plasma immersion of phosphorous ion to produce a shallow and uniform source/drain profile. Additionally, the plasma immersion method has the advantage of avoiding a high thermal budget, which can melt metal NCs, for electrical dopant activation and diffusion into

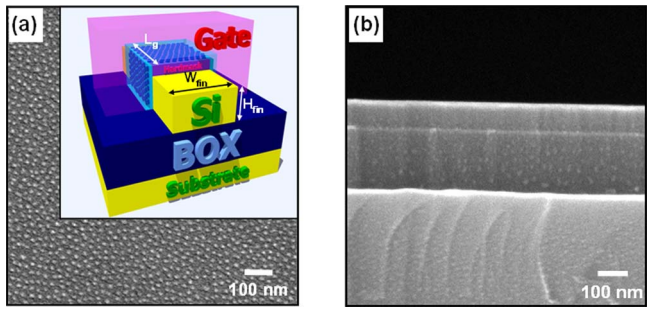

FIG. 2. (Color online) A SEM image of Co NCs on (a) the top surface and (b) the sidewall surface. The inset shows a 3D schematic diagram of the 3D vertical floating gate memory with NCs on the sidewall and the top.

an exposed whole Si surface.[17] Finally, the forming gas was performed for 1 h at 400 °C.

The inset of Fig. 2(a) shows a 3D schematic diagram of the fabricated vertical floating gate memory device. The fabricated device structure is the same as a conventional fin-shaped field electronic transistor except for a wide fin. A scanning electron microscopy (SEM) image of the top surface of the device in Fig. 2(a) shows that the NC has a size of about 9 nm and a density of $2.4\times10^{11}/\mathrm{cm}^2$. A comparison of SEM images confirms that the NCs are formed well even on the sidewall. As shown in Figs. 2(a) and 2(b), the NCs have the same size and distribution on the sidewall as on the top.

Figure 3(a) shows the memory characteristics of the vertical floating gate memory device induced from ±11 V for 100 ms pulse of programing and erasing. The device without NCs shows a negligible V_T shift; thus, it confirms that the V_T shift is due solely to the Co NCs. It should be noted that the

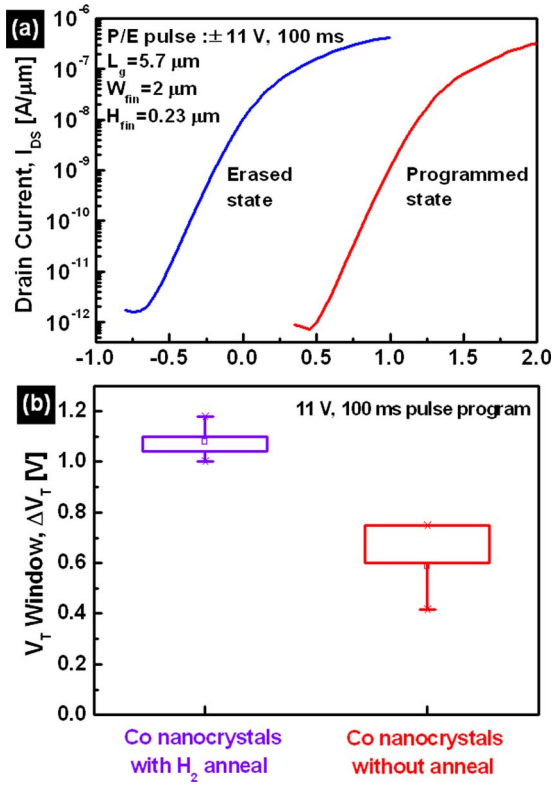

FIG. 3. (Color online) (a) The memory characteristics of the fabricated vertical floating gate memory device with pulses of ±11 V for 100 ms for the program/erase operations. (b) The effect of hydrogen annealing on memory performance. The programing pulse was 11 V for 100 ms.

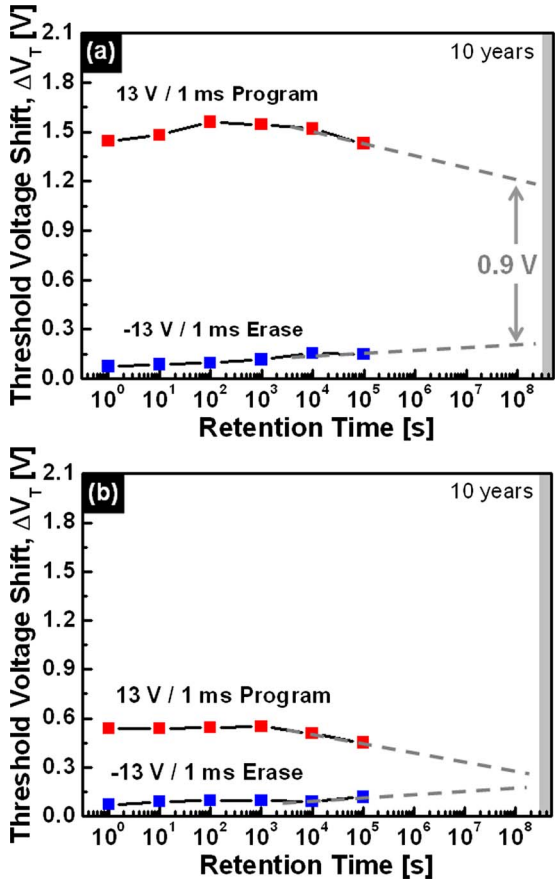

FIG. 4. (Color online) The measured data retention characteristics of the vertical floating gate memory devices (a) with and (b) without hydrogen annealing at room temperature after the application of a pulse of 13 V for 1 ms.

V_T shift was caused only by the NCs on the sidewall because of a thick hardmask oxide on the top surface. Figure 3(b) shows the hydrogen annealing effect on memory performance. Because the charge trapping efficiency on the metallic NCs is better than that on the metal-oxide NCs, the V_T window of the device with the metallic Co NCs reduced by hydrogen annealing is bigger than the V_T window of the device with the Co-oxide NCs.[15]

Figures 4(a) and 4(b) show the retention time characteristics of the device with hydrogen annealing and without hydrogen annealing after the application of a pulse of 13 V for 1 ms at room temperature. The device with the hydrogen annealing preserves more than 60% of the initial V_T difference for up to ten years, which is the required minimum data retention time of a good nonvolatile characteristic. However, the device without hydrogen annealing shows a greater charge loss characteristic and a worse retention time.

In summary, we have demonstrated the 3D vertical floating gate memory device with Co NCs synthesized by means of a reversed micelle structure based on a diblock copolymer. A uniform NC size and spatial distribution were achieved on both the sidewall and the top through the use of a monolayered micelle structure formed by means of the dipping method. In addition, the NC diameter and NC-to-NC space can be separately controlled by modification of the molecular weight of each core-shell block. Because metallic Co NCs have a better charge-trapping efficiency than Co-oxide NCs, the fabricated device with hydrogen annealing shows a wide memory window and a prolonged retention time, which preserves more than 60% of the initial charge after ten years. This research highlights the potential of using a 3D vertical floating gate memory device with metal NCs through a polymeric template in scaled-down devices.

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