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Selective Electroless Metal Deposition for Via Hole Filling in VLSI Multilevel Interconnection Structures

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ABSTRACT

Selective electroless metal deposition process is investigated for via hole filling to provide a planar surface for the fabrication of high density multilevel interconnections. The substrates used in this work consisted of a 1.0 μm thick Al layer covered with 1.0-1.5 μm thick CVD silicon dioxide layer. Via holes of 1.5 μm nominal size are formed in the oxide layer by plasma etching. Selective deposition of Ni is achieved by first activating the Al surface in a Pd solution, Ni is then deposited on the activated surface from an aqueous solution using dimethylamineborane or hypophosphite as reducing agents. Pd can be selectively deposited directly on the Al surface without the need of surface activation. Either hypophosphite or hydrazine is used as the reducing agent in the Pd deposition solution. Cobalt can also be selectively deposited to fill the via holes. The filled via holes can have almost perfectly planar surface. Good contact resistance has been obtained by measuring the via chain resistance.

Multiple layers of conductors are needed to interconnect the large number of devices contained in a single VLSI (very large scale integration) chip. The surface topography created by multiple deposition and etching steps in fabricating the interconnection patterns presents a serious problem for subsequent processing. One of the most challenging issues is the step coverage at via holes because the via holes are not only small in size, but also have nearly vertical sidewalls. Therefore, a via hole filling process is indispensable to achieve a high density multilevel interconnection structure. Selective CVD (chemical vapor deposition) tungsten has been studied extensively for via hole filling (1). While much progress has been made, the selective CVD W process still has many issues. In this work, the selective electroless metal deposition process was studied for via hole filling (2, 3) as an alternative to the selective CVD W process. The selective electroless deposition process may provide an attractive alternative to the CVD process because it is a versatile, low temperature, and potentially very low cost process.

Experimental

Substrate preparation.—The substrates used in this study are thermally oxidized 100 mm diam silicon wafers. A 1.0 μm thick Al (with 1% Si) layer is deposited on the wafer surface by a conventional sputtering process. The Al layer is patterned with standard photolithography and plasma etching process. The minimum pitch of the metal pattern used in this work is 5 μm. A dielectric layer of 1.0-1.5 μm thick undoped oxide is deposited over Al by a low temperature CVD process (LTO). Via holes of 1.5 μm nominal size are formed in the LTO layer using standard photolithography and plasma etching process. The photoresist is then stripped with either a solvent or by an oxygen plasma. These wafers are then used to study via hole filling using selective deposition of electroless Ni, Co, or Pd. For contact resistance measurements, a second Al-Si layer is deposited on the wafers after via filling. No special cleaning processes were used to clean the filled via surface before the second Al deposition. The second Al layer is then patterned using standard processes followed by a 450°C nitrogen anneal. The via chain resistance is determined by standard electrical measurements.

Palladium activation process.—Nickel is selected for via filling studies because there is a lot of information already available on electroless Ni deposition (4). Aluminum surface is, however, not catalytic to Ni deposition, therefore a surface activation step is necessary. Many different Pd solutions have been tested for Al surface activation (5, 6). The composition of a Pd activation solution that gives good selectivity between Al surface and oxide surface is given in Table I. The sample is first cleaned by dipping in diluted HF for a few seconds followed by DI water rinse. The sample is then immersed in the Pd activation solution for a few seconds and rinsed in DI water. Electroless Ni can then be selectively deposited on the activated Al surface without any deposition on the oxide surface. The excellent

Table I. Composition of a Pd activation solution

$PcCl_2$	0.2g
HCl	1 ml
Glacial acetic acid	500 ml
HF (50:1)	250 ml
H_2O	245 ml

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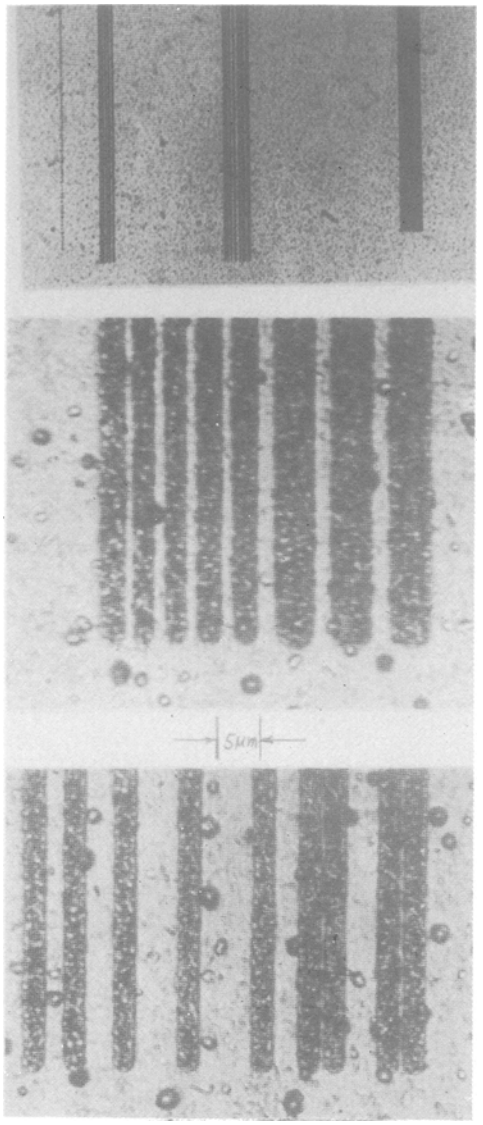

Fig. 1. Demonstration of good selectivity: (a, top) over view of the test patterns, (b, center) approximately 1 μm gap between two deposited lines, and (c, bottom) submicron gap between two deposited lines.

selectivity achieved by this process is illustrated in Fig. 1. Figure 1a shows the overall view of test patterns with various line and space dimensions. Figure 1b is the magnified view of the first test structure (from the right side). The minimum spacing between two deposited lines is approximately 1 μm. Figure 1c is the magnified view of the second test structure where submicron spacing between two lines is maintained in this selective activation and deposition process.

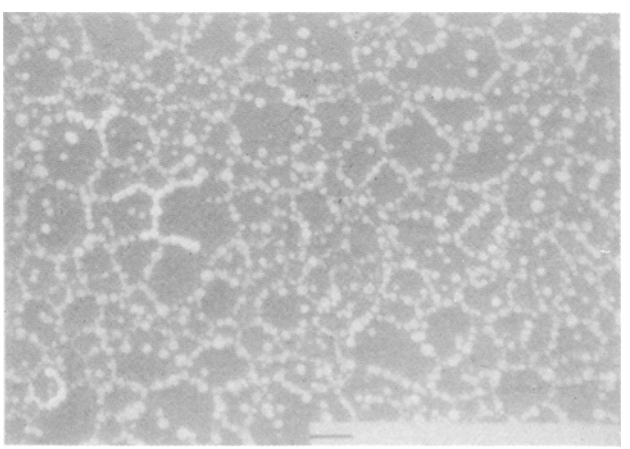

Fig. 2. Al grain boundaries decorated by Pd deposits

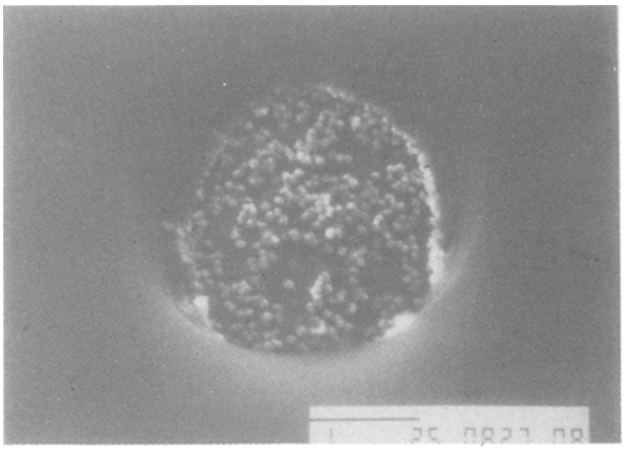

Fig. 3. SEM photo of a Pd activated via hole

The Al surface is not ideal for the selective metal deposition process because its surface is not uniform. The Al surface is covered with a native oxide layer, and it is very rough due to hillock formation during CVD deposition of SiO_2. Hillocks of several microns in size can be seen in Fig. 1. The aluminum surface also has grain boundaries. Pd deposition tends to congregate on these boundaries, as illustrated in Fig. 2. The Pd deposition solution used in Fig. 2 has been adjusted to give heavier deposits than that normally used in activating Al surfaces in order to accentuate this effect. Even with the considerable variations in Al surface, uniform activation can still be obtained in the via holes with properly adjusted activation conditions. Figure 3 shows one of the via holes after proper Pd activation.

Results and Discussion

Nickel deposition process.—Selectivity in electroless Ni deposition into via holes depends not only on the Pd activation process, but also on the compositions of the electroless Ni deposition solution. The composition of a typical Ni deposition solution is given in Table II (4). With this solution, a deposition rate of approximately 3 μm/h is obtained at 58°C. The exact formulation of the deposition solution must be adjusted to fit not only the Pd activation process, but also for a specific Al surface condition. The Al surface condition was found to be dependent on the processing or thermal history of the wafer. For example, a blanket Al surface seems to behave differently from a patterned Al surface which has gone through photoresist and plasma etching process. The Al surface is also influenced by the via hole plasma etching process. Different photoresist stripping processes after via hole etching, such as wet solvent stripping or dry oxygen plasma stripping, change the Al surface sufficiently to require different optimization of the activation and the deposition processes. Unless

Table II. Composition of a Pd activation solution

$NiSO_4\ 6H_2O$	40 g/liter
Sodium citrate	20 g/liter
Lactic acid	10 g/liter
DMAB	2 g/liter
NH_4OH	Adjust pH to 6.0

Table III. Composition of an electroless Pd deposition solution

$PdCl_2$	1-4 g/liter
HCl	1-5 ml/liter
NH_4OH	200-400 ml/liter
NH_4Cl	5-10 g/liter
$NaH_2PO_2H_2O$	1-5 g/liter

Table IV. Composition of an electroless Co deposition solution

$CoSo_4 \cdot 7H_2O$	10-25 g/liter
Sodium succinate ($6H_2O$)	25-50 g/liter
$Na_2SO_4 \cdot H_2O$	10-15 g/liter
DMAB	4 g/liter
pH	5-7

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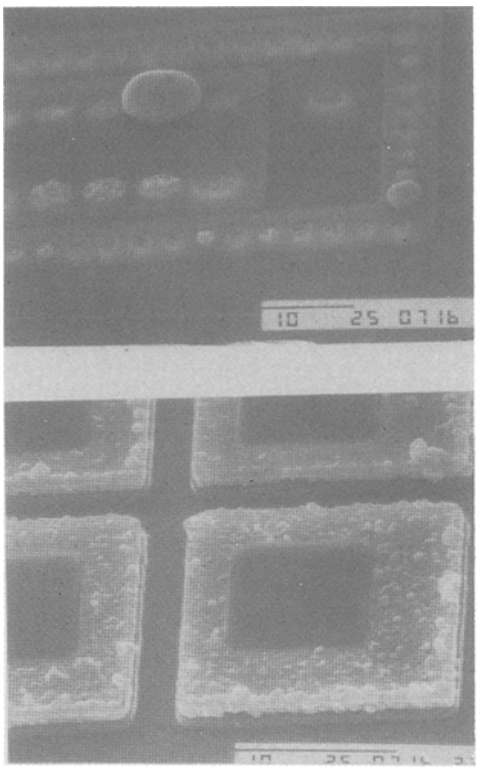

Fig. 4. Typical problems encountered in poor via filling process: (a, top) unfilled vias and nodules, (b, bottom) extraneous deposition.

these processes are fine tuned to suit specific surface conditions, uniform via fillings cannot be obtained. Some of the common problems encountered are unfilled or significantly underfilled vias, nodules or significantly overfilled vias, and extraneous deposits near the edge of a large pattern. These problems are illustrated in Fig. 4. Figure 4a shows the unfilled vias and nodules together with some properly filled vias. Figure 4b shows the extraneous deposit near the edge of a large pattern. However, when the process is properly tuned for the surface conditions, uniformly filled vias can be obtained as illustrated in Fig. 5. Figure 5a shows a 1.5 μm via hole array in low magnification while Fig. 5b is a high magnification SEM photo to show that individual via holes are properly filled. In this sample, hypophosphite was used as a reducing agent (7, 8).

Palladium deposition process.—Since the Al surface is catalytic to Pd deposition, a simplified via filling process can be obtained by depositing electroless Pd directly without any activation step (9). A typical electroless Pd deposition solution is given in Table III. Even though sodium hypophosphite is specified as a reducing agent in Table III hydrazine can also be used. The reason to use hydrazine as a reducing agent is because it can give very pure deposits as compared to hypophosphite which incorporates some phosphorous into the deposited Pd (7). The Pd deposition solution with hydrazine as reducing agent is a strong base (*p*H ~13) which attacks the Al significantly. As a result, the deposited Pd will protrude into the original Al surface. A SEM cross-sectional view of Pd filled via on 1.0 μm thick Al is shown in Fig. 6. The extension of Pd deposit into the Al surface can clearly be seen. This is not a problem for relatively thick Al layer (~1.0 μm) but may not be acceptable for very thin Al layer (<0.5 μm) since the protrusion may extend through the entire thickness of the thin Al layer.

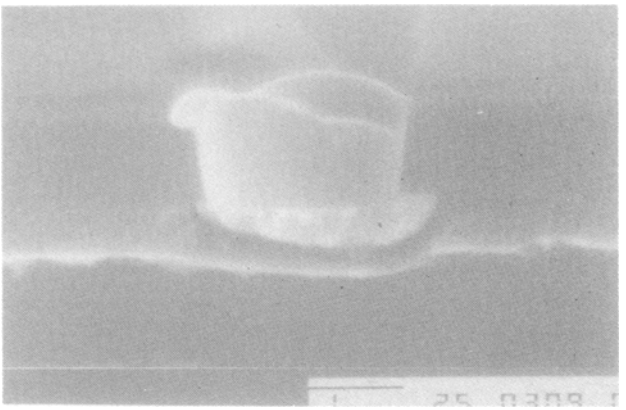

Fig. 6. SEM cross section of a Pd filled via hole

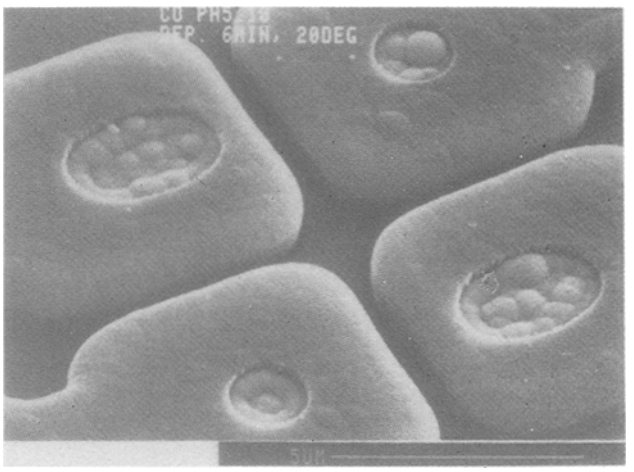

Fig. 7. Co-filled via hole

Cobalt deposition process.—Cobalt can also be used to fill the vias selectively. The Co deposition process is similar to that of Ni deposition process. It also requires a surface activation step, and the Pd activation solution given

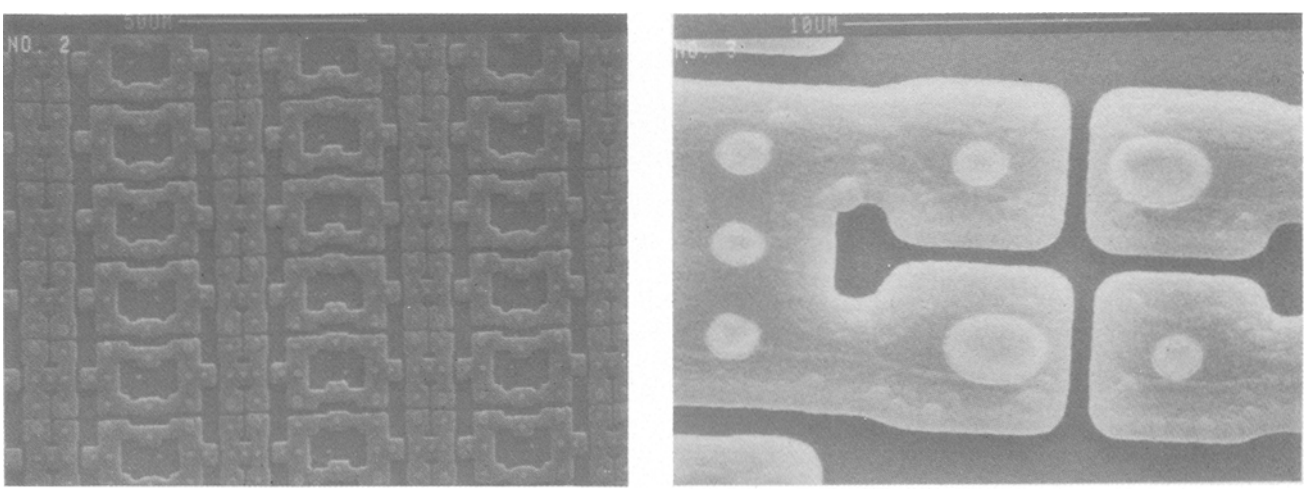

Fig. 5. Properly filled via array: (a, left) low magnification photo, (b, right) high magnification SEM photo of individual vias

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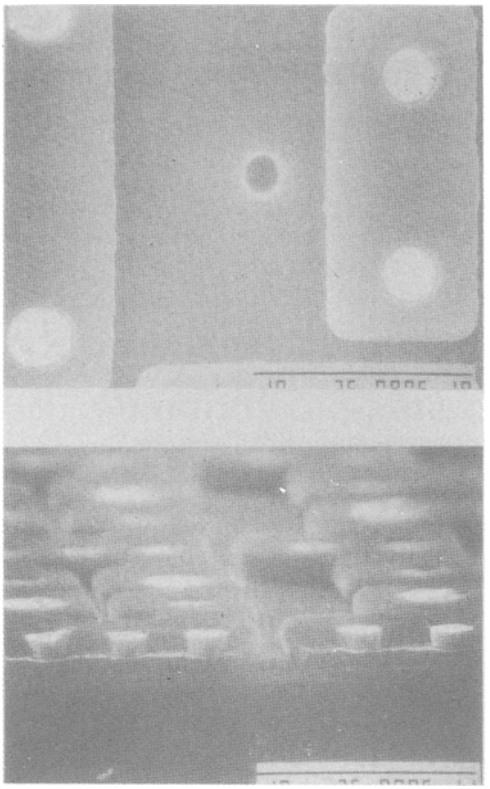

Fig. 8. Ni-filled via over first Al pattern: (a, top) top view, and (b, bottom) cross section.

in Table I can again be used for activation. The composition of a typical Co deposition solution is given in Table IV (10). Good via filling obtained with the Co process is illustrated in Fig. 7. The relative merits between Ni and Co for via filling are not clear at the present time.

Via chains and via resistance.—Via chains are formed by two Al layers. The first level Al pattern is connected to a second level Al pattern through a via hole, then the second level Al pattern is connected to another first level Al pattern through a second via hole. A via chain pattern of any desired length can be formed by repeating this structure. In this work, the via holes are filled with selectively deposited electroless Ni (P) before the deposition of second Al layer. Figure 8 shows the wafer surface after via holes are filled. Figure 8a is the top view of the filled vias of 1.5 μm nominal size. Figure 8b gives the cross section of these structures. In Fig. 8 the first layer Al used is 1.0 μm thick and the undoped CVD glass layer is also 1.0 μm thick. As can be seen from Fig. 8b, these vias are almost filled to the top surface to give a nearly planar surface. This should be compared to the severe topography in the dielectric surface at the edge of the Al pattern. Part of the completed via chain after the patterning of second Al layer is shown in Fig. 9. The total chain length has 1080 vias. The resistance of the chain was measured by electrical probing; the measured resistance is very high before annealing, however, after a 450°C nitrogen annealing cycle resistance value of less than 100 mΩ per via has been obtained. This corresponds to a specific via resistivity of less than 1×10^{-9} Ω-cm^2, a very low value.

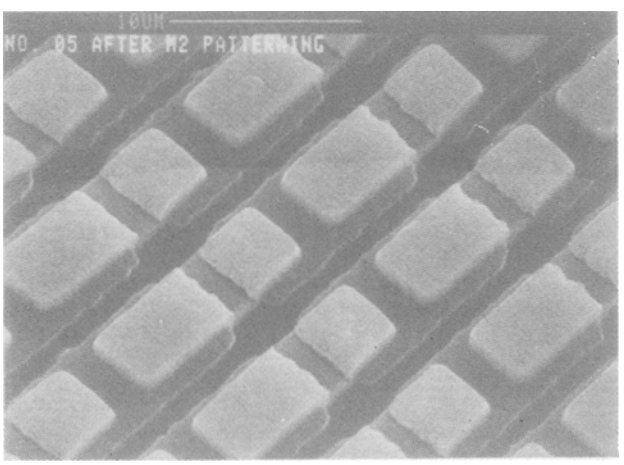

Fig. 9. Part of the complete via chain structure

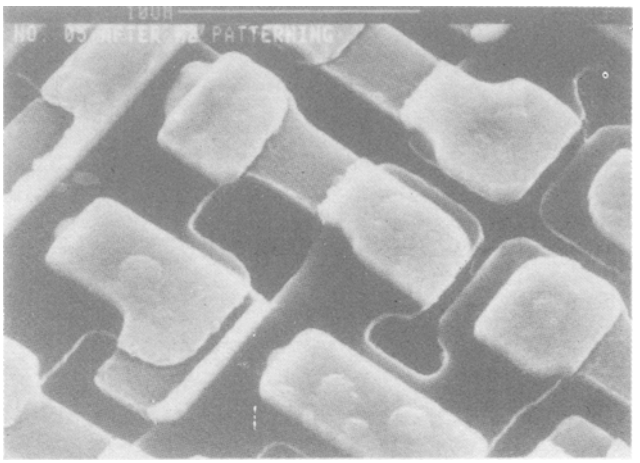

Fig. 10. Partially exposed Ni filled via holes after Al patterning

By using Ni filled vias, the patterns in second Al layer are no longer required to cover the via holes completely. This is illustrated in Fig. 10. In Fig. 10 the second Al pattern is misaligned significantly thus exposing Ni and some via holes to the Al etching process. Since the Al plasma etching process does not attack Ni significantly, there is no observable change in the exposed Ni. This is a very important advantage in using Ni-filled via other than surface planarity. By eliminating the overlap requirement between the second Al pattern and the via hole pattern, significant compaction can be realized in the conductor layout.

Summary

Selective electroless metal deposition process has been studied for via hole filling in VLSI multilevel interconnection structures. Suitable processes for Pd activation and electroless deposition of Ni, Pd, and Co have been developed. Although not reported here, alloys have also been successfully deposited into the via holes. The Al surface condition was found to be dependent on the processing and thermal history of the wafer such as resist stripping process. The activation and the deposition processes can be modified to suit different Al surface conditions to give good uniformity and selectivity in filling via holes. Long via chains were fabricated using Ni filled vias. Ni-filled vias with a nearly planar surface was obtained. Good contact resistance was measured after 450°C annealing. Since only test structures were fabricated using this via filling process, more work is needed to establish its compatability with the actual device fabrication process.

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Elimination of End-of-Range Shallow Junction Implantation Damage during CMOS Titanium Silicidation

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ABSTRACT

Interstitial dislocation loops present in shallow junctions formed following Ge preamorphization (85 keV, 1×10^{15} cm^{-2}) and rapid thermal annealing have been eliminated using titanium silicide. The dissolution of these end-of-range defects is attributed to the injection of vacancies during silicidation. The size and number of the residual extended defects were reduced in both p^+ and n^+ junctions after the formation of $TiSi_2$. The silicide sheet resistance is a measure of the amount of silicide reaction and concomitant vacancy injection. The total elimination of these defects was observed in shallow p^+ junctions for sheet resistance of $TiSi_2$ below 3 Ω/□. Leakage current reduction in silicided p^+/n junctions, was correlated with the defect reduction.

Preamorphizing single-crystal silicon with ion implantation prior to junction implantation has been shown to be a promising technique for forming shallow junctions for VLSI CMOS (1-6). This preamorphization prevents channeling and offers the potential of reducing the junction depth. Nevertheless, following dopant activation via solid-phase epitaxial (SPE) regrowth, a zone of interstitial dislocation loops remains near the amorphous/crystalline interface due to residual end-of-range damage from the heavy amorphizing ion. Complete removal of ion implantation induced defects after dopant activation is a serious concern in producing junctions with low leakage current. A second serious concern with shallow junction technology is the high junction sheet resistance that results from the limited dopant solubility in silicon. Cladding the junction regions with a highly conductive metal silicide has been widely accepted as one technique to reduce resistance. Recently, the generation of excess vacancies by a reaction of a refractory metal and silicon has been reported (7-11). For many refractory metals, silicon is the diffusing species during the silicidation. Silicon atoms move through the silicide layer thereby leaving behind a vacancy. The excess vacancies generated by silicidation are injected into the silicon substrate and can recombine and dissolve the interstitial end-of-range dislocations in the silicon substrate. In this work, shallow junctions were formed by using Ge preamorphization technique. Following dopant activation via solid phase epitaxial regrowth, a zone of interstitial dislocation loops remained near the original amorphous/crystalline interface due to residual end-of-range damage. A total annihilation of the Ge-induced interstitial defects in shallow p^+/n junctions was found during titanium silicidation. The effect of the metal-silicon reaction on defect reduction was also studied.

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Experimental

P-type, boron-doped or N-type, phosphorus-doped silicon wafers of 10-15 Ω-cm resistivity with <100> orientation were used in the course of this work. This study was conducted in the context of optimizing shallow junctions for 1 μm retrograde n-well CMOS technology (12). In this technology, shallow p^+ and n^+ junctions were formed by Ge^+ preamorphization and B^+ or As^+ implantation. Germaniun was implanted at 85 keV with a dose of 1×10^{15} cm^{-2} prior to the junction implantation. The energy and dose of the Ge were selected to amorphize the entire region of the boron implantation in order to effectively avoid channeling, and to keep the extended end-of-range defects produced at the original amorphous/crystalline interface, inside the heavily doped junction and away from the depletion region. This avoids excessive leakage currents due to electrically active defects in the depletion layer. Boron was then implanted at 10 keV with a dose of 1×10^{15} cm^{-2} to form the p^+ regions. The n^+ regions were formed by As implantation at 50 keV with a dose of 5×10^{15} cm^{-2}. The implanted junctions were annealed using two-step anneal-

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