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Nonvolatile memory with Co–SiO_2 core-shell nanocrystals as charge storage nodes in floating gate

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In this letter, we reported nanocrystal floating gate memory with Co–SiO_2 core-shell nanocrystal charge storage nodes. By using a water-in-oil microemulsion scheme, Co–SiO_2 core-shell nanocrystals were synthesized and closely packed to achieve high density matrix in the floating gate without aggregation. The insulator shell also can help to increase the thermal stability of the nanocrystal metal core during the fabrication process to improve memory performance. © *2009 American Institute of Physics*. [doi:10.1063/1.3258471]

The flash memory market has increased very quickly during the past decade. Nanocrystal (NC) floating gate flash memory is considered to be one of the most promising candidates to replace conventional highly doped polysilicon floating gate flash memory widely used in today's commercial market. Using discrete NCs embedded in a dielectric as a floating gate to store charge, lateral charge migration in the floating gate can be dramatically suppressed, making the device more robust against local defects, which can act as a leakage path in the very thin tunneling oxide. Thus smaller memory cell size, better programing/erasing characteristics, and better retention characteristics can be achieved. Since first described by Tiwari *et al.*,[1] much work has been done in this area to improve NC flash memory device performance. Different materials, such as Si,[2,3] Ge,[4] SiGe,[5] Ni,[6] and Au,[7,8] have been studied to work as the charge storage nodes. To achieve uniformly distributed NC matrix with high density, various NC deposition methods have been employed.[9–14] However, as the memory cell continuously scales down, there are still big challenges. According to International Technology Roadmap for Semiconductors (ITRS) 2007,[15] the memory cell size will reduce to ~1000 nm^2 by 2020, where only about ten NCs can be contained per memory cell. For such small scale, it becomes increasing challenging to synthesize suitable materials with uniform size and shape, and assemble them into a well-ordered NC matrix. In this letter, we present an approach to fabricate flash memory device with Co–SiO_2 core-shell NCs as charge storage nodes in the floating gate, where the Co–SiO_2 core-shell NCs are synthesized by biochemical technique to achieve controlled shape and size.

The NC memory device with Co–SiO_2 NC floating gate were fabricated on P-type silicon (100) substrate with the resistivity about 1–10 Ω cm. A schematic structure is shown in Fig. 1. After standard RCA clean and dilute 1:40 HF etch, thermal SiO_2 (~2 nm) was grown on silicon substrate at 850 °C. Our solution-phase synthesis of colloidal NCs is based on standard airless techniques on a Schlenk line.[16,17] First, cobalt NCs were fabricated by using a standard airless technique. As precursor for cobalt, di-cobalt octacarbonyl $[Co_2(CO)_8]$ was used. A solution of 0.54 g of $Co_2(CO)_8$ diluted in 3 ml of anhydrous o-dichlorobenzene (DCB) was rapidly injected in a three-neck flask containing 0.1 g of tri-octylphosphine and 0.1 ml of oleic acid in refluxing DCB. The temperature of the solution was lowered after 5 min and the colloids were recovered using a gas-tight syringe. Second, the Co NCs were coated with SiO_2 by adding a 5 ml aliquot of 0.5 mg ml^{-1} of synthesized colloids into a solution of 5 ml of Igepal CO-520 in 100 ml of cyclohexane. After this, a 0.6 ml solution of aqueous NH_4OH was added dropwise, for subsequent addition of 0.5 ml of tetraethyl orthosilicate. This reaction proceeded for 48 h, after which the NCs were recovered by employing a solvent/antisolvent purification technique. This washing step included precipitation with excess hexane and collection by centrifugation, followed by redispersion in ethanol. Using the water-in-oil microemulsion technique, the NCs were synthesized with controlled shape and size, as shown in Fig. 2(a), where the diameter of cobalt core is about 3.4 nm and the SiO_2 shell thickness is about 3.5 nm. When self-assembled, separated by the insulating shell, the Co NCs can form a close pack with a density about $\sim 0.8 \times 10^{12}$ cm^{-2} on the tunneling oxide surface, as shown in Fig. 2(b), without aggregation. In our experiment, Co is more desirable as the core material compared to its semiconductor counterpart, such as Si or Ge, because metals have large work function and can be engineered down to 1 nm without decreasing potential well depth due to quantum confinement effects. Thus, continuous reduction of the shell thickness may yield ultrahigh density NC matrix, which can potentially satisfy long term requirements for nonvolatile memories as for ITRS 2007. After NCs were deposited, the wafer was annealed in N_2 at 500 °C for 10 min. Then about 20 nm low-pressure chemical vapor depo-

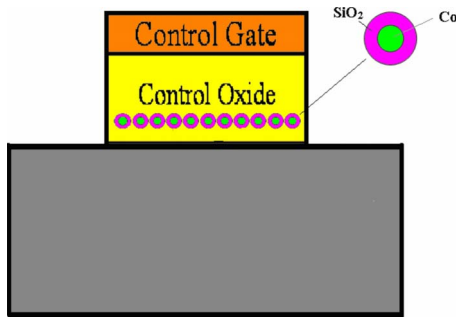

FIG. 1. (Color online) Schematic cross section view of Co–SiO_2 memory cell.

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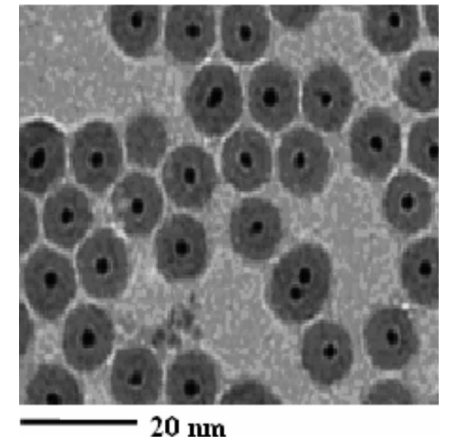
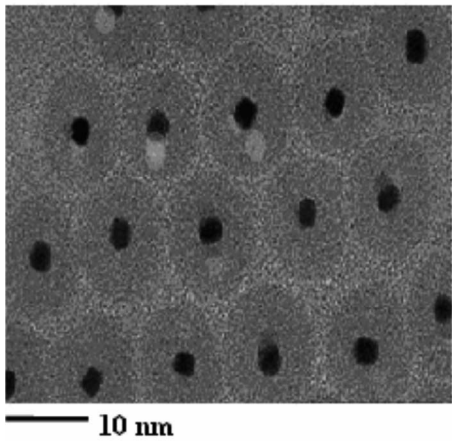


(a)



(b)

FIG. 2. (a) Synthesized colloidal Co–SiO_2 NCs. (b) Closely packed Co–SiO_2 NCs.

sition SiO_2 was deposited as control oxide and finally 2000 Å TaN was deposited by reactive dc sputtering at room temperature (RT) as control gate electrode. A control sample without Co–SiO_2 core-shell NCs but including all other layers was also fabricated to test the trapping characteristics of the dielectrics.

High frequency capacitance-voltage tests (1 MHz) were used to characterize the electrical properties of the devices. The threshold voltage (V_{th}) was determined by applying a −3 to 3 V scan after each programing/erasing stress pulse.

The programing characteristics as a function of voltage and pulse width for various operation conditions are shown

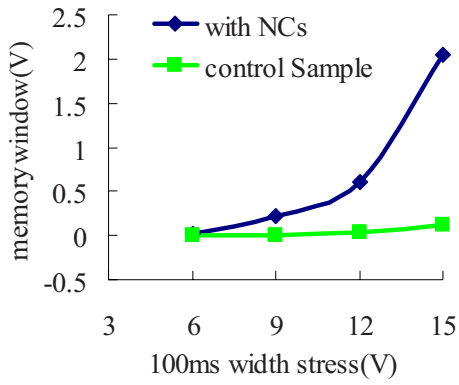


FIG. 3. (Color online) Memory window for different programing/erasing options with 100 ms pulse width.

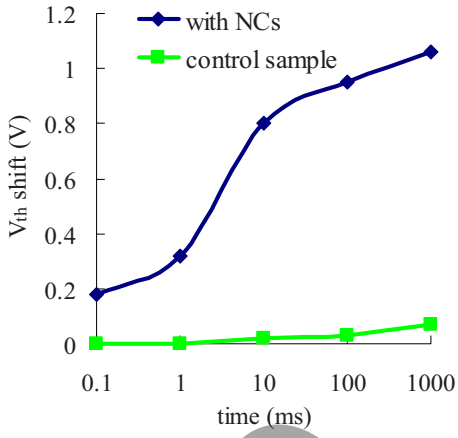


FIG. 4. (Color online) Programing speed for +15 V pulse.

in Figs. 3 and 4, respectively. Figure 3 shows that the memory window, which is defined as the V_{th} difference between the programing and erasing state, increases with the stress pulse magnitude. About 2.0 V memory window can be observed under +15 V, 100 ms programing and −15 V, 100 ms erasing conditions. For programing speed characteristics, in Fig. 4, V_{th} shift about 0.8V can be obtained under +15 V, 10 ms stress. Meanwhile, for both cases, only negligible memory window was found for control sample. This indicates that stored charges are not due to the traps in bulk SiO_2 dielectric layer or the interface traps between control oxide and tunneling oxide, but due to the embedded NCs. By using the following equation, the electron storage number per NC can be calculated as

$$\Delta V_{th} = \frac{q n_{nc} x}{\varepsilon_{ox}} \left(t_{control} + 0.5 \frac{\varepsilon_{ox} t_{nc}}{\varepsilon_{nc}} \right), \quad (1)$$

where the NC density $n_{nc}=0.8\times10^{12}/cm^2$, control oxide thickness $t_{control}=20$ nm, tunneling oxide dielectric constant $\varepsilon_{ox}(SiO_2)=3.9\varepsilon_0$, and ε_{nc} is the dielectric constant of the NC. Since Co NC is used as charge storage nodes in our experiment, ε_{nc} is very large and the second term in the parenthesis can be neglected. From Fig. 4, V_{th} shift under 15 V, 10 ms programing condition is about 0.8 V, thus it yields $x=1.1$ as the approximate number of electrons stored per NC.

Figure 5 shows the retention characteristics at RT. For an initial V_{th} shift about 1.52 V, about 0.88 V V_{th} shift still remains after 10^4 s. With extrapolation, 0.58 V V_{th} shift is still retained after 10^8 s. It is important to point out here that,

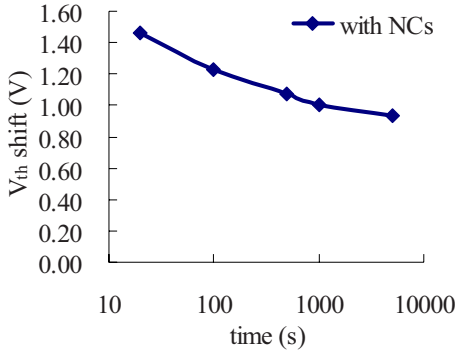


FIG. 5. (Color online) Retention characteristics at RT.

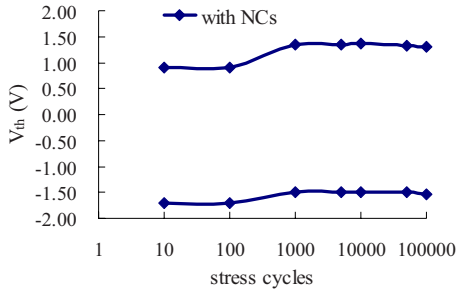


FIG. 6. (Color online) Endurance characteristics for ±15 V, 100 ms stress cycles.

with the SiO_2 shell, the thermal stability of the metal core can be improved to reduce oxidation of cobalt NCs during annealing and control oxide deposition steps and promotes a better interface. Some previous research has also shown that this kind oxidation of the metal NCs, which degrades interface quality, is a major reason for poor retention characteristics.[18] The endurance characteristics can also benefit from the improvement of the interface quality, as shown in Fig. 6. After up to 10^5 program/erase cycles with ±15 V, 100 ms pulse, the memory window does not show obvious degradation.

In summary, we have presented a NC flash memory device using $Co-SiO_2$ core-shell NCs as charge storage node in the floating gate. By using biochemical technique, $Co-SiO_2$ NCs can be synthesized with controlled shape and size and closely packed to achieve high density. The insulating shell also can help to increase the thermal stability of the NC metal core during the fabrication process to improve the memory device performance.

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