Journal of The Electrochemical Society, **156** (9) H734-H739 (2009)
0013-4651/2009/156(9)/H734/6/$25.00 © The Electrochemical Society

Integration of Atomic Layer Deposition-Grown Copper Seed Layers for Cu Electroplating Applications

L. Wu and E. Eisenbraun[z]

College of Nanoscale Science and Engineering, The University at Albany–State University of New York, Albany, New York 12203, USA

A plasma-enhanced atomic layer deposition (PEALD) copper process, using Cu(II) acetylacetonate and atomic hydrogen, was developed for Cu seed applications in nanoscale semiconductor processing. In this paper, the integration characteristics of PEALD Cu with electroplated Cu for advanced interconnect applications were investigated. Superconformal electroplated [electrochemical deposition (ECD)] copper was demonstrated on PEALD Cu-seeded high aspect ratio patterned structures. The filling characteristics of ECD/PEALD-grown Cu were compared with those of a conventional ECD/physical vapor deposition (PVD)-grown Cu stack. Void-free electroplated Cu was demonstrated on 60 and 35 nm patterned via structures using both atomic layer deposition Ru/TaN and conventional PVD Ta/TaN liner/barrier structures coupled with PEALD Cu seed layers. The resulting integration characteristics suggest that electroplated/PEALD Cu is a promising integration approach for emerging complementary metal oxide semiconductor metallization applications.
 [DOI: 10.1149/1.3166184]

Manuscript submitted April 20, 2009; revised manuscript received June 3, 2009. Published July 14, 2009.

Cu electroplating, or electrochemical deposition (ECD), is the interconnect conductor deposition method of choice for leading edge nanoelectronics.[1] A thin Cu seed layer is required before the Cu electroplating step to provide a more conductive substrate and to facilitate the nucleation of the electroplated Cu.[2] This seed layer is deposited over a barrier/liner stack, often TaN/Ta.[1] The conformality and coverage of the Cu seed layer over via and trench patterns is critical in determining whether the subsequent Cu electroplating is void free.[1] With the downscaling of interconnect feature dimensions, each individual layer within the metallization stack must become thinner and more conformal to comply with the overarching geometric constraints.[1] The ionized physical vapor deposition (iPVD) process currently employed becomes increasingly challenged to meet the seed/barrier requirements with respect to sidewall coverage and uniformity.[3] The low sidewall coverage, asymmetry, and overhang of the iPVD barrier/seed can result in electroplated Cu filling voids, which compromise the reliability and electrical performance of the Cu interconnects.[4,5] Therefore, a more conformal Cu seed layer is desirable to allow void-free filling of subsequent Cu electroplating in sub-45 nm interconnect structures.

Atomic layer deposition (ALD) is a self-limiting thin-film deposition method based on alternating saturated surface chemical reactions, which allows conformal deposition of materials on high aspect ratio (AR) trenches.[6] ALD is a promising alternative barrier/seed deposition method because of its excellent conformality and precise thickness control capability.[7] In particular, plasma-enhanced atomic layer deposition (PEALD) can deposit high density films at low processing temperatures, which is critical for the growth of thin continuous Cu films that are resistant to agglomeration.[8,9] The agglomeration of chemically deposited thin Cu layers is a major roadblock to extending Cu seed layer technology.[10] However, while a number of groups have reported the growth of Cu films by ALD, the suitability of such processes for seed layer applications has not been established.[11-13] In particular, the integration details of Cu ECD on high quality ALD Cu seeds for interconnect applications have not been reported.

Accordingly, a PEALD Cu process, using Cu(II) acetylacetonate [$Cu(acac)_2$] and plasma-generated atomic hydrogen, was developed for seeding applications in advanced interconnects.[14-16] This paper describes the integration feasibility of such a layer employing this PEALD Cu process.

Experimental

PEALD Cu films were deposited employing a modified Tokyo Electron Limited Phoenix cluster tool possessing dual 200 mm wafer processing modules. A direct plasma was generated by use of a plasma mesh oriented parallel to the substrate surface. The capacitively coupled plasma was driven by a 50 kHz power supply. The $Cu(acac)_2$ was heated in a stainless steel bubbler to 138°C and delivered to the process module with a He carrier gas. A low deposition temperature (85°C) was used to minimize the thermally induced agglomeration and surface roughness of the Cu films. Similarly, an in situ 10 min hydrogen plasma pretreatment before film deposition was used to enable improved Cu film quality, as described in another study carried out by the authors.[16] The precursor pulse/purge/H plasma pulse/purge time was 5/4/3/3 s. The PEALD Cu growth rate was 0.02 nm/cycle. Prior compositional measurements indicated that the Cu purity was greater than 95 atom % with O and C at the measurement noise level.[14] Analyses of these samples indicated that PEALD Cu films routinely contained less than 1.5 atom % hydrogen in the bulk of the Cu film, which is important for the stability of the Cu layers.[16] The resistivity of a 12 nm PEALD Cu layer deposited on a SiO_2 surface was 38.8 $\mu\Omega$ cm, while a 40 nm PEALD Cu had a resistivity of 7.6 $\mu\Omega$ cm, which was comparable to that of a 40 nm physical vapor deposition (PVD) Cu film (5.1 $\mu\Omega$ cm).[16] A 42 nm PEALD Cu had a (111) texture with a (111)/(200) peak ratio of ~6, which might be important for the formation of robust electromigration-resistant copper interconnects.[17]

PEALD Ru and TaN films were deposited using a 200 mm wafer capable in-house designed vertical flow, warm-wall ALD reactor. Both PEALD Ru and TaN processes employed NH_3-based plasmas and had the same process temperature (300°C) and pressure (50 mTorr). The Ru precursor source was an ethylcyclopentadienyl pyrrolyl ruthenium compound (Praxair Inc.), and the TaN precursor source was tert-butylimino-trisdiethylamino tantalum. For the PEALD Ru and TaN processes, the processing step time for each material was 5 s precursor pulse/10 s Ar purge/5 s NH_3 plasma/10 s Ar purge. The Ru and TaN film growth rates were 0.032–0.035 nm/cycle.[18] PVD Ta and TaN films were deposited in a Veeco Connexion 200 mm cluster tool. Cu electroplating was carried out in a customized electroplating cell, in which the plating area could be flexibly adjusted. A programmable power supply, PDPR 10-1-3 series (Dynatronix, Inc.), was operated in a constant current mode. The plating current density was 10 mA/cm^2. Samples were wetted with deionized (DI) water before immersion into the electrolyte and rinsed with DI water and dried using nitrogen gas after the Cu electroplating. The electrolyte consisted of 45 g/L Cu as $CuSO_4$, 85 g/L H_2SO_4, and the Enthone Viaform additive package, which enhanced the superconformal Cu filling in high AR trenches.[19]

Film composition was measured by Auger electron spectroscopy using a Perkin-Elmer PHI600 system. Hydrogen profiling was car-

[z] E-mail: eeisenbraun@uamail.albany.edu

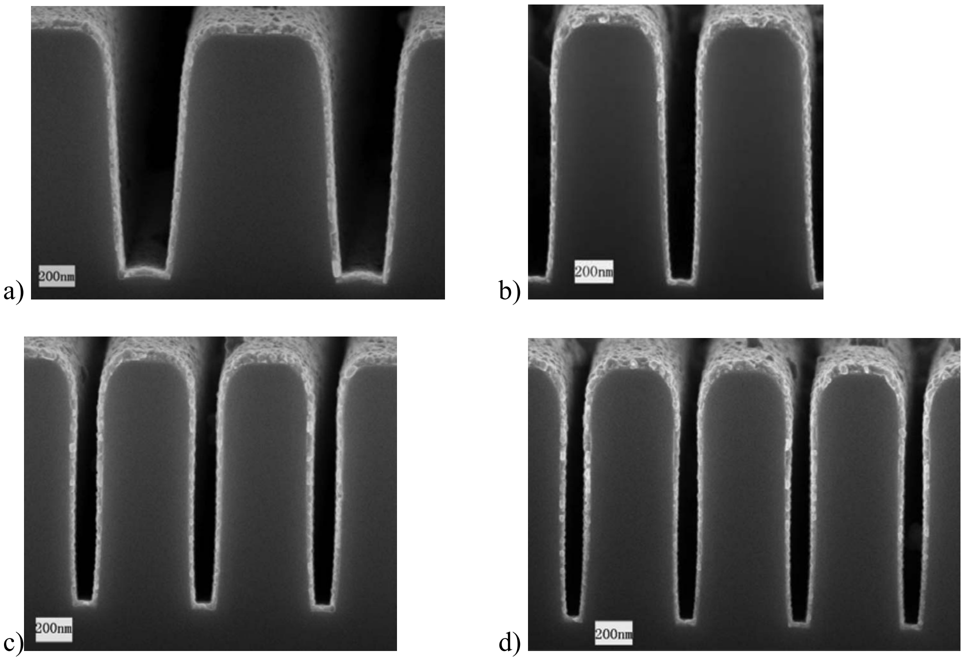

Figure 1. Cross-section SEM demonstrating nearly 100% conformality for a 42 nm PEALD Cu film deposited on SiO_2 trenches with different widths and ARs: (a) 400 nm, AR ~ 3.5, (b) 260 nm, AR ~ 5, (c) 200 nm, AR ~ 7, and (d) 160 nm, AR ~ 9.

ried out using a nuclear reaction analysis on the SUNY Dynamitron linear accelerator utilizing a ^{15}N primary beam operating between 6.375 and 6.705 MeV. Film continuity and electroplated Cu characteristics were studied by scanning electron microscopy (SEM) and transmission electron microscopy (TEM). A LEO 1550 SEM was operated with a 10 keV primary electron-beam energy. TEM was performed on a JEOL 2010F employing a 200 keV primary beam energy. Cross-sectional SEM and TEM specimens were prepared by focused ion beam (FIB) on an FEI 200 FIB tool. FIB microscopy was also employed to visualize the grain structure of polycrystalline electroplated Cu. The texture of the thin films was obtained from X-ray diffraction (XRD) employing a Scintag XDS 2000 X-ray diffractometer. Film sheet resistance was measured on a Signatone SYS-301 resistivity probing system, and the adhesion was evaluated by means of the Scotch tape test. In this test, Scotch tape is applied to and firmly pressed over the sample surface and then removed by pulling the tape off at an angle of 90° from the surface plane.[20,21] The peel force gave a qualitative measure of the Cu film adhesion to the substrate. In addition, pull testing was used to semiquantitatively assess the adhesive strength of the electroplated Cu deposited on Ru/SiO_2. The test studs were attached to sample surfaces by adhesive epoxy and pulled off under controlled conditions. Adhesion failure occurred when the tensile load exceeded the film adhesion strength at any interface or within any layer.[21]

Superconformal Cu Electroplating on Conformal PEALD Cu Seeds

A key advantage of PEALD is its capability to deposit conformal films over narrow, high AR structures. During the precursor pulse step, the self-limiting nature of the precursor adsorption process ensures that no more than a monolayer of precursor is adsorbed. This monolayer of precursor does not contain enough metal atoms to form a full monolayer of metallic film because of the size of adsorbed precursor molecules, which blocks surface sites due to steric effects.[6,7] During the precursor reduction step, the substrate is negatively biased as a result of the presence of the hydrogen plasma, which may facilitate the transportation of hydrogen ions into high AR trenches. The self-limiting Cu precursor adsorption combined with a uniform atomic hydrogen precursor reduction step enables conformal Cu film deposition on trenches. Sidewall coverage, which is defined as the ratio of the film thickness at the middle of the trench sidewall to that on the field, was used to quantify the conformality of the Cu film. Figure 1 shows cross-sectional SEM images of a 42 nm PEALD Cu deposited on SiO_2 trenches with widths from 160 to 400 nm and ARs from 3.5 to 9. Nearly 100% step coverage is observed on those trenches.

Superconformal Cu electroplating can lead to void-free, seamless via/trench filling for damascene-type Cu interconnects, which can be achieved by the use of organic additives that lead to a higher deposition rate at the bottom of the feature than on the sidewalls or field of the feature.[2,22] Superconformal via/trench filling eliminates filling seams, which act as surfacelike fast diffusion pathways for Cu electromigration, which would otherwise be present in the case of subconformal or conformal deposition.[23] Another important characteristic of electroplated Cu is its grain growth attributes, which significantly augment the range of linewidths where bamboolike Cu structures result.[2] Large grain size and bamboolike structures have a positive impact on electromigration, which is associated with grain boundary diffusion.[2,24] Figure 2 shows cross-sectional SEM images of 0, 10, 20, 30, 40, and 60 s duration electroplated Cu films on 42 nm PEALD Cu-seeded SiO_2 trenches (300 nm, AR ~ 5). The PEALD Cu was conformal on the trench surfaces before the Cu electroplating, as shown in Fig. 2a. As the Cu electroplating duration

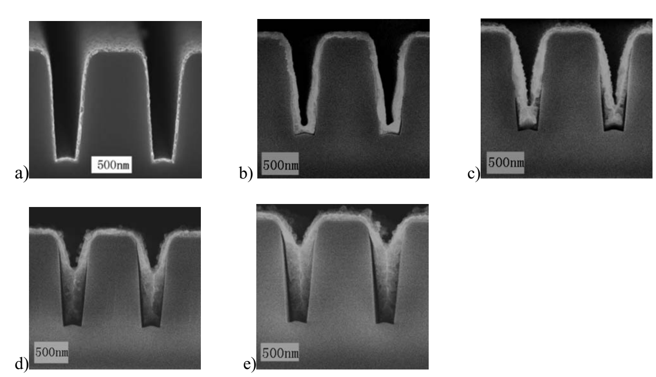

Figure 2. Cross-sectional SEM images of (a) conformal 42 nm PEALD Cu deposited on SiO_2 trenches with a width of 300 nm and an AR of ~5. Void-free superconformal electroplated Cu layers were observed after (b) 10, (c) 20, (d) 30, and (e) 40 s duration depositions on the 42 nm PEALD Cu seed. The electroplating current density was 10 mA/cm^2.

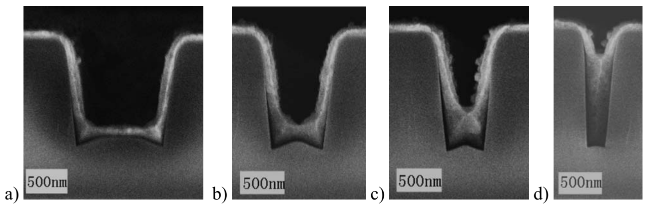

Figure 3. Cross-sectional SEM data from a 30 s duration electroplated Cu film deposited over a 42 nm thick PEALD Cu seed layer in SiO_2 trenches of (a) 1100 nm, AR ~ 1, (b) 600 nm, AR ~ 2, (c) 450 nm, AR ~ 3, and (d) 250 nm, AR ~ 6. A higher Cu deposition rate was observed in the smaller trenches.

increased from 10 to 60 s, the electroplated Cu gradually grows from the trench bottoms without the formation of filling voids, as shown in Fig. 2b-e. The cross-sectional SEM samples were prepared by simple cleaving. Because of the poor adhesion of the Cu–SiO_2 interface, the Cu films are slightly pulled away from the SiO_2 surfaces. This cleaving artifact generates topographical contrast and gives the appearance of a filling seam in Cu cross sections. The electroplated Cu growth rate at the bottom of the trenches was higher than that on the field and trench sidewalls, which resulted in the expected "bottom up" superconformal Cu filling behavior. As shown in Fig. 3a, for 1100 nm trenches with AR ~ 1, the growth rates on the trench sidewalls and bottoms are similar to that on the field. As the trench size decreases and the AR increases, the growth rate inside the trenches increases. As shown in Fig. 3d, the growth rate inside the 250 nm trenches with AR 6 is ~12 times higher than that on the field.

Performance of Electroplated Cu on PEALD-Grown Cu Seed

Ru has been proposed as a liner for direct Cu electroplating; however, there are several issues associated with this approach.[25,26] In particular, the oxidation of Ru blocks the underpotential electrodeposition of Cu and the adsorption of bath additives, and the residual Ru oxide can also result in a weak Cu/Ru adhesion, a low nucleation density, and a poor trench filling.[25,26] Similar to the function of a PVD Ta liner deposited over the TaN barrier, a conformal PEALD Ru is deposited on PEALD TaN as the liner to promote the Cu adhesion and wettability and to enhance the PEALD Cu nucleation.[16,27,28] To study the performance of PEALD Cu vs PVD Cu, a series of different integration structures, including PVD Cu/Ta/TaN, PEALD Cu on PVD Ta/TaN, PEALD Cu/Ru on PVD TaN, and PEALD Cu/Ru/TaN, was systematically studied. In consideration of the lower intrinsic step coverage for the PVD seed/barrier, the PVD layers were fabricated to possess approximately three times the field thickness of the ALD layers, which is expected to have a favorable impact on ECD Cu nucleation and texturing. The PVD Cu seed layer thickness was 30 nm, and the PEALD Cu thickness was 10 nm. Only PVD Cu/Ta/TaN films were deposited without breaking the vacuum, while all the liner/barrier substrates (PVD and ALD) were exposed to the air before PEALD Cu deposition due to tooling limitations. The patterned samples used in this study have trench sizes ranging from ~160 to 1500 nm and ARs ranging from 1 to 9, which are the same as in the previous figures.

Table I summarizes the integration schemes used and the results obtained on the patterned samples. Specular electroplated Cu was observed on the PVD 30 nm Cu/8 nm Ta/12 nm TaN-coated substrate, and the electroplated Cu passed the Scotch tape adhesion test (STAT). The 30 nm thick PVD Cu seed was sufficient for Cu electroplating on large trenches with low AR. However, filling voids were observed at the bottom of trenches smaller than 350 nm with AR greater than ~4. For 10 nm PEALD Cu seed on a PVD 8 nm Ta/12 nm TaN stack, the electroplated Cu was smooth and specular; however, abundant voids were observed inside most structures. Because the PVD Ta/TaN-coated substrate was exposed to air before PEALD Cu deposition, the metallic Ta surface layer may have been oxidized. Unlike Ru oxide, native Ta oxide cannot easily be reduced to metallic Ta during the predeposition hydrogen plasma treatment due to its high Gibbs free energy.[29] This surface oxide has a negative impact on PEALD Cu nucleation, preventing the formation of a fully continuous PEALD Cu layer at a 10 nm equivalent film thickness.[16,30] As a result, the exposed Ta oxide may react with the plating electrolyte to form unwanted compounds, leading to a poor quality of the electroplated Cu.[31] For the electroplated Cu on 10 nm PEALD Cu/4 nm PEALD Ru/12 nm PVD TaN, filling voids were observed only in trenches smaller than 200 nm with an AR higher than 7. Even for those trenches with filling voids, electroplated Cu was observed at the bottom of the trenches, which suggests that the trench sidewalls and bottoms were electrically continuous.[32] For all PEALD-grown 10 nm Cu/3 nm Ru/3 nm TaN samples, void-free Cu was observed in all trenches. Electroplated Cu was specular and passed the STAT. These results indicate that all the ALD seed/liner/barrier structures have the best filling properties for Cu electroplating among the sample sets tested.

Because any ALD liner- or seed-based integration scheme is likely to only be employed in a sub-32 nm technology, it is important to test the scalability of PEALD Cu in smaller structures. The test structures used in this work for the scalability test have six sets of patterns; each set of the pattern is made of five identical trenches. The depth of all trenches was ~180 nm, while the trench widths ranged from 35 to 500 nm, resulting in ARs between ~0.3 and 5. The liners/barriers compared for this study were 3 nm PVD Ta/3 nm PVD TaN and 3 nm PEALD Ru/3 nm PEALD TaN. To examine the scalability, various thicknesses of PEALD Cu were deposited over the structures before subsequent Cu electroplating. The sheet resistance values of the PVD Ta/TaN and PEALD Ru/TaN were 800 ± 130 and 769.0 ± 24.1 $\Omega/\square$, respectively.

An initial evaluation of the PEALD Cu continuity was done using a simple sheet resistance measurement. The PVD Ta/TaN substrate conductivity did not improve after 6 and 8 nm thick PEALD Cu depositions. The sheet resistance only decreased after a 12 nm thick PEALD Cu deposition (215.5 ± 36.9 $\Omega/\square$), and a 14 nm thick PEALD Cu deposition significantly decreased the substrate resistance (15.4 ± 1.0 $\Omega/\square$). During the initial PEALD Cu nucleation on the Ta/TaN substrate, isolated Cu islands formed. The isolated Cu islands do not improve substrate conductivity because of

Table I. Performance of electroplated Cu on various seed/liner/barrier structures.

Cu seed	Liner/barrier	Cu electroplating results
30 nm PVD	8 nm PVD Ta/ 12 nm PVD TaN	Smooth specular Cu passed the STAT. Void-free ECD filling for trenches ≥350 nm with AR ≤ 4.
10 nm ALD	8 nm PVD Ta/ 12 nm PVD TaN	Specular Cu, failed STAT. Voids observed in most trenches.
10 nm ALD	4 nm ALD Ru/ 12 nm PVD TaN	Smooth specular Cu passed STAT. Void-free filling for trenches ≥250 nm with AR ≤ 6:1.
10 nm ALD	3 nm ALD Ru/ 3 nm ALD TaN	Smooth specular Cu passed STAT. Void-free filling for all trenches.

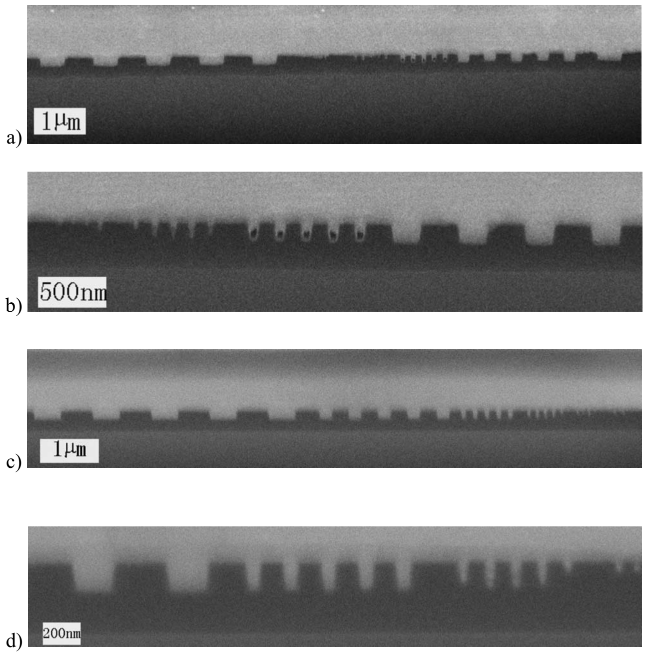

Figure 4. Cross-sectional SEM images of (a) an overall view and (b) a magnified view at an angle of 45° of electroplated Cu on 8 nm PEALD Cu/3 nm PVD Ta/3 nm PVD TaN-seeded structures. Voids were observed in 60 and 85 nm structures. (c) An overall view and (d) a magnified view at an angle of 45° of void-free electroplated Cu on 14 nm ALD Cu/3 nm PVD Ta/3 nm PVD TaN-seeded structures.

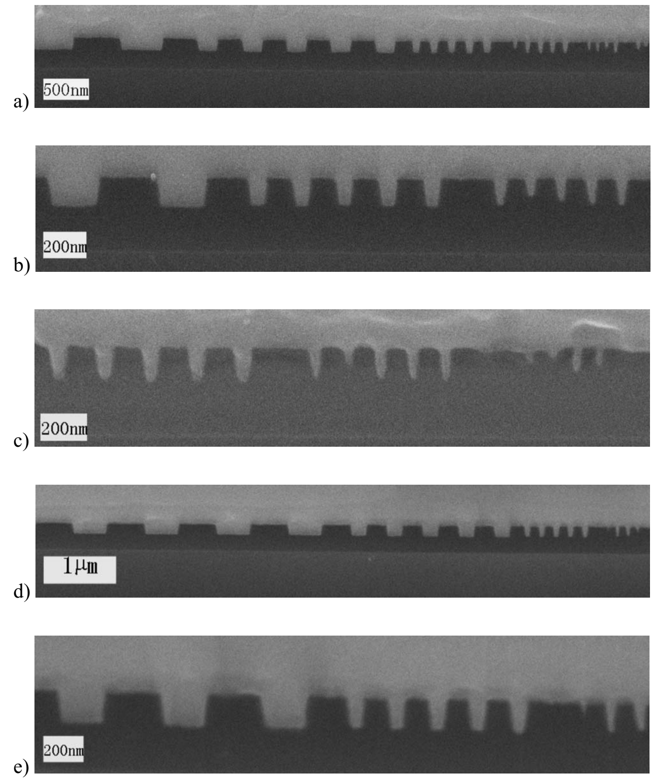

Figure 5. Cross-sectional SEM images of (a) an overall view and [(b) and (c)] magnified views at an angle of 45° of void-free electroplated Cu on 6 nm PEALD Cu/3 nm PEALD Ru/3 nm PEALD TaN structures. (d) An overall view and (e) a magnified view at an angle of 45° of void-free electroplated Cu on 14 nm PEALD Cu/3 nm PEALD Ru/3 nm PEALD TaN structures.

the lack of Cu conduction pathways among those islands. After a certain thickness of Cu deposition, a fraction of the PEALD-grown Cu islands coalesces, and substrate conductivity increases. Eventually, a continuous PEALD Cu film significantly improves the substrate conductivity. In contrast, the sheet resistance values of 6 and 14 nm thick PEALD Cu layers grown on PEALD-grown Ru/TaN substrates were 182.4 ± 3.6 and 20.88 ± 0.50 $\Omega/\square$, respectively, which indicates that PEALD Cu grains achieve coalescence more easily on such surfaces. The 10 min predeposition plasma treatment was observed to reduce the Ru oxide to metallic Ru and removed the surface hydroxyl groups.[16] This in turn improved the PEALD Cu nucleation and wetting properties on the Ru/TaN substrate, leading to partial coalescence of Cu nuclei in the 6 nm thick PEALD Cu film. The presence of potential conduction paths in the PEALD Cu is reflected by the low resistance of the films deposited on the Ru/TaN substrate.

To evaluate the specific effect of PEALD Cu seed layer thickness and continuity on Cu electroplating, 60 s long Cu electroplating processes were done on 8 and 14 nm thick PEALD Cu seed layers deposited over patterned structures with PVD-grown 3 nm Ta/3 nm TaN liners. The electroplating potential between electrodes was 1.98 V for an 8 nm thick Cu-seeded substrate, while the electroplating potential decreased to 0.22 V for the 14 nm thick PEALD Cu-seeded sample, as a result of the lower substrate sheet resistance. The filling characteristics of 8 and 14 nm thick PEALD Cu-seeded structures are shown in Fig. 4. The dark area is the substrate, and the light area is electroplated Cu. Samples were prepared by FIB, and SEM images were taken from a 45° top-down direction; therefore, the actual AR of the trench is ~1.4 times greater than what appears in the image. For 8 nm thick PEALD Cu-seeded structures, filling voids were observed in 60 and 85 nm structures. Void-free electroplated Cu was only obtained on samples with 14 nm thick PEALD Cu-seeded structures. For the 35 nm structures, the PEALD 14 nm Cu/3 nm Ru/3 nm TaN stack fills the 35 nm structures even before the electroplating. Any seam inside such structures arising from the conformal Cu/Ru/TaN deposition might be smeared out during the FIB sample preparation. For the 6 and 14 nm PEALD Cu deposited on PEALD Ru/TaN substrates, the potentials between electrodes during electroplating were 0.40 V for the 6 nm thick Cu-seeded substrate and 0.20 V for the 14 nm thick Cu-seeded substrate. The electroplated Cu films on both seeds were smooth and specular and passed the STAT. As shown in Fig. 5, void-free electroplated Cu was observed in all size trenches for both 6 and 14 nm thick PEALD Cu seeds. Cross-sectional TEM confirmed the void-free electroplated Cu filling characteristics on 14 nm thick PEALD Cu-seeded samples, as shown in Fig. 6. By way of comparison with other work done in this area, Huo et al. demonstrated void-free electroplated Cu

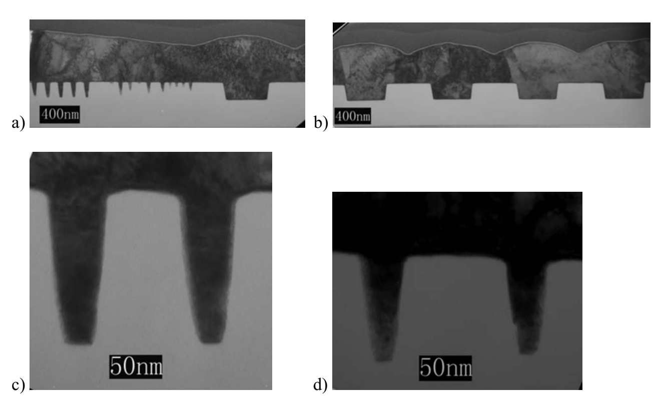

Figure 6. Cross-sectional TEM images of electroplated Cu on 6 nm PEALD Cu/3 nm PEALD Ru/3 nm PEALD TaN structures. Void-free electroplated Cu was observed in all trenches. (a) An overall view. (b) 500, (c) 60, and (d) 35 nm trenches.

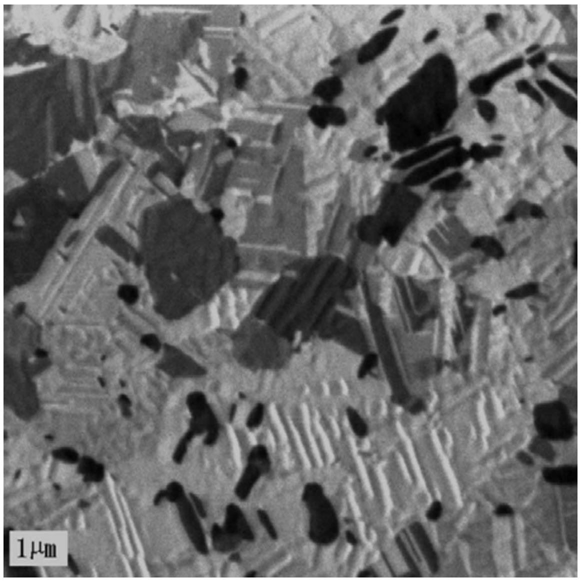

Figure 7. FIB image of 160 s electroplated Cu on 10 nm PEALD Cu/3 nm ALD Ru/3 nm ALD TaN. The average Cu grain size was 1000 nm.

on a 20 nm thick ALD Cu seed on an undisclosed substrate.[33] However, only limited information was provided in that paper, and the feature size (~150 nm) was larger than we used in this study. This paper reports void-free electroplated Cu on ALD Cu-seeded sub-100 nm features.

Integration Properties of Electroplated Cu with PEALD Cu Seed Layers

For a typical electroplated Cu layer deposited on a PEALD Cu/Ru/TaN substrate, nearly 100% Cu purity was observed. All the electroplated Cu layers deposited on Ru substrates passed the STAT. Pull testing was used to semiquantitatively assess the adhesive strength of an ~1000 nm electroplated Cu deposited on 20 nm Ru/SiO_2.[21] The delamination occurred not at the Cu/Ru interface, but instead at the Ru/SiO_2 interface, and the tensile strength when the failure occurred was 25.9 ± 0.6 MPa. While Ru generally has poor adhesion strength to SiO_2-based dielectrics, the Ru/SiO_2 interface delamination suggests that the Cu/Ru interface has a higher adhesion strength than the Ru/SiO_2 interface.[34,35] In addition to providing a more conductive substrate and improving adhesion, the seed layer also stimulates the nucleation and subsequently the crystallographic texture of the electroplated Cu.[2] Figure 7 is a typical top-down FIB image of a 160 s duration electroplated Cu film deposited on a 10 nm PEALD Cu/3 nm PEALD Ru/3 nm PEALD TaN substrate after it was self-annealed at room temperature for 15 days. The FIB image revealed distinct large Cu grains, which are indicative of recrystallization and subsequent grain growth of the Cu microstructure.[36] The recrystallized microstructure also exhibits a high degree of crystallographic twinning, and many of the grains contain more than one set of twins. The average grain size of this film was 1000 nm, as measured by commercial image processing software.[37]

A high degree of twinning, along with a large grain size, is commonly found in plated Cu thin films.[2] This type of electroplated Cu grain growth is predicted to enhance the range of linewidths with bamboolike Cu filling, hence reducing the grain boundary diffusion and improving the electromigration performance.[2] The large volume of twinning is proposed to be a potentially beneficial effect because twin boundaries are known to be low diffusivity paths.[2] Texture inheritance from the underlying seed layer is a common phenomenon in thin films,[38,39] and thick PEALD Cu films typically possess a strong (111) texture.[15] XRD analysis indicated a comparatively

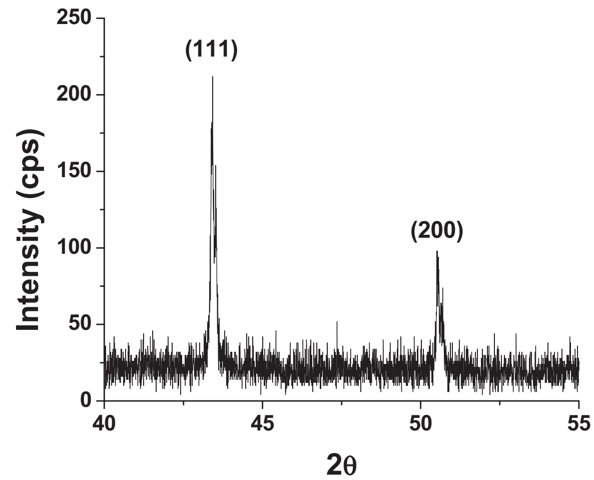

Figure 8. XRD spectrum of 160 s electroplated Cu deposited on 10 nm PEALD Cu/3 nm ALD Ru/3 nm ALD TaN. The (111)/(220) peak ratio was 2.5.

low fraction of (111) component in the Cu film (as shown in Fig. 8); the (111)/(200) peak ratio was 2.5. In comparison, a strong (111) texture with a (111)/(200) peak ratio at 10.7 in electroplated Cu was observed on the PVD-grown 30 nm Cu/8 nm Ta/16 nm TaN substrate. These suggest that the 10 nm thick PEALD Cu film may not possess a strong (111) texture as do thicker PEALD Cu films, although no direct comparison with such a thin seed layer is available because only results from thicker seed layers are reported. As such, it is believed that a less significant (111) texture may be evident regardless of the seed layer processing technique and is due simply to seed layer thickness.

Conclusions

A manufacturable PEALD Cu process has been developed for interconnect seed layer applications. The superconformal filling characteristics of electroplated Cu on PEALD Cu-seeded trenches were demonstrated. When compared with other integration configurations, the PEALD-grown Cu/Ru/TaN stack exhibits the best filling characteristics on high AR trenches. The scalability of PEALD Cu on PVD Ta/TaN and PEALD Ru/TaN-coated test structures was studied. Void-free electroplated Cu was demonstrated on 35–500 nm wide patterned via structures using both ALD Ru/TaN and conventional PVD Ta/TaN liner/barrier structures coupled with PEALD Cu seed layers. These results suggest that Cu electroplating on PEALD Cu is a promising approach for future complementary metal oxide semiconductor metallization technologies.

Acknowledgments

This work is supported by the New York State Foundation for Science, Technology, and Innovation (NYSTAR) and the Semiconductor Research Corporation (SRC) under the New York State Center for Advanced Interconnect Science and Technology (CAIST), which is gratefully acknowledged. The authors thank the International Business Machines Corporation (IBM) for the fabrication of patterned structures that were used in this study. The authors also thank Thomas Murray at the University at Albany College of Nanoscale Science and Engineering for his assistance with TEM imaging.

University at Albany–State University of New York assisted in meeting the publication costs of this article.

References

1. The International Technology Roadmap for Semiconductors, Semiconductor Industry Association, http://public.itrs.net, last accessed July 10, 2009.
2. R. Rosenberg, D. C. Edelstein, C.-K. Hu, and K. P. Rodbell, *Annu. Rev. Mater. Sci.*, **30**, 229 (2000).
3. U. Helmersson, M. Lattemann, J. Bohlmark, A. P. Ehiasarian, and J. T. Gudmunds-

son, *Thin Solid Films*, **513**, 1 (2006).
4. W. L. Goh and K. T. Tan, *Thin Solid Films*, **462–463**, 275 (2004).
5. C. M. Tan and A. Roy, *Mater. Sci. Eng., R.*, **58**, 1 (2007).
6. M. Ritala and M. Leskelä, *Handbook of Thin Film Materials*, Vol. 1, p. 103, Academic, San Diego, CA (2002).
7. H. Kim, *J. Vac. Sci. Technol. B*, **21**, 2231 (2003).
8. C. Yang, J. S. Jeng, and J. S. Chen, *Thin Solid Films*, **420–421**, 398 (2002).
9. H. Kim, Y. Kojima, H. Sato, N. Yoshii, S. Hosaka, and Y. Shimogaki, *Jpn. J. Appl. Phys., Part 2*, **45**, L233 (2006).
10. H. Kim, H. B. Bhandari, S. Xu, and R. G. Gordon, *J. Electrochem. Soc.*, **155**, H496 (2008).
11. P. Martensson and J. O. Carlsson, *J. Electrochem. Soc.*, **145**, 2926 (1998).
12. A. Niskanen, A. Rahtu, T. Sajavaara, K. Arstila, M. Ritala, and M. Leskelä, *J. Electrochem. Soc.*, **152**, G25 (2005).
13. Z. Li, A. Rahtu, and R. G. Gordon, *J. Electrochem. Soc.*, **153**, C787 (2006).
14. L. Wu and E. Eisenbraun, *J. Vac. Sci. Technol. B*, **25**, 2581 (2007).
15. L. Wu, W. Zeng, and E. Eisenbraun, *ECS Trans.*(7), **11**, 67 (2007).
16. L. Wu and E. Eisenbraun, *Electrochem. Solid-State Lett.*, **11**, H107 (2008).
17. H. Lee, S. S. Wong, and S. D. Lopatin, *J. Appl. Phys.*, **93**, 7 (2003).
18. S. Kumar, D. Greenslit, T. Chakraborty, and E. Eisenbraun, *J. Vac. Sci. Technol. A*, **27**, 572 (2009).
19. M. Zheng, M. Willey, and A. C. West, *Electrochem. Solid-State Lett.*, **8**, C151 (2005).
20. Scotch MagicTM Tape, 3M Company, www.3m.com, last accessed July 10, 2009.
21. R. Lacombe, *Adhesion Measurement Methods: Theory and Practice*, Taylor & Francis, New York (2005).
22. P. C. Andricacos, C. Uzoh, J. O. Dukovic, J. Horkans, and H. Deligianni, *IBM J. Res. Dev.*, **42**, 567 (1998).
23. L. Su, S. Subbanna, E. Crabbe, P. Agnello, E. Nowak, R. Schulz, S. Rauch, H. Ng, T. Newman, A. Ray, et al., in *IEEE Symposium on VLSI, Technical Digest*, IEEE, p. 12 (1996).
24. K. N. Tu, *J. Appl. Phys.*, **94**, 5451 (2003).
25. T. P. Moffat, M. Walker, P. J. Chen, J. E. Bonevich, W. F. Egelhoff, L. Richter, C. Witt, T. Aaltonen, M. Ritala, M. Leskelä, et al., *J. Electrochem. Soc.*, **153**, C37 (2006).
26. L. D. Burke, N. S. Naser, and R. Sharna, *J. Appl. Electrochem.*, **38**, 377 (2008).
27. H. Kim and Y. Shimogaki, *J. Electrochem. Soc.*, **154**, G13 (2007).
28. H. Kim, T. Koseki, T. Ohba, T. Ohta, Y. Kojima, H. Sato, and Y. Shimogaki, *J. Electrochem. Soc.*, **152**, G594 (2005).
29. *Handbook of Chemistry and Physics*, D. R. Lide, Editor, pp. 5–72, CRC, Boca Raton, FL (1995).
30. S. L. Cohen, M. Liehr, and S. Kasi, *Appl. Phys. Lett.*, **60**, 50 (1992).
31. U. Cohen, *Solid State Technol.*, **49**, 7 (2006).
32. J. H. Sukamto, E. Webb, T. Andryushchenko, and J. Reid, *J. Appl. Electrochem.*, **34**, 283 (2004).
33. J. Huo, R. Solanki, and J. McAndrew, *J. Mater. Res.*, **17**, 2394 (2002).
34. U.-S. Chen, W.-J. Hsieh, H. C. Shih, Y.-S. Chang, K.-W. Weng, and D.-Y. Wang, *Nucl. Instrum. Methods Phys. Res. B*, **237**, 470 (2005).
35. E. H. Lee, N. Truong, R. Prater, and M. Diana, U.S. Pat. Appl. 20,080,274,369 (2008).
36. A. Tzanavaras, G. Young, and S. Gleixner, *J. Electrochem. Soc.*, **152**, C101 (2005).
37. W. S. Rasband, ImageJ, U.S. National Institutes of Health, Bethesda, MD, http://rsb.info.nih.gov/ij/, last accessed July 10, 2009.
38. D. P. Tracy, D. B. Knorr, and K. P. Rodbell, *J. Appl. Phys.*, **76**, 2671 (1994).
39. C. E. Murray, K. P. Rodbell, and P. M. Vereecken, *Thin Solid Films*, **503**, 207 (2006).