Real-Time Implementation of a Reconfigurable IMT-2000 Base Station Channel Modem

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ABSTRACT

Research suggests that joint methods combining smart antennas, RAKE reception, multi-user detection or other adaptive methods may be practically implemented for IMT-2000 channel modems using computationally simplified algorithms. Using software-defined radio methods, these modems can be employed in a new generation of adaptive multimode base stations which permit software reconfiguration from second- to third-generation air interfaces. Practical implementation is made possible by corresponding advances in hardware technology, including new processors and high-bandwidth I/O fabrics which replace traditional computer buses with their inherent limitations in bandwidth and scalability. In this article recent adaptive processing research is reviewed, implementation requirements for second- and third-generation base stations are considered, and the capabilities of selected new monolithic silicon devices are examined. A possible implementation approach for a reconfigurable multimode base station channel modem using SDR design methods is proposed.

INTRODUCTION

International Mobile Telecommunications-2000 (IMT-2000) is the International Telecommunications Union's (ITU's) vision of global wireless (mobile) access in the 21st century. It is scheduled to start service after the year 2000 subject to market considerations, using one of five defined air interfaces. To achieve the required system performance and spectrum efficiency, ITU M.1036 recommends adaptive technologies be used [1]:

> *"6. Spectrum efficiency: that methods should be employed to ensure efficient use of the spectrum, such as the following:*
> *a) radio transceiver technology and access protocols, including access technology, modulation and coding, adaptive interference management, diversity techniques, and smart antenna technology;"*

During the spectrum allocation process for IMT-2000, several national administrations assumed the use of smart antennas and adaptive technologies when calculating the spectrum requirements for IMT-2000 deployment. Thus, third-generation (3G) network operators *may not achieve full network capacity without these methods*. Competitive pressures from growing numbers of 3G users, demanding high bandwidth, high quality of service, and small phones, may further motivate IMT-2000 operators to implement smart antennas, multi-user detection (MUD), 2D RAKE receivers, and other space-time adaptive processing (STAP) algorithms. In addition, because of the gradual implementation of 3G systems around the world, the ability to upgrade base stations from 2G to 3G, using software reconfiguration, is a highly desirable feature. The chip technologies needed to practically implement these new adaptive, software-reconfigurable modems are now becoming available to base station designers.

A *software-defined radio* (SDR) is defined as a radio in which the receive digitization is performed at some stage downstream from the antenna, typically after wideband filtering, low-noise amplification, and downconversion to a lower frequency in subsequent stages. A reverse process occurs for the transmit digitization. Software radios employ one or more reconfigurable processors embedded in a real-time multiprocessing fabric, permitting flexible reprogramming and reconfiguration using different software downloads. SDRs often employ wideband radio frequency (RF) front-end architectures in addition to reconfigurable digital signal processing in their design (Fig. 1). Such designs are well suited for implementing multiband, multimode base stations equipped with smart antennas and adaptive processing [2]. As new services or signal processing algorithms become available, the service provider may upgrade the base station using software downloads, adding new hardware if more processing is required for real-time performance. Another primary consideration of SDR technology application in base stations is reductions in cost [3]. Software base stations also offer cross-standards support and reconfigurability across networks, and may be used to deploy new features and instantiate new air interfaces on demand. Standards and architectures for SDR are under development by the SDR Forum and other groups around the world [4].

SPACE-TIME ADAPTIVE PROCESSING

Application of STAP can be used to enhance the performance of 2G and 3G systems [5]. In a com-

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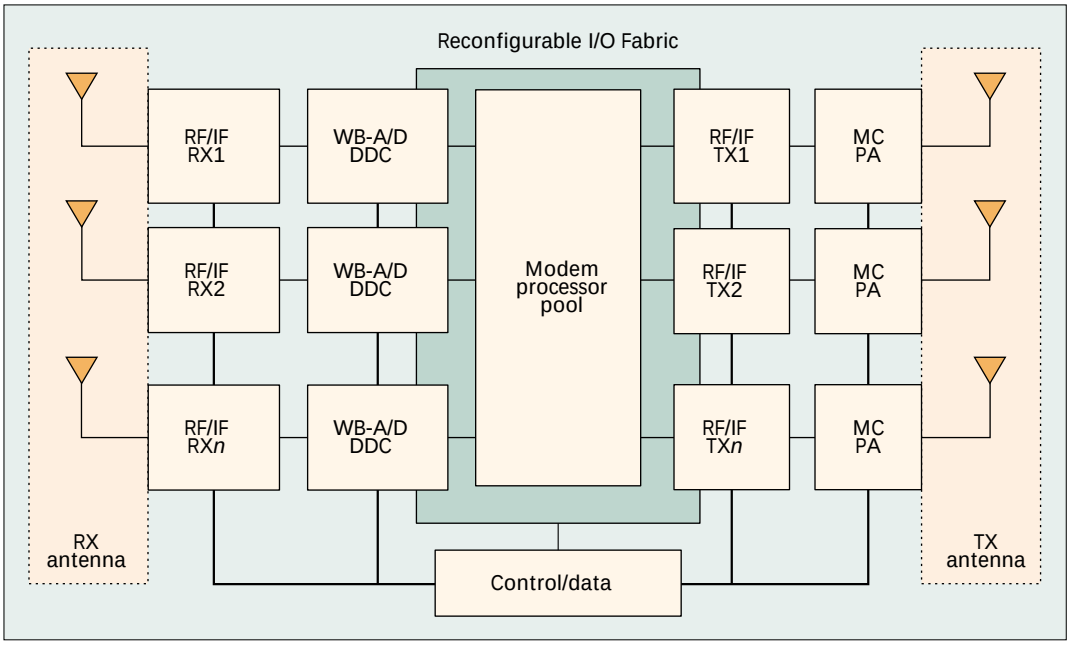

Figure 1. *In a software-defined base station, a reconfigurable, reprogrammable "pool of processors" including RISCs, DSPs, and ASICs offers unprecendented flexibility in designing wideband modems for IMT-2000 base station front-ends.*

In a commercial GSM field trial conducted by Ericsson and Mannesmann Mobilfunk, smart antennas achieved a 120 percent capacity increase under real-world network conditions.

mercial Global System for Mobile Communications (GSM) field trial conducted by Ericsson and Mannesmann Mobilfunk, smart antennas achieved a 120 percent capacity increase under real-world network conditions [6]. In simulations of IS-95 code-division muliple access (CDMA) networks using smart antennas, "sculpting" of sector coverage to provide load balancing increased forward link capacity by 27 percent [7].

While smart antennas for 3G systems involve greater implementation complexity than systems for GSM or CDMA, similar benefits are achievable [8]. Switched fixed-beam smart antennas are under serious consideration by several wideband CDMA (W-CDMA) base station designers. These antennas offer significant performance benefits over conventional (two-element diversity) base station antenna designs.

Research shows promising combinations of spatial diversity with other methods, giving new meaning to "hybrid vigor." One method, 2D RAKE, combines traditional RAKE receivers with spatial diversity. Separate beamformers are assigned to each finger of the receiver [9]. Space-time array receivers (STARs) may improve antenna performance by 14 dB over conventional adaptive array methods for W-CDMA, and also mitigate co-channel interference (CCI) [10].

Reduced Complexity Methods

The computational complexity of adaptive algorithms has been reduced by use of suboptimal methods. In the example of multi-user detectors (MUDs), which may double or even triple the number of simultaneous users in CDMA networks, optimal detectors for MUD are exponential in complexity with respect to the number of users. Typically several teraflops of processing and several gigabytes per second of interprocess I/O are required to implement optimal detectors for 3G base stations. In contrast, suboptimal detectors such as multistage parallel interference cancellation (PIC) may be implemented with quadratic complexity, and are of great interest to base station designers [11].

With two- and three-branch diversity antennas, use of groupwise successive interference cancellation (GSIC) may increase system capacity by over 200 percent for CDMA networks that support multiple bit rates [12]. Implementation complexity for basic and extended GSIC requires approximately 21.7 Gflops and 43.4 Gflops, respectively. However, when implementing multistage interference cancellation systems, *computational latency must be kept low* to avoid intolerable processing delays in digitized voice and video applications.

Joint space-time processing methods are desirable, not only for their improved performance, but also for their *synergistic reduction in computational complexity over single-discipline methods* when tightly coupled to overall 3G system design [13].

Implementation Requirements

A key design issue is the processing complexity for multimode air interface implementation. Table 1 shows the estimated implementation requirements for GSM, IS-95 CDMA, or W-CDMA using SDR methods on a wideband (5 MHz) channel modem.

A second key consideration is the effect of partitioning. Table 2 shows the effect of partitioning on processing requirements to implement one 200 kHz GSM air interface without equalizers or adaptive processing [14]. By using sufficiently powerful processors, partitioning can be eliminated or minimized. This may reduce implementation complexity by an order of magnitude or more. (Note: the complexity estimates in Table 1 do not consider the effect of parti-

Air interface	GSM	CDMA	W-CDMA
Proc. reqt per RF channel	405 Mflops	1945 Mflops	12,300 Mflops
RF channels allocated	16x 200 kHz	3x 1230 kHz	1x 5000 kHz
Users/channels	$N = 8$	$N = 13$	$N = 16$
Total Gflops	6.6	5.4	12.3

Table 1. *Estimated processing requirement for a 5 MHz base station modem. Partitioning is not considered.*

Partitioning (for eight GSM logical channels)	Implementation requirement			
	SPECint95		SPECfp95	
	Min	Max	Min	Max
1	1.1	2	1.4	2
2	3.3	5.6	3.7	5.6
4	10	17	11	17
8	34	57	40	58

Table 2. *Processing requirement for a GSM modem without equalizer, with consideration given to processor partitioning. For best implementation efficiency, partitioning should be kept to a minimum. (Turletti & Tennenhouse, 1999).*

Sample BW	5 MHz	10 MHz	15 MHz	25 MHz
2x oversample	40 Mbytes/s	80 Mbbytes/s	120 Mbytes/s	200 Mbytes/s
4x oversample	80 Mb/s	160 Mb/s	240 Mb/s	400 Mb/s

Table 3. *Stream bandwidths per RF stream for 16-bit I and Q data, assuming 2x or 4x oversampling, range from 40 to 400 Mbytes/s.*

tioning.) New architectures such as the PowerPC/G4 with integrated 128-bit vector processors permit efficient implementation of software radio algorithms with minimal partitioning.

A third design consideration is the performance of wideband digitizers. To meet GSM and IMT-2000 specifications, analog–digital converters (ADCs) require true 14-bit performance, and support a sustained sample rate of at least 20 megasamples/s with a spur-free dynamic range (SFDR) in excess of 80 dB. Minimum bandwidths of 40 Mbytes/s assuming 4 bytes per complex sample (I and Q) must be supported (Table 3). Maximum stream bandwidths may range as high as 400 Mbytes/s for 25 MHz wideband designs.

A fourth design consideration is the need for high-performance I/O, both between processors on a circuit board and between circuit boards. Numerous adaptive applications like MUD, 2D RAKE, and adaptive antennas are I/O-intensive and sensitive to latency. Industry estimates of interprocessor I/O bandwidths required to implement certain adaptive processing algorithms such as multistage PIC and fully adaptive antennas exceed 1 Gbyte/s. The low-latency, high-bandwidth crossbar fabrics and multiprocessing with port-to-port switching times of 100 ns or less may be used to meet these requirements. Off-board I/O between the channel modem and other base station "layers," such as link processing, source coding, and internetworking, are implemented using one or more asynchronous transfer mode (ATM), Ethernet, SCSI, or Firewire interconnections in modern base station designs. These interfaces typically handle bandwidths of 100 Mb/s or more per line.

"Super Chips"

Practical implementation of smart antennas and adaptive modems benefit from the availability of high-performance low-cost components on monolithic silicon (i.e., "super chips"), including:

- RISCs, digital signal processors (DSPs), application-specific inegrated circuits (ASICs), and field programmable gate arrays (FPGAs) which offer over 1 Gflop (or fixed-point equivalent) per device
- High-density FPGAs offering one million or more gates per device
- I/O devices capable of digitizing, tuning, and filtering 2G and 3G signal channels
- Highly integrated devices such as the PowerQUICC II or Star*Core combining RISC or DSP cores with communications processors and I/O fabric gateways
- New I/O fabrics using crossbar switches with over 1 Gbyte/s bandwidth per device

Processors

Low-latency processing is needed to meet air interface synchronization requirements, avoid degradation of beamforming performance, and eliminate intolerable delays in digitized speech and video. High processing bandwidth can eliminate or minimize partitioning, which reduces implementation cost and complexity. When algorithms can be parallelized (as in the case of OFDM, MUD, and STAP), improvements in real-time computing speed may also be obtained by parallel execution of multiple data streams.

Powerful new RISC processors, such as the 3.2 Gflop MPC7400 PowerPC/G4 with 128-bit vector processor, have recently emerged as ideal implementation platforms for software radio. While the Alpha and Pentium III processors may offer comparable fixed-point or floating-point performance to the PowerPC, those devices also consume substantially more power (Table 4). The new RISCs offer numerous implementation advantages over traditional DSPs, such as ease of programmability, cross-platform software portability and FFT performance. Using such a processor, researchers successfully implemented a 19.7 Mb/s OFDM modem using a single 375 MHz PowerPC/G4 [15].

High-Density FPGAs

While ASICs may continue to be the technology of choice for high-volume production implementations, new high-density, high-speed reconfigurable logic devices may aid the designer in prototype development. An example is the Xilinx Virtex, a new high-density FPGA offering devices with up to 1,000,000 system gates (27,648 logic

cells) on monolithic silicon. The chip offers over 500 user I/O pins. Using a 2.5-V, 0.22 μ, five-layer complementary metal oxide semiconductor (CMOS) process, this super-FPGA features compile times of 200,000 gates/hr, making "overnight" reprogramming for base stations feasible.

I/O Devices

New I/O devices with high levels of integration have also made SDR base stations more practical to implement. Examples of these new I/O devices are shown in Table 5.

Another useful device class is the highly integrated combination of RISC or DSP cores and I/O peripherals on monolithic silicon. Examples include:

- MPC8260 PowerQUICC II (200 MHz, PowerPC 603e RISC core, ATM, Ethernet, SCSI, PCI bridge)
- MPC8101 Star*Core (300 MHz, 16-bit fixed point DSP core, ATM, Ethernet, SCSI, PCI bridge)
- TMS320-C6205 (200 MHz, 16-bit fixed point DSP core, PCI bridge)

Future examples of these highly integrated devices may also include "glueless" interfaces to high-performance I/O fabrics, further reducing implementation costs.

High-Speed Crossbar Fabrics

An open standard method for implementing high speed fabrics is RACEway (ANSI/VITA 5-1994). RACEway has been used to implement several experimental smart antenna and adaptive processing systems. The high processor-to-processor bandwidth provided by crossbar fabrics is essential for implementing adaptive methods such as MUD and fully adaptive antenna processing. Crossbar fabrics can also be used to reconfigure data flows between processing elements. Such reconfiguration may be necessary to change a smart-antenna-equipped base station from time-division multiple access (TDMA) to CDMA air interfaces (e.g., GSM to W-CDMA conversion).

These "super chip" components may be employed in the design of a *software-reconfigurable, scalable* IMT-2000 channel modem, using the "pool of processors" approach (Fig. 1). A "building block" approach may be economically employed in a range of 2G/3G applications, starting with a single-board "minicell" modem, and scaling up as required for higher-volume macrocell designs, smart antennas, and adaptive processing as additional capacity and features are required. The following configurations, while conceptual, are feasible using available components.

Minicell IMT-2000 Base Station Modem — Features: 560 MIPS, onboard 32-bit RISC processing plus Virtex, implemented on a single 6U-sized card. It can be programmed to support multiple 2G and 3G air interfaces, including IS-136 TDMA, IS-95 CDMA, GSM, and W-CDMA. Can be scaled up to basic configuration (#2) by addition of one quad PPC/G4 circuit card. PowerQUICC II's embedded I/O capability includes up to 2x PCI — for use with PCI mezzanine cards (PMC) or backplane bus — 4x ATM, 2x Ethernet, 2x SCSI, and 2x DUART. Components include:

Processor	MHz	Watts	SPECint95	SPECfp95
PPC G3	400	6	18.8	12.2
PPC G4	400	8	21.0	21.0
Sun Ultra 10	360	20	15.2	19.9
Pentium III	500	28	20.6	14.7
Alpha	600	46	18	27
TI-C62XX	200	1.2	1600 MIPS	—
Star*Core	300	0.5	3600 MIPS	—

Table 4. *Processor comparison. A balance of good performance with low power, as exhibited by the new MPC-7400 PowerPC G4 and Star*Core, are desirable features when designing software radio modems.*

- 2x MPC8260 PowerQUICC II
- 1x Virtex FPGA
- 1x RACE++ crossbar

Basic IMT-2000 Base Station Modem — Features: 12 Gflops onboard 32-bit RISC processing plus Virtex, implemented on a two 6U-sized circuit cards. It is imilar to the minicell modem, but has increased system capacity. It can be scaled up to the adaptive version (#3) by addition of four quad PPC/G4 circuit cards for additional processing. Components include:

- 2x MPC8260 PowerQUICC II
- 1x Virtex FPGA
- 4x MPC7400 PowerPC/G4
- 2x RACE++ crossbar

Adaptive IMT-2000 Base Station Modem — Features: 60 Gflops onboard processing, implemented on six 6U-sized circuit cards. It supports multiple 2G and 3G air interfaces, including IS-136 TDMA, IS-95 CDMA, GSM, and W-CDMA. It supports adaptive processing algorithms such as multistage PIC or GSIC for MUD, smart antennas, and joint methods. Components include:

- 2x MPC8260 PowerQUICC II
- 1x Virtex FPGA
- 20x MPC7400 PowerPC G4
- 6x RACE++ crossbar

Conclusions and Recommendations

Using software radio techniques and recently developed "super chips," practical implementation of software-reconfigurable IMT-2000 modems featuring smart antennas and other space-time adaptive methods has become feasible. While reducing overall computational complexity, these methods may involve iterative or serialized computations which require parallel multiprocessing to keep processing delays tolerable. While requiring fewer "chips" to implement, high chip-to-chip I/O bandwidth with short transfer latencies should be provided between multiprocessing streams. Future "super chips" may soon include on-chip interfaces to crossbars, satisfying this demand for interprocessor bandwidth while further reducing implementation costs.

Using software radio techniques and recently developed "super chips," practical implementation of software-reconfigurable IMT-2000 modems featuring smart antennas and other space-time adaptive methods has become feasible.

Device type	Model, manufacturer	Required features	Advertised performance
Wideband A/D Converter	AD6644 Analog Devices	20 MSPS 14-bit 80 dB SFDR	65 MSPS 14-bit 90 dB SFDR 100 dB w/dither
Quad Digital Receiver	GC4014 Graychip	14-bit 25 MHz 1 channel	14-bit 62 MHz 4 channels
CDMA Receiver	CSM2000 QualComm	IS-95 CDMA RAKE 1 user	IS-95 CDMA 4-finger RAKE 8 users
Crossbar I/O Fabric	RACE++ Mercury Computer	200 MB/s/port; 100 ms latency	266 MB/sec/port 75 ns latency; 8 ports
Integrated RISC + Comms Processor + PCI	MPC8260 Power-Quicc II Motorola	PCI Bridge ATM Ethernet SCSI Serial RISC Core	PCI-C Bridge 2x ATM 100BT Ethernet SCSI 2x Serial PPC 603e RISC
Integrated DSP + Comms Processor + PCI	MSC8101 Star*Core Motorola	PCI Bridge 2x ATM Ethernet SCSI Serial DSP Core	PCI-X Bridge 2x ATM 100 BT Ethernet SCSI 2x Serial Star*Core DSP
Integrated DSP+ PCI	C6205 TI	PCI Bridge DSP Core	PCI Bridge TI C62 DSP

Table 5. *New I/O devices, including chips which combine communications processors and PCI bridges with DSP or RISC cores, simplify implementation of software-reconfigurable 3G base station modems.*

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DAVID MUROTAKE (dmurotake@mc.com) is the digital wireless architect at Mercury Computer Systems, Inc. He leads the company's development of real-time, embedded multiprocessing solutions for third-generation base stations and other digital wireless platforms. A graduate of MIT (1975), he received Bachelor's and Master's degrees in electrical engineering and computer science, a Bachelor's degree in English literature and creative writing, and a Ph.D. in management of technological innovation from the MIT Sloan School of Management. Over the past 25 years, he has been a practitioner in numerous engineering disciplines with the U.S. Army, RCA, GE, Lockheed, and Mercury Computer. Over the past decade, he has been a champion of software radio and spread spectrum technology, and is active with the SDR Forum, an international industry organization promoting architectures and standards for software-defined radios. He chairs the Forum's base station working group. A past U.S. delegate to the ITU, he has contributed to ITU Radiocommunications Standardization Sector (ITU-R) standards recommendations for spread spectrum radio in fixed service, and IMT-2000 3G technology in mobile service.

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