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Microporous SiO_2 with huge electric-double-layer capacitance for low-voltage indium tin oxide thin-film transistors

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Electric-double-layer (EDL) effect is observed in microporous SiO_2 dielectric films deposited at room temperature by plasma-enhanced chemical vapor deposition method. Indium tin oxide thin-film transistors gated by such microporous SiO_2 gate dielectric are fabricated at room temperature, and a low operating voltage of 1.5 V is obtained due to the huge EDL specific capacitance (2.14 $\mu F/cm^2$). The field-effect electron mobility is estimated to be 118 $cm^2\ V^{-1}\ s^{-1}$. Current on/off ratio and subthreshold gate voltage swing are estimated to be 5×10^6 and 92 mV/decade, respectively. Room-temperature deposited microporous SiO_2 dielectric is promising for low-power field-effect transistors on temperature sensitive substrates. © *2009 American Institute of Physics*. [doi:10.1063/1.3271029]

In field-effect thin-film transistors (TFTs), the semiconductor channel is insulated from the gate electrode by a dielectric layer, and the gate/dielectric stack is responsible for inducing mobile charges in the active channel.[1] While extensive consideration has been given to new semiconducting channels with respect to understanding and improving performance, little attention has been paid to the gate dielectric.[2,3] At the same time, low-voltage TFTs operation is of intense current interest for many reasons, particularly for low power application and portable electronics.[4,5] In general terms, the performance of TFTs can be improved by using gate dielectric with higher specific capacitance.[6] The benefits of higher specific capacitance are (1) much higher output current at a given applied gate voltage and (2) much lower operating voltages; both are a direct consequence of the large two-dimensional electron density that can be induced in the channel by means of the high specific capacitance.

In order to get higher specific capacitance for low-voltage operation, thinner SiO_2 and insulators with high dielectric constant are used as the gate dielectrics.[7–10] For example, the operating voltage of $InGaZnO_4$ TFTs gated with amorphous $BaSrTiO_3$ was reduced down to 3.0 V.[11] Another interesting approach to achieve low-voltage operation is using ion gel or ionic liquid as gate dielectrics.[12–14] For example, low-voltage organic transistors gated by ionic liquids operating at 1.0 V were demonstrated due to the electric double layer (EDL) formation.[12] In this letter, microporous SiO_2 with EDL effect was deposited by plasma-enhanced chemical vapor deposition (PECVD) method at room temperature. The room-temperature processed indium tin oxide (ITO) TFTs gated by such microporous SiO_2 dielectric showed a low operating voltage of 1.5 V due to the high specific capacitance (2.14 $\mu F/cm^2$). The mobility, current on/off ratio, and subthreshold swing were estimated to be 118 $cm^2/V\ s$, 5×10^6, and 92 mV/decade, respectively.

Microporous SiO_2 films with the thickness of about 8.0 μm were deposited on n^+-type Si (100) substrates by PECVD using SiH_4 and O_2 as reactive gases at room temperature. The flow rate ratio of SiH_4/O_2 was 5:18 SCCM (SCCM denotes standard cubic centimeter per minute at STP). The deposition pressure and deposition time were 25 Pa and 1 h, respectively. Coplanar homojunction TFTs with ITO channel layer were fabricated and characterized. First, 50-nm-thick ITO channel layers were deposited on the microporous SiO_2 dielectric by radio frequency (rf) magnetron sputtering in Ar/O_2 mixed ambient at 0.5 Pa. Then, highly conductive ITO source and drain electrodes with the thickness of 100 nm were deposited by rf magnetron sputtering and patterned using a nickel shadow masks in pure argon ambient at 0.5 Pa. The channel length and width-to-length ratio of the TFTs were 80 μm and 5:1, respectively. The entire process of device fabrication was performed at room temperature. The structural characterization of the microporous SiO_2 was investigated by field emission scanning electron microscopy (Hitachi S-4800 SEM). The electrical characterizations of the microporous SiO_2 dielectric and ITO-based TFTs were investigated by an impedance analyzer (Agilent 4292A) and a semiconductor parameter analyzer (Keithley 4200 SCS) at room temperature.

Figure 1(a) shows a cross-section SEM image of the as-deposited SiO_2 film, and its thickness is found to be ~8.0 μm. The inset in Fig. 1(a) shows a high-resolution SEM image of the SiO_2 dielectric. A microporous structure with high-density nanoclusters is clearly observed. A microporous material is a material containing pores with diameters less than 2.0 nm.[15] The capacitance-frequency (C-f) curve in 40 Hz–10 kHz range is presented in Fig. 1(b). The inset of Fig. 1(b) is the schematic diagram of $ITO/SiO_2/n^+$-Si sandwich structure for capacitance measurement. Although the physical thickness of the microporous SiO_2 was 8.0 μm, the measured specific capacitance is as large as 2.14 $\mu F/cm^2$ at 40 Hz. It was also found that it decreased with increasing frequency and reduced to 16.6 nF/cm^2 at 10 kHz. The relationship between the capacitance and frequency is in good agreement with that of the ion gels or SiO_2 deposited by PECVD using SiH_4 and O_2 as reactive gas.[12,16] The main contributions to the capacitance at low frequencies are interpreted to be the response of

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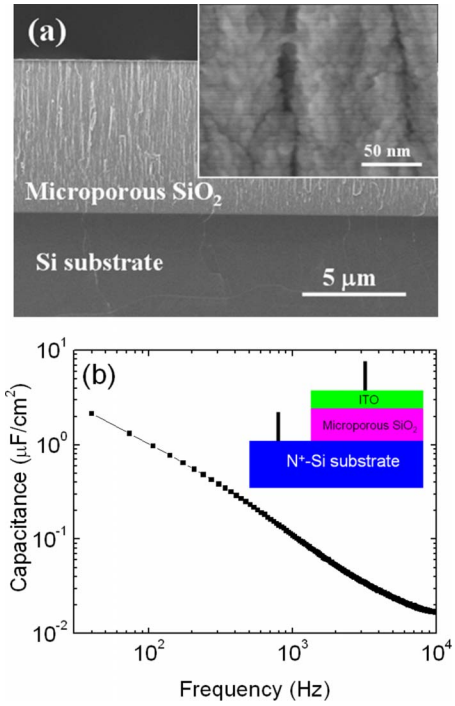

FIG. 1. (Color online) (a) Cross-section SEM image of microporous SiO_2 dielectric film deposited at room temperature by PECVD method. Inset in (a) shows a HR-SEM image of the microporous SiO_2 dielectric. (b) Specific capacitance as a function of frequency from 40 Hz to 10 kHz for an 8.0-μm-thick microporous SiO_2 film. Inset shows the schematic diagram of ITO/SiO_2/n^+-Si sandwich structure for capacitance measurement.

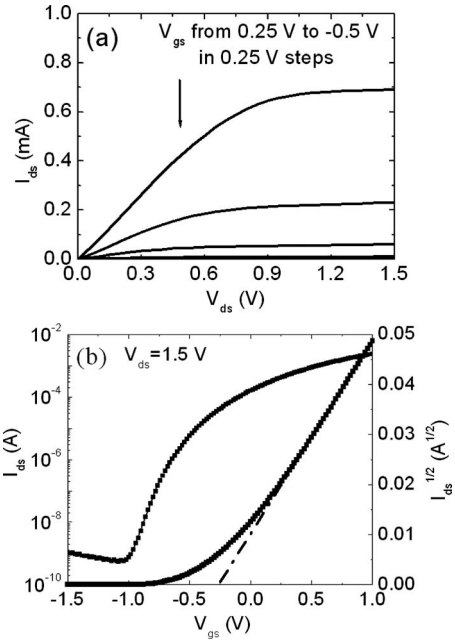

FIG. 2. Electrical characteristics of ITO-based TFTs gated by microporous SiO_2 dielectric processed at room temperature. (a) Output characteristics of the device. V_{ds} was swept from 0 to 1.5 V at each V_{gs} varied from 0.25 to −0.5 V at −0.25 V steps. (b) Transfer characteristics (drain-to-source current I_{ds} vs gate voltage V_{gs} and square root of I_{ds} vs V_{gs}) at V_{ds}=1.5 V.

the EDL formed at the SiO_2/ITO channel interface. The frequency dependence of the microporous SiO_2 capacitance is strong because the proton mobility in microporous SiO_2 with the thickness of 8.0 μm can limit the speed of this TFTs switching, which requires the migration of protons to form the EDL. In fact, a 150-nm-thick thermally oxidation dense SiO_2 only has a capacitance of ~20 nF/cm^2 and is weakly dependent on frequency. Our results also indicate that SiO_2 deposited at higher SiH_4 flow rate shows larger specific capacitance at low frequency. It is likely that high SiH_4 flow rate would result in a high porosity and more protons in SiO_2 films, which are of great significance for EDL formation.

The electrical characteristics of the ITO-based TFTs gated by the microporous SiO_2 dielectric were measured in air ambient. Figure 2(a) shows the output characteristics (I_{ds}-V_{ds}) with V_{gs} varying from −0.5 to 0.25 V in 0.25 V steps. The device exhibited an n-type characteristic with a "hard" saturation below 1.5 V. The output curves displayed good Ohmic contacts, and a saturation current of 714 μA was obtained at a V_{ds}=1.5 V and V_{gs}=0.25 V. And the hard saturation also reveals that the Fermi level in the channel is effectively controlled by the gate and drain voltages. Figure 2(b) shows the transfer characteristics (drain-to-source current I_{ds} as a function of the gate voltage V_{gs} and square root of I_{ds} versus V_{gs}) measured at V_{ds}=1.5 V. The TFT exhibited a very small subthreshold swing of 92 mV/decade calculated by $S=dV_{gs}/d(\log I_{ds})$ and a high current on/off ratio of about 5×10^6. The V_{th} of −0.25 V was determined by fitting a straight line to the plot of the square root of I_{ds} versus V_{gs} in this figure.

The saturation field-effect electron mobility (μ_{FE}) is estimated by the following equation:

$$I_{ds}=\left(\frac{\mu_{FE}WC_{OX}}{2L}\right)(V_{gs}-V_{th})^2,$$

where C_{OX} is the areal dielectric capacitance. For C_{OX} calculation, the physical thickness (8.0 μm) of the microporous SiO_2 film cannot be used as traditional calculation methods. Here, the measured value 2.14 μF/cm^2 of C_{OX} was used. At the same time, in the case of small channel ratios, the effective channel width was not equivalent to the geometrical channel width but was extended somewhat because of the fringing electric field at the ends of the electrodes, which could lead to the overestimation of the field-effect mobility. The field-effect mobility of undefined TFTs becomes overestimated by about 241% at the small geometrical channel ratio of 5.5.[17] Thus, the calculated mobility was 118 cm^2 V^{-1} s^{-1}, which is much higher than that of the oxide-based TFTs gated with traditional dielectrics.[18,19] It is likely that two-dimensional electron gas formation near the dielectric/channel interface related to the EDL effect is of great help for this high mobility value.

In general, during the PECVD process, the hydrogen dissociated from SiH_4 in the plasma can enter the microporous SiO_2 dielectric layer, which can induce some mobile charges in SiO_2 layer as reported in the literature.[16] However, bare proton should not exist in a-SiO_2. The most often referred to as the "proton" is almost certainly associated with a bridging oxygen atom to form a three-coordinate oxygen center (Si−OH$^+$−Si).[20] The schematic diagram of the working mechanism for the EDL TFTs is shown in Fig. 3, which can be described as follows. Basically, an "on" state or "off" state of the TFTs is induced by applying an electric field across the gate oxide to place the protons either at the microporous SiO_2/ITO channel interface or at the microporous SiO_2/gate electrode interface where they remain stable after testing for many times. When a positive gate voltage is ap-

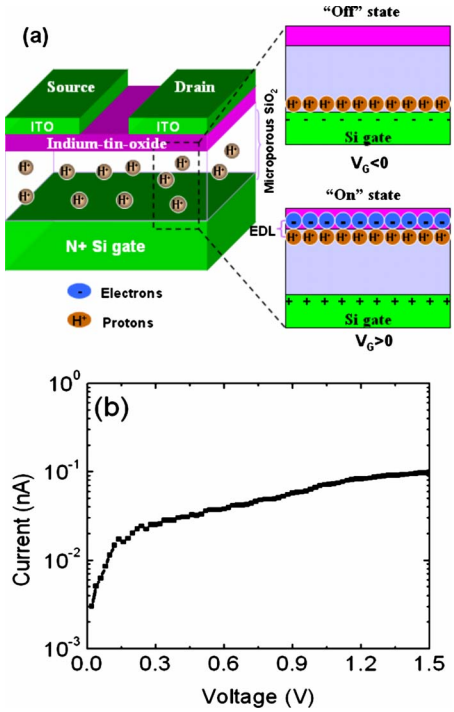

FIG. 3. (Color online) (a) Schematic diagram of EDL formation and low-voltage operation mechanism of the ITO-based TFTs gated by microporous SiO_2 dielectric. When a negative gate voltage is applied to the gate electrode, protons will move to the gate electrode/dielectric interface and the device is turned off. When a positive gate voltage is applied, protons move to a thin boundary layer at the SiO_2/ITO channel interface, and the device is switched on. (b) Leakage current curve of the 8.0-μm-thick microporous SiO_2 film deposited by PECVD at room temperature.

plied, protons move to a thin boundary layer at the SiO_2/ITO channel interface, and the resulting positive charges induce image charges of equal density and opposite sign in the ITO channel layer, which is similar to the case of the EDL formation in organic transistors gated by ionic liquids.[12] This huge EDL gate capacitance of 2.14 $\mu F/cm^2$ results in a very low operating voltage of 1.5 V and a high electron field-effect mobility.

Figure 3(b) shows the leakage current of the microporous SiO_2 film deposited by PECVD. The leakage current is ~0.1 nA at 1.5 V bias, which is much smaller than that of the solid polymer electrolytes or ionic liquids.[12–14] This is likely due to the electrochemical silence and the small ionic current in microporous SiO_2. Despite the porosity in gate dielectric, the leakage current is seven orders of magnitude smaller than the channel current, which guarantees the field-effect performance will not be affected by the leakage.

In conclusion, huge EDL specific capacitance of 2.14 $\mu F/cm^2$ was measured in microporous SiO_2 deposited by PECVD method at room temperature. Coplanar homojunction ITO-based TFTs gated with such microporous SiO_2 were fabricated at room temperature. The operating voltage was found to be as low as 1.5 V due to the extraordinary strong EDL capacitive coupling. The field-effect mobility, current on/off ratio, and subthreshold gate voltage swing were found to be 118 $cm^2 V^{-1} s^{-1}$, 5×10^6, and 92 mV/decade, respectively. These low-voltage TFTs deposited at room temperature were very promising for low-power circuit applications.

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