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Lateral heating of SiO_2/Si: Interfacial Si structure change causing tunneling current reduction

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Lateral heating processing of SiO_2/Si samples can reduce the tunneling current of SiO_2 by 5 orders of magnitude with very good reproducibility. There is a strong correlation between the flatband voltage shift of metal-oxide-semiconductor capacitors and the tunneling current reduction. Analysis of the flatband voltage shift suggests that origin of the tunneling current reduction after lateral heating is caused by the structure change of Si, most likely tensor strained Si, near the SiO_2/Si interface. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4709418]

HfO_2 based high-k gate oxide stack is used in complimentary metal-oxide-semiconductor (MOS) technology-based integrated circuits. An interfacial SiO_2 layer is used between HfO_2 and silicon to assure high-quality insulator/silicon interface.[1,2] Therefore, improving both the SiO_2 layer and the SiO_2/Si interface is very important for the high-k gate oxide stacks. In the past, we reported observation of phonon-energy coupling enhancement induced by rapid thermal processing (RTP) of the SiO_2/Si using infrared spectroscopy.[3,4] Large tunneling current reduction (~5 orders of magnitude) across SiO_2 (2-3 nm thick) was also observed accompanying the phonon energy coupling enhancement.[3,4]

However, we could only reproduce leakage current reduction of 2–3 orders of magnitude for SiO_2 and silicon oxynitride.[5–7] It was very difficult to reproduce the best results (4–5 orders). In addition, how could phonon-energy coupling enhancement cause the tunneling current reduction? It is of critical importance to understand what causes the reduction of tunneling current from the material structure point of view. In this Letter, we report a sample heating process by which much better results can be obtained reproducibly, and then study the material structure through electrical characterization.

We designed two approaches for realizing lateral heating process (LHP). The first one was a sandwich structure to heat the sample laterally as shown in Fig. 1(a). The substrate holder (4 in. Si wafer) was much larger than the sample ($\sim 1 \times 0.5$ in^2.) and the radiation blocker that was just slightly larger than the sample. The bottom supporter was much larger than the top supporter. The second one was to modify the conventional RTP equipment by turning off the top lamps (See Fig. 2(b)). In these setups, the samples were completely isolated from the light radiation. Because the heat generation was dependent on the area exposed to light, most heat was generated in the substrate holder, because it is large. The heat flows from the substrate holder to the sample. In this arrangement, the heat flows laterally from the contact area to the edge and material structure change due to thermal stress is maximized.

Si (100) 2-in. wafers were prepared using conventional Radio Corporation of America (RCA) cleaning. The wafers were loaded in furnace at 900 °C and oxidized at 900 °C in N_2 with 6% O_2 for ~20 s to obtain a SiO_2 film of ~22 Å. After oxidation, wafers were cut into quater pieces. Some pieces were used as control samples without further processing and other pieces were subjected to the LHP processing in the above setups at 1050–1080 °C in helium containing 200–300 ppm O_2. After processing, Ni gate MOS capacitors were fabricated using a bi-layer resist lift-off process as described in Refs. 6 and 7.

Capacitance-voltage (C-V) measurements were carried out on the control and LHP-processed samples (See Fig. 2(a)). There was no hysteresis observed in C-V curves. Berkeley quantum simulator was used for C-V simulation to fit the experimental C-V data to obtain the oxide thickness and the flatband voltage. The current-voltage (I-V) measurements were also carried out on the same control and LHP samples. The control oxide of 2.2 nm exhibits a leakage (tunneling) current density of 6×10^{-1} A/cm^{-2} at V-$V_{FB} = 1$ V, where the flatband voltage (V_{FB}) is 0.86 V (see Fig. 2). LHP processes were carried out at 1050–1080 °C for 45 s in ~200–300 ppm O_2 in the setting shown in Figures 1(a) and 1(b). Most good results were from devices in the hanging areas of the processed samples. ***The most striking finding is that there is a strong correlation between the faltband voltage (V_{FB}) shift and the tunneling current reduction***. From Figure 2(a), it can be found that the flatband voltage is shifted toward left after lateral heating, comparing with the control sample. The corresponding tunneling current is shown in Figure 2(b). The more flatband voltage shift, the lower tunneling current the MOS capacitor exhibits (see Fig. 2). After V_{FB} was shifted by 0.86 V, the leakage current density of SiO_2 at V-$V_{FB} = 1$ V ($V_{FB} = 0$ V) becomes 2×10^{-7} A/cm^2, which is 6.5 orders of magnitude reduction comparing with the control oxide (see Fig. 2(b)). However, the oxide thickness was increased by 3 Å after the LHP processing, corresponding to 1.5 orders of magnitude reduction due to the thickness increase. Therefore, we reproducibly demonstrate using the LHP process that the leakage current of SiO_2 can be reduced by **5 orders of magnitude** ($10^5\times$).

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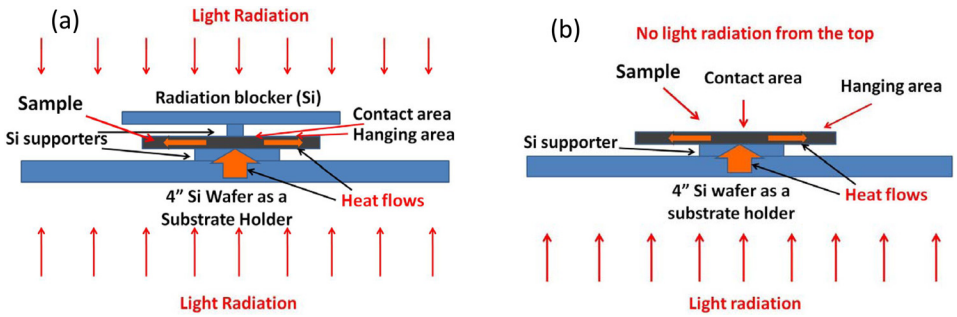

FIG. 1. (a) In a RTP chamber, a sandwich structure for lateral heating of a sample was used, where radiation from the top was blocked out. (b) The RTP equipment was modified for lateral heating of a sample by turning off the radiation from the top lamps. In both cases, there is no direct radiation on the sample, and the sample was heated by heat flows from the substrate holder. Most good results were from the hanging areas not from the contact area.

Using electrical characterization and modeling, we are able to study the interfacial material structure change. The flatband voltage can be described by the following equation:[8]

$$V_{FB} = \Phi_{MS} - \frac{Q_{it}}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{T_{ox}} \frac{x}{T_{ox}} \rho(x) dx, \qquad (1)$$

where $q\Phi_{MS} = q\Phi_M - q\Phi_S$ is the work-function difference between the gate metal (Ni) and silicon; Q_{it} is the interface trap charges; C_{ox} is the oxide capacitance per unit area; T_{ox} is the oxide thickness, and $\rho(x)$ is the oxide charge, which may be distributed along the thickness of the oxide.

According to Eq. (1), there are only two factors that affect the flatband voltage V_{FB}. One is the charges inside the gate oxide $\rho(x)$ and at the interface Q_{it}, and the other one is the work-function difference $q\Phi_{MS} = q\Phi_M - q\Phi_S$. Is there any possibility that the charges $\rho(x)$ were introduced into the samples due to contamination or repairing oxygen vacancies by reoxidation after LHP? Let us first exam contamination by studying samples processed in the LHP setting in Fig. 1(b). We exam C-V curves at two locations on the same sample, the hanging area and the contact area (see Fig. 1(b)), after the LHP process. Figure 3(a) shows that V_{FB} of the MOS capacitors at the contact area (near the center of the sample) has no shift, i.e., it is the same as that (0.86 V) of the control sample (also see Figure 2(a)), while that in the hanging area has a large shift (−0.86 V), because V_{FB} became zero after the shift. It should be noted that these happened on the same sample subjected to the same process in the same chamber at the same time (see Fig. 1(b)). If the flatband voltage shift were caused by charges introduced due to contamination during the process, there would have been charges everywhere on the sample, so that the flatband voltage in both hanging and contact areas would have shifted. However, comparing with the control sample, there is no flatband voltage shift in the contact area, but a large shift in the hanging areas (see Fig. 3(a)). Thus, samples were not contaminated. Then, let us consider the possibility for repairing oxygen vacancies by reoxidation because in the hanging part the oxide is 2 Å thicker than that in the contact area (see Fig. 3(a)). It is well known that for ultrathin SiO_2 thin film (<3 nm), there are few oxygen vacancies or little bulk oxide charge. In addition, oxygen vacancies exhibit positive charges. After repairing oxygen vacancies, positive charges in the oxide would have been reduced, so that the flatband

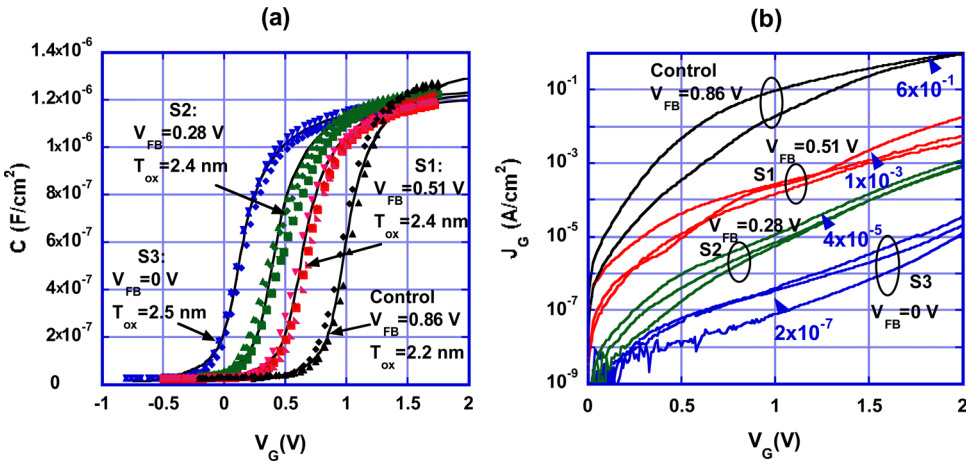

FIG. 2. (a) Experimental (dots) and simulated (lines) C-V curves of the Ni/SiO_2/n-Si MOS capacitors in the hanging areas of samples before (control) and after lateral heating. Sample S1 was processed at 1050 °C for 10 s in helium containing ~300 ppm O_2 in the setting in Fig. 1(a). Sample S2 was processed at 1070 °C for 10 s in helium containing ~250 ppm O_2 in the setting in Fig. 1(a). Sample S3 was processed at 1050 °C for 45 s in Helium containing ~200 ppm O_2 in the setting in Fig. 1(b). Three devices (▲ ■ ♦) in each processed sample and two devices (▲ ♦) in the control sample were tested for repeatability. Berkeley quantum simulator was used for C-V simulation. (b) I-V curves of the same Ni/SiO_2/n-Si MOS capacitors as shown in (a). The marked current is obtained at $V_G = V_{FB} + 1$ V.

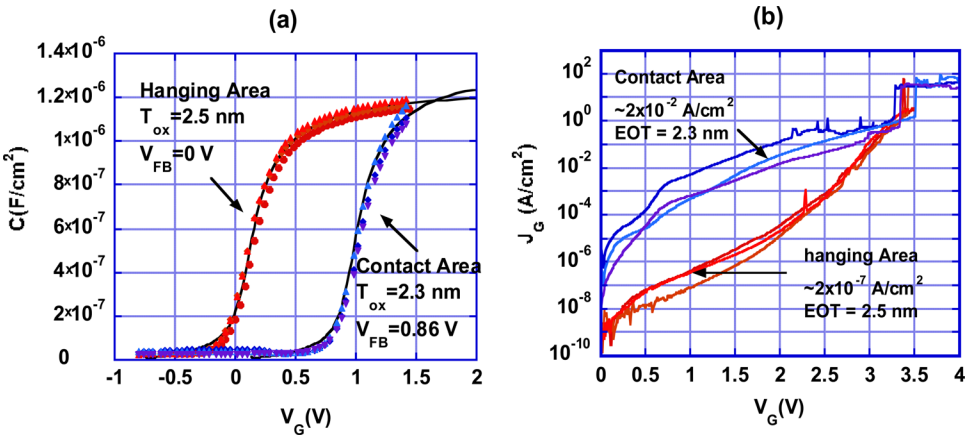

FIG. 3. (a) Experimental (dots) and simulated (lines) C-V curves of Ni/SiO_2/n-Si MOS capacitors in the contact area and the hanging area after lateral heating in the setting shown in Fig. 1(b) at 1050 °C for 45 s in Helium containing ~200 ppm O_2. Three devices (● ▲ ◆) in the hanging area and three devices (▼ ▲ ◆) in the contact area were tested for repeatability. Berkeley quantum simulator was used for C-V simulation. (b) I-V curves of the same Ni/SiO_2/n-Si MOS capacitors as shown in (a).

voltage would have shifted toward the right hand side in Fig. 3(a) after LHP. However, this is opposite to our result in Fig. 3(a). Therefore, charges inside the oxide $\rho(x)$ are 0.

Is it possible that the flatband-voltage shift was caused by the interface trap charges Q_{it}? From the Figures 2(a) and 3(a), it can be found that the C-V curves after LHP still remain in good shape, which is very similar to that of the control sample. Therefore, the interface quality of the samples remains the same after LHP. For a regular quality SiO_2 (the control sample), its interface trap density N_{it} is $\sim 2 \times 10^{10}\,cm^{-2}$ and thus its interface charges $Q_{it} = qN_{it}$ is $1.6 \times 10^{-9}\ cm^{-2}$. Therefore, the flatband-voltage shift caused by Q_{it} itself is given by

$$\Delta V_{FBit} = -\frac{Q_{it}}{C_{ox}} \approx -1.3 \times 10^{-3} V. \quad (2)$$

It is only 1.3 mV, which can be ignored, comparing with the large shift due to the process.

If V_{FB} shift is not caused by charges, there is only one possibility, i.e., the work-function difference, $q\Phi_{MS} = q\Phi_M - q\Phi_S$, has been changed after LHP process. Because the metal gate (Ni) was deposited on SiO_2 after the LHP process, the metal work function $q\Phi_M$ does not change. Therefore, it must be the silicon work function Φ_S that has changed after the LHP process. Therefore, for ultrathin SiO_2 without contamination, the flatband voltage can be expresses as

$$V_{FB} = \Phi_{MS} = \Phi_M - \Phi_S. \quad (3)$$

We can use the experimental data to verify Eq. (3). For our control sample as shown in Figure 2(a), $V_{FB} = 0.86$ V. The work function of Ni metal $q\Phi_M$ is ~5.15 eV. The Si work function is dependent on the location of Fermi level (doping). Our control Si was n-type Si with a doping level of $1.5 \times 10^{16}\,cm^{-2}$. The energy from the Fermi level to the conduction band edge is $E_C - E_F \approx 0.25$ eV. Therefore, for our control Si sample, $q\Phi_S = q\chi + (E_C - E_F)$, where $q\chi$ is the electron affinity of Si, which is ~4.05 eV. This results in $q\Phi_S \approx 4.30$ eV. Finally, $V_{FB} = \Phi_{MS} = \Phi_M - \Phi_S \approx 0.85$ V, which is in agreement with our experimental value, 0.86 V.

From Eq. (3), it is clearly seen that $q\Phi_S$ must have been changed after the LHP process. Because the flatband voltage was shifted toward negative direction (see Figs. 2(a) and 3(a)), according to Eq. (3), $q\Phi_S$ must have increased, so that the conduction band E_c of Si is decreased (see Fig. 4). In order to understand the valence band, we also studied C-V curves of MOS capacitors based on p-Si after LHP process,[6] because the Fermi level of p-Si is more close to valence band edge (E_v). From our experiments, there was no flatband voltage shift for C-V curves on p-type Si after LHP.[6] Therefore, the valence band is not changed after LHP. This is illustrated schematically in Figure 4. It is clear that the energy band gap of Si has to be decreased (see Fig. 4). ***Because of the conduction band edge (E_c)of Si is decreased, the energy barrier between SiO_2 and Si (ΔE_c) is increased so that the tunneling barrier is increased, resulting in tunneling current reduction!***

In the above analysis (See Eq. (3)), no SiO_2 parameters are involved in. Therefore, the observed phenomena have nothing to do with SiO_2. Therefore, it can be inferred that the structure of Si was changed because the Si work function $q\Phi_S$ was changed after LHP. It is unlikely that the crystal structure of the entire Si substrate was changed after LHP. We carried out regular x-ray diffraction analysis of the samples and found no difference between the control sample and the LHP processed sample. Therefore, it is likely that the Si structure near the SiO_2/Si interface has changed after LHP. There are several reports about formation of strained Si near the SiO_2/Si interface after thermal oxidation in furnace.[9–12] It was suggested that the tensor strained Si near the SiO_2/Si interface was caused by the compress stress in the transistion

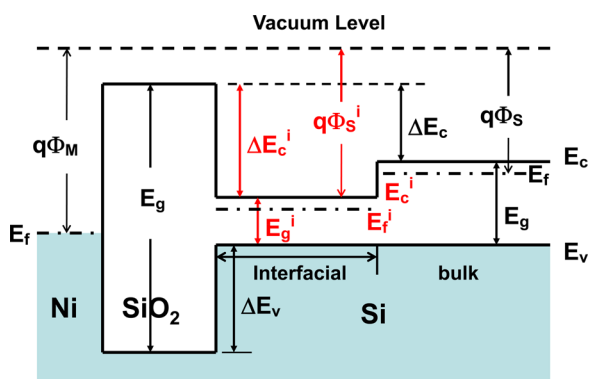

FIG. 4. Schematic band structure of a Ni-gate MOS capacitor after high temperature lateral heating processing, where Si structure at the interfacial region is changed due to strain or stress.

layer in SiO_2 near the interface.[9] In the transition layer, the SiO_2 network is believed to be compressed due to a large volume expansion upon oxidation.[13,14] The Si lattice distortion at the SiO_2/Si interface can propagate more than 2 nm from the interface.[9] In our early report,[5] the transmission electron microscope (TEM) image (Figure 2 in Ref. 5) clearly showed that the silicon structure was different near the SiO_2/Si interface after processing. At that time, we did not have LHP and the sample was processed in RTP, where the structure change could be much less than what we have now. The results in the above Refs. 9–14 and the TEM image in Ref. 5 suggest that it is possible to induce a strained Si layer near the SiO_2/Si interface by thermal process. It should be noted that in the above Refs. 9–14, oxidation was carried out in furnace, where the slow cooling process may relax most of the stress, so that only limited strain in Si occurs. In RTP and LHP, rapid cooling may preserve most of the stress and more strain in Si may be induced.

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[1]C. Choi, C.-Y. Kang, S. J. Rhee, M. S. Akbar, S. A. Krishan, M. Zhang, H.-S. Kim, T. Lee, I. Ok, F. Zhu, and J. C. Lee, IEEE Electron Device Lett. **26**, 454 (2005).
[2]S. Monaghan, J. C. Greer, and S. D. Elliott, Phys. Rev. B **75**, 245304 (2007).
[3]Z. Chen, J. Guo, and F. Yang, Appl. Phys. Lett. **88**, 082905 (2006).
[4]Z. Chen and J. Guo, Solid-State Electron. **50**, 1004 (2006).
[5]Z. Chen, Appl. Phys. Lett. **91**, 223513 (2007).
[6]P. L. Ong, Z. Chen, A. Haggag, and T.-Y. Luo, Electrochem. Solid-State Lett. **11**, H293 (2008).
[7]Z. Chen, P.-L. Ong, and Y. C. Wang, J. Electrochem. Soc. **157**, G44 (2010).
[8]R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd ed., (Wiley, New York, 1986), pp. 384 and 401.
[9]K. Nakajima, M. Suzuki, K. Kimura, M. Yamamoto, A. Teramoto, T. Ohmi, and T. Hattori, Jpn. J. Appl. Phys. **45**, 2467 (2006).
[10]Y. P. Kim, S. K. Choi, H. K. Kim, and D. W. Moon, Appl. Phys. Lett. **71**, 3504 (1997).
[11]N. V. Nguyen, D. Chandler-Horowitz, P. M. Amirtharaj, and J. G. Pellegrino, Appl. Phys. Lett. **64**, 2686 (1994).
[12]W. Daum, H.-J. Krause, U. Reichel, and H. Ibach, Phys. Rev. Lett. **71**, 1234 (1993).
[13]Y. Sugita, S. Watanabe, N. Awaji, and S. Komiya, Appl. Surf. Sci. **100/101**, 268 (1996).
[14]S. Miyazaki, H. Nishimura, M. Fukuda, L. Ley, and J. Ristein, Appl. Surf. Sci. **113/114**, 585 (1997).