films. The shift of the C-V curve in P-glass films occurs at lower temperature (150°C) and is perhaps related to electron trapping by the hydrogenous species-phosphorus oxide complex. In undoped silicon dioxide the C-V curve starts to shift at 350°C, which is postulated to be due to vacancies at the sites of the hydrogenous species sites in the silicon-oxygen network. The activation energies of the process of loss of hydrogenous species and the generation of the hydrogen-vacancies-related oxide charges are found.

The measurements of I-V characteristics have shown an increase in the dielectric breakdown strength of the oxides on annealing at higher temperatures. Annealing is found to improve the oxide properties perhaps due to associated loss of the hydrogenous species which significantly lowers the current in the as-deposited oxides.

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Plasma-Enhanced Chemical Vapor Deposition of Silicon Dioxide Films Using Tetraethoxysilane and Oxygen: Characterization and Properties of Films

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ABSTRACT

SiO_2 films were deposited in a commercial single wafer parallel plate plasma deposition reactor using tetraethoxysilane as the silicon source. Deposition conditions were varied to produce films with widely differing properties. Electrical, optical, mechanical, and wet-etch-rate characterization were then used to investigate the as-deposited film quality. Moisture uptake was also measured and related to the initial properties. The films were studied in an ongoing investigation of silicon dioxide interlevel dielectric films used in multilevel ultra large scale integrated chip wiring.

The use of silicon dioxide as the interlevel dielectric in multilevel chip wiring technologies places many demands upon the film properties and processes used for its deposition. One of these is that the deposition temperature be low enough to prevent thermal voiding in aluminum-based conductors, but not so low that the dielectric properties of the films are adversely affected, as is often observed when low temperature, high deposition rate processes are used. The high deposition rate is necessary, since interlevel dielectrics are typically quite thick and most modern deposition systems are single wafer reactors. Dielectric layers a few micro-meters in thickness are not uncommon in bipolar chip wiring. Although the electrical properties of the films can be relaxed somewhat from those used in close proximity to the silicon device surface, a key parameter for the interlevel dielectric is its dielectric constant. The dielectric constant directly affects chip wiring delays and thus directly influences the performance of the finished chip. Other key properties of the dielectric are the electrical leakage and breakdown characteristics which are related to chip reliability issues, as well as the stability of the physical characteristics of the films. Finally, the dielectric must protect the metal wiring from environmental influences, such as moisture, which can be a factor in corrosion-induced failure of the chip.

In the studies reported here, we investigated SiO_2 films deposited in a single-wafer plasma reactor from mixtures of O_2 and TEOS (tetraethoxysilane). Deposition parameters were varied over wide ranges. Since temperature and deposition rate have been reported to have a significant effect on film properties, many of our experiments focused on these parameters. The dielectric constant and breakdown characteristics were determined using metal oxide semiconductor (MOS) capacitor measurements. Moisture (as -OH and H_2O) in the films was determined using infrared absorption spectrum analysis (FTIR) and the stability of the moisture content was determined by exposing the films to 100% relative humidity ambients either at room temperature or 62°C. The etch rates in buffered HF (BHF) and P-etch[1] were measured, as was the room temperature stress of the deposited films.

Experimental

The films were deposited by plasma-enhanced chemical vapor deposition (PECVD) in a commercial multiple-chamber system with a load lock. The deposition chamber

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had a parallel-plate configuration and 13.56 MHz rf power was applied to the driven electrode which was also the gas distribution head. The wafer rested on the grounded electrode spaced 0.48 cm below the rf driven electrode. This grounded electrode could be independently heated and its temperature was varied from 300-440°C. The actual wafer temperature during deposition depended upon heat transfer between the wafer holder and the back side of the wafer. It is estimated that the actual wafer temperature was within 5-10°C of the holder temperature. However, although we have used the terms wafer temperature or deposition temperature, the temperature is that of the wafer holder. The silicon source was TEOS liquid, and its vapor was transported to the reaction chamber using helium gas flowing through a bubbler.

Three sets of experiments were performed. The experimental conditions used for the first two sets were: chamber pressure: 9.0 Torr (kept constant by throttling the chamber exhaust line); rf power: 350 W (approximately 2.7 W/cm^2); O_2 flow rate: 325 sccm: TEOS/He (total flow out of the TEOS bubbler): 310 sccm; TEOS reservoir: 32°C. The temperature of the TEOS reservoir could be varied to change the TEOS flow rate, keeping the He carrier gas flow constant.

In the third set of experiments, a modified gas delivery system was used in which an independent helium line was employed to maintain a fixed total gas flow under different deposition conditions. The TEOS delivery could be varied by controlling the flow into the bubbler. The TEOS bubbler was equipped with a mass flow controller on the He inlet side and a mass flow monitor on the outlet side. The difference in flows measured across the bubbler was proportional to the TEOS vapor flow (calibration supplied by the equipment manufacturer). In this system, the TEOS reservoir was kept at 39.6°C and the carrier gas was varied to transport 12.6, 21.7, 29.5, and 36.6 sccm TEOS vapor in the majority of the depositions. Total helium flow was kept at 260 sccm by dilution with helium through the independent line. A series of runs was made at a TEOS flow rate of 46.8 sccm, with the TEOS reservoir heated to 43.3°C to achieve this delivery date. Deposition conditions were modified slightly from those used on the first two sets of experiments: chamber pressure 8.7 Torr; power 360 W; O_2 flow 231 sccm. However, there were no measurable differences in the fundamental properties of the SiO_2 films due to the small differences in chamber pressure and input power. The oxygen to TEOS flow ratios investigated were between 4.9 and 18.3.

Wafers were 125 mm in diam and were polished on both sides to facilitate the IR transmission spectroscopy. 10 to 20 Ω-cm p-type wafers were used most often, but some of the electrical characterization techniques required 1 to 2 Ω-cm n-type wafers. Wafers were cleaned with the peroxide "FET" cleaning solutions.[2] Immediately prior to deposition, some wafers were immersed in isopropyl alcohol, deionized water spray rinsed, and warm nitrogen spin dried. Reference made to a "standard" process in following sections of this paper corresponds to an oxygen to TEOS ratio of 6.3:1 and a deposition temperature of 390°C.

Electrical characterization was carried out using aluminum capacitors formed by evaporation through a metal mask. A large electrode (0.168 cm^2 in area) was used for dielectric constant measurements, while equal numbers (45 each) of large and 0.0746 cm^2 electrodes arrayed over most of the wafer surface were used in the breakdown field strength determinations to improve the statistics of the measurements, to obtain information on area effects, and to yield information of the film properties over most of the surface area of the wafer. The dielectric constant was computed using the average capacitance measured on 12 large capacitors near the wafer center. The largest source of error in these measurements was the oxide film thickness variation over the measured area. In samples with a large thickness gradient, the film thickness had to be measured at each individual capacitor to give reliable dielectric constant values. About 500 nm of aluminum was evaporated for the capacitors and a blanket deposition of 200 nm was used on the wafer back side to provide the back side electrical contact. Usually, an e-gun evaporation source was used, but for oxide charge determination, a resistance-heated source was substituted.

The capacitance measurement used for determination of the dielectric constant was made with a standard capacitance bridge at a bias voltage determined by measuring the C-V characteristics of the capacitor to ensure the silicon surface was in full accumulation. Measurements were carried out at 10 kHz, and were checked at 100 kHz and 1 MHz on a few wafers to determine that there were no unexpected frequency effects present. Breakdown characteristics were determined by stepping the applied voltage, so that the electrical field in the capacitor increased, at a rate of approximately 0.02 MV/cm-s. The voltage at which the first breakdown event occurred (evidenced typically by a current spike greater than 100 microamperes in the case of "self-healing" breakdowns) was used to calculate the breakdown field. Little information could be obtained from continuing to increase the applied voltage through multiple breakdown events until one happened to result in a shorted capacitor. In one instance a true voltage ramp (not stepped) resulting in a field ramp of 10^{-5} MV/cm-s, was used to evaluate the reliability of the oxide more thoroughly.

The index of refraction of the films was determined at the wafer center, using a prism coupler.[3] The infrared absorption analysis was carried out with an FTIR instrument on films 600 to 800 nm thick. Spectra were taken at 4 wave number resolution between 5000 and 400 cm^{-1} at the wafer center. The -OH and H_2O content of the oxides were measured by estimating the intensities of the 3650 and 3330 cm^{-1} bands and relating these to the corresponding concentrations according to the method given by Pliskin.[4] As with any quantitative IR absorption analysis, an estimation must be made of the transmittance in this spectral region in the absence of any impurity bands (the "base line"). This is complicated in the case of thin films on silicon substrates since film interference fringes exist in the spectrum which are of such a long period that they cannot be removed by lowering the resolution. Estimation of the base line was made by curve-fitting a cubic polynomial at both ends of the absorption bands. A visual estimation of the goodness of fit of this approach was made. Spectra which showed poor base line fit and spectra of a few randomly chosen samples were analyzed by subtracting spectra of samples of thermal oxide of the same thickness which did not contain the absorption bands due to OH or H_2O. In the case of the random samples with good base line fit, the concentrations were the same to within 0.2 weight percent (w/o).

To determine water pickup of the films, they were exposed either to 100% humidity at room temperature for seven days, or were kept in closed containers in an oven controlled at 62°C and examined periodically. Water reservoirs were placed inside the containers to keep the relative humidity at 100% and prevent contact between liquid water and the films.

The film stress at room temperature was calculated from the change in the radius of curvature of a single crystal silicon wafer with and without a film by measuring the lattice curvature using x-ray diffraction.[5] The uncertainty in the stress measurement is estimated to be about ±20 MPa.

Results and Discussion

Initial studies.—Deposition rate.—The deposition rate of the films used in these studies was in the range of about 600-1050 nm/min. The rate decreased monotonically with increasing wafer holder temperature and decreasing TEOS flow.[6] The decrease in deposition rate with increasing substrate temperature has been reported previously[7] and is characteristic of an adsorption controlled reaction. For the standard process, the rate was about 700 nm/min.

Film properties.—Dielectric constant.—The dielectric constant of films produced in the reactor was very consis-

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tent for the standard process. The average dielectric constant of the oxide deposited using this process, on a total of 69 test wafers over a period of several months, is 4.09 with a standard deviation of 0.05 (1.2%). The minimum value was 3.99 and the maximum 4.20, a spread of 5%, and the average remained at 4.1 in samples taken less frequently thereafter. 41 of the original 69 wafers were annealed at 400°C for 1 h in forming gas. After anneal the dielectric constant was 4.06 with a standard deviation of 0.03. This by itself was not a significant change in dielectric constant, but it was observed that all samples except one were slightly lower after the anneal. There was no significant difference due to wafer type or to sputter etching of the oxide after deposition. The dielectric constant was observed to decrease to a value of 3.80 after an hour anneal at 1000°C in N_2 in the few samples subjected to the high temperature anneal. It is clear, therefore, that the dielectric constant of the oxide films produced with the standard process is adequately reproducible for practical applications.

Stress.—The stress in the films at room temperature was compressive and increased monotonically with increasing rf power; the stress was increased 115% by a 30% increase in input power (130 MPa at 343 W, 280 MPa at 442 W). The deposition rate was unchanged in this power range. The increased stress may be the result of increased ion bombardment of the substrate, although the processes which occur have not been elucidated, as they have for bias sputtered SiO_2 and PECVD silicon nitride. In bias sputtered SiO_2, the higher compressive stress has been related to increased incorporation of Ar at higher substrate bias.[8,9] In PECVD nitride, Aite *et al.*[10] related the compressive stress to the expansion of the film due to ion implantation which increased as ionization in the plasma increased. Claasen[11] reported that the stress was a combined effect of the extent of ion bombardment and deposition temperature on the desorption rate of hydrogen, *i.e.*, on the H content of the film.

We found, however, that the stress in films deposited using the same conditions at different times in the same reactor or in different reactors of the same design, could differ by a factor of 2-3. Since the rf power influences the stress substantially, it was inferred that unknown variability in the rf coupling might be responsible. This could not be verified. Moisture absorption increases the compressive stress in SiO_2 films.[12] However, there was no correlation between the measured stress and the interval between deposition and measurement; we therefore concluded that uncontrolled moisture absorption/desorption was not responsible for the variability.

The stress was unchanged, within the experimental error, after annealing the films at 400°C for 30 min in forming gas.

Effects of process changes.—Temperature.—It has been shown that increasing the temperature improves the properties of deposited dielectric films.[13] Therefore a limited survey experiment was run to examine the effect of changing the wafer holder (deposition) temperature from 375 to 405°C, keeping all the other deposition parameters constant.

With increasing substrate temperature the refractive index of the film increased (from 1.4605 to 1.4617) and the dielectric constant decreased (from 4.19 to 4.09), the relative etch rate in BHF decreased 15%, and the porosity (determined by densification at 900°C) decreased (from 1.8 to 1.4%). The OH content (approximately 3 w/o) as well as the small propensity for moisture pickup (reflected in an increase in H_2O and/or OH-content) all decreased. Although the changes are small, they are a consistent set of results which show that increased deposition temperature increases the density of the film and improves its dielectric properties, at least as indicated by the dielectric constant. Water was not detected by IR spectroscopy in any of the as-deposited films. These results will be discussed in greater detail below.

Temperature, reactant flow rate, and storage.—An expanded range of deposition temperatures, 300 to 440°C, was then explored. It has been reported that PECVD is a method of preparing films with excellent electrical properties at low temperatures if the conditions are such that the deposition rates are exceptionally low. For example, Batey and Tierney[14] showed that the electrical properties of PECVD SiO_2 deposited using a mixture of SiH_4 and N_2O, were improved significantly when the deposition rate was decreased substantially, at constant temperature, by using very low flow rates of the reactant gases. Falcony *et al.*[15] report deposition of good quality films at low (200°C) temperatures (using silicon halides and O_2 or N_2O) but again, using very low flow rates of reactant gases so that the deposition rates were about 10 nm/min. It seems reasonable that increasing the temperature and lowering the rate will be beneficial; a precursor can more readily find an optimal surface site at which to react.

To examine the effect of deposition rate at constant temperature, the flow rate of TEOS was varied, by varying the temperature of the TEOS reservoir from 27 to 37°C, keeping the flow of O_2 constant. The range of TEOS flow rates used resulted in changes in deposition rate about the same as those due to substrate holder temperature changes.

The index of refraction of the wafers, deposited at different temperatures, was measured on the as-deposited wafers and the trends were the same as those in the initial survey experiment discussed above. However, the samples were then put aside for a period of months before the measurements were continued. Upon resumption of the measurements, the index of refraction determinations were repeated and they were found to decrease with increasing deposition temperature, a trend opposite to that observed initially. Samples deposited at the lowest temperatures showed a substantial increase in refractive index whereas the increase in the samples deposited at high temperatures was either very small or was not detectable. The dielectric constants of the samples deposited at the lowest temperature approached 5.0. Samples deposited at low flow/deposition rates (lower TEOS reservoir temperature) had lower values of the dielectric constant than those deposited using high flows. The films were then annealed at 400°C for 30 min in forming gas and remeasured. The refractive index of all the samples reverted essentially to the original values and the dielectric constants were reduced substantially. The effect of annealing was most dramatic in the case if the samples deposited at the lowest temperatures.

Companion PECVD and thermally-grown SiO_2 films were etched simultaneously in P-etch. The ratio of the etch rate of the PECVD oxide to that of thermally grown SiO_2 (ERR), before and after anneal were measured. There was only a small decrease in ERR after annealing, but it was larger for the samples deposited at the lower temperatures. After annealing, the ERR decreased from about 5.5 for the sample deposited at 300°C to less than 3 for that deposited at 440°C. We also noted that reducing the deposition rate, whether achieved by raising the temperature or decreasing the TEOS supply, decreases ERR.

Rutherford backscattering spectroscopy (RBS) indicated that the silicon to oxygen ratio was very close to 1:2. There were slight variations among the samples but no discernable trends with temperature or deposition rate.

Preliminary measurements of the relative H-content were made using the resonant nuclear reaction (NRA) ^1H + ^{15}H.[16] The H-content of the films was increased when the deposition rate was increased whether this was accomplished by decreasing the deposition temperature or increasing the reactant supply; annealing reduced the H-content; the magnitude of the change was smaller for samples deposited at the lower rates.

The compressive film stress, measured at room temperature, increased from about 20 MPa to about 105 MPa as the temperature during deposition was increased from 300 to 440°C. If the higher compressive stress is due to the larger temperature excursion between the deposition and measurement temperatures, the effect of the thermal mismatch

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between SiO_2 and the silicon substrate can be estimated. Using the elastic constants and a constant value of the thermal expansion coefficient of thermal SiO_2, about 1/5 of that of silicon,[17] the estimated increase is about half of that measured. The approximation equating the PECVD oxide constants with those of thermal SiO_2 probably would not account for this difference. Since the stresses are relatively low, a disagreement of a factor of 2 may not be significant. However, the results may also be interpreted as a difference in the intrinsic stress in films deposited at different temperatures; a higher compressive stress for the film deposited at the higher temperature (a somewhat denser film) is not unreasonable. Films deposited at lower temperatures have a higher H-content and absorb moisture more readily (as discussed in detail below); as mentioned above, absorption of moisture by PECVD SiO_2 films produces an increase in compressive stress.[12] However, the films deposited at the lower temperature were less compressive. Another alternative which may explain the observed trend, but cannot be verified, is that the more open (porous) structure of films deposited at the lower temperatures/higher rates relax more readily. This may be consistent with the effect of power on stress.

Exposure to atmospheric moisture.—Atmospheric water absorption was suspected to be the cause of the changes during storage. The reversal upon annealing at 400°C for 30 min in forming gas, which neither densifies the film nor eliminates Si-OH, lends weight to this conjecture. Therefore, it was decided to expand the investigation to include not only the wafer holder temperature, but also a wider range of O_2:TEOS ratios (R) to produce films of widely varying properties, and purposely expose them to a warm, high humidity ambient. Although the dielectric constant of unmetallized wafers increased during storage, wafers on which the (large) electrodes had been deposited were unchanged after a year of exposure to the laboratory environment.

Deposition temperature and O_2:TEOS flow ratio (R) experiments.—These experiments were performed in the modified reactor. Although the results are reported in terms of R, the O_2 flow rate was held constant at 231 sccm and only the TEOS flow rate varied, maintaining a constant flow rate of He. Therefore, a higher value of R is equivalent to a lower TEOS flow rate. The effect of changing R by changing the O_2 flow rate as well has not yet been thoroughly investigated, although preliminary studies indicate that R is a legitimate parameter. Film thicknesses were nominally 650 nm, although some 120 nm samples were evaluated as well. For the as-deposited films, the deposition rates (Fig. 1), index of refraction (Fig. 2), and dielectric constants (Fig. 3), as a function of temperature and R, agree with the earlier trends. In Fig. 4 the dependence of the index of refraction on deposition rate is shown for several substrate temperatures. Figure 5 shows the dependence of the dielectric constant of all the samples on deposition rate.

The samples deposited at 300°C show a sharp increase in dielectric constant at low R values. We will return to the interpretation of this behavior after the IR spectra are discussed. Films deposited at lower temperatures have lower indexes than those deposited at high temperatures. In addition, there is a considerable dependence upon R.

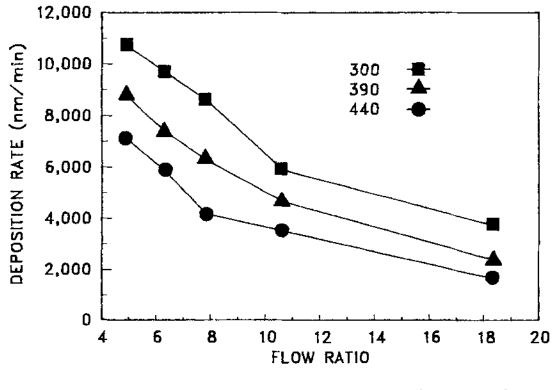

Fig. 1. Deposition rate *vs.* R for 300, 390, and 440°C deposition temperatures.

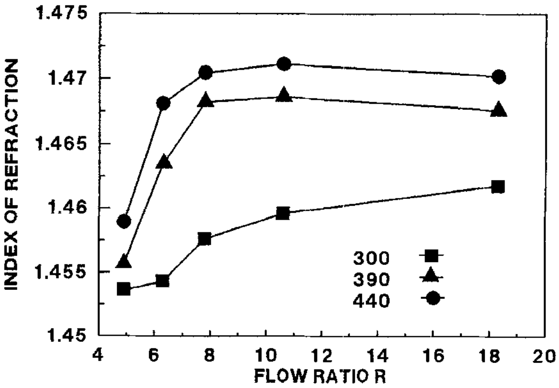

Fig. 2. Refractive index *vs.* R for 300, 390, and 440°C deposition temperatures.

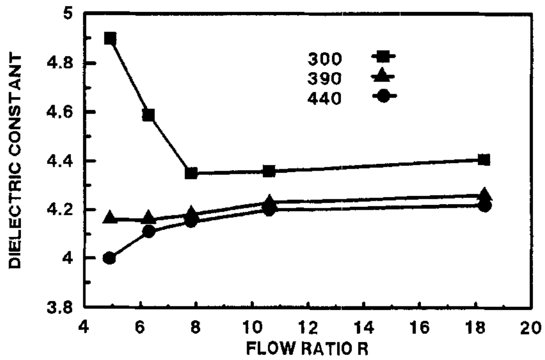

Fig. 3. Dielectric constant *vs.* R for 300, 390, and 400°C deposition temperatures.

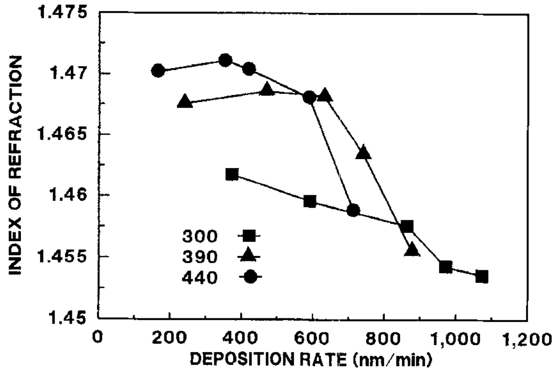

Fig. 4. Refractive index *vs.* deposition rate.

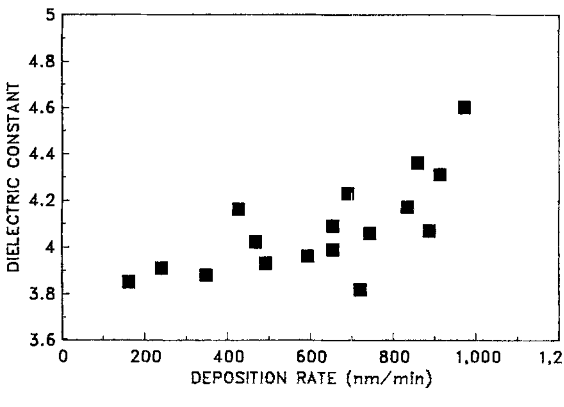

Fig. 5. Dielectric constant *vs.* deposition rate.

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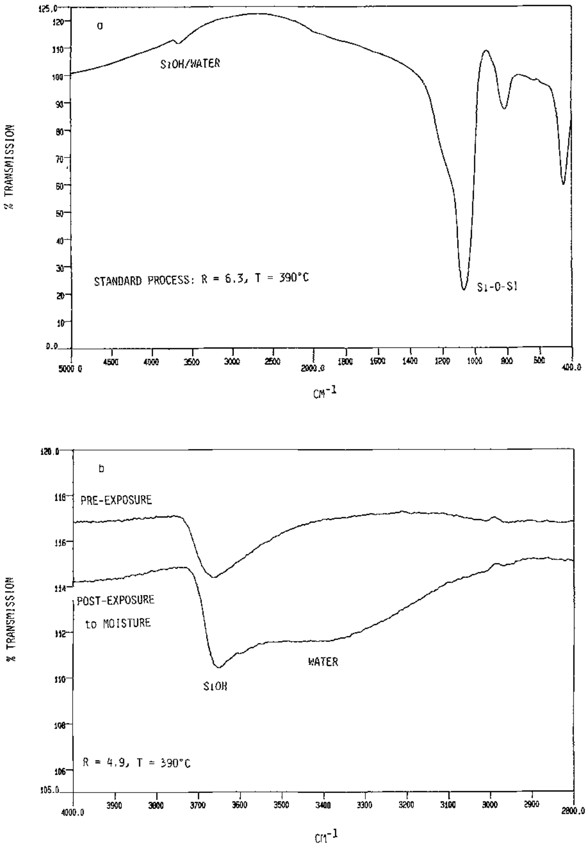

Fig. 6. a) IR absorption spectrum over full range recorded in these studies. b) IR absorption spectrum; expanded scale of spectrum in water region.

In the as-deposited films, water was detected only in those prepared at the lowest temperature (300°C) at the lower *R* values. Although all attempts were made to avoid exposure of the samples to the atmosphere after deposition by storing them in dry N_2, some exposure, though it may have been brief, was inevitable. It can be seen in the results of the water-uptake experiments (discussed below), that the initial water-uptake in these films was very rapid. It is consistent with our observations to conclude that the as-deposited films are water-free.

A typical IR spectrum is shown in Fig. 6a covering the 5000 to 400 cm^{-1} range. The -OH band at 3650 cm^{-1} and H_2O band at 3330 cm^{-1} are shown in more detail in Fig. 6b. Analysis of the -OH and H_2O absorption bands in the as-deposited samples is summarized in Fig. 7. The OH concentration increases as the deposition temperature is decreased and there is also an appreciable rise for flow ratios less than about 8. The increase in H_2O content is plotted for the 300°C samples only since H_2O was not detected in samples deposited at higher temperatures.

The uptake of water was determined by exposing the samples to 100% relative humidity at 62°C. The behavior of oxides deposited at the three deposition temperatures used was distinctly different. Figure 8a shows that the increase in OH-content was relatively small in the samples deposited at 300°C, but the H_2O increase was considerably greater (Fig. 8b). In Fig. 8c it can be seen that the total H-content, computed from the values obtained in the IR analysis, increased in all the oxides deposited at 300°C. The films deposited at high *R* values exhibited a smaller increase than those deposited at low values. The shape of the curves tended to be similar: an initial rapid rise was followed by a more gradual, diffusion-limited increase. As seen in Fig. 9a, the increase in OH for the oxides deposited at 390°C was confined to the low *R*-value samples, as was the H_2O increase shown in Fig. 9b. The total increase in H was therefore confined to the low *R*-value samples (Fig. 9c). Thus, samples prepared with the standard process (390°C, *R* = 6.3) also eventually picked up water. The only increase in H in the 440° samples was seen in the one deposited at *R* = 49:1; this was due to a small increase in both OH and H_2O (Fig. 10). As noted in the preceding section, the water pickup was completely reversible, since a 400°C anneal could be used to return the films to the original levels (or lower). Furthermore, samples left at 62°C in a low humidity ambient lost water (although not OH).

The main Si-O stretching vibration in the vicinity of 1080 wave numbers decreased slightly in full width at half maximum (FWHM) as the OH content rose with water absorption, and the band maximum also shifted to slightly higher wave numbers. This is consistent with the increase in OH content with water absorption and has been interpreted to indicate some strained Si-O bonds are destroyed by the incorporation of OH groups.[18]

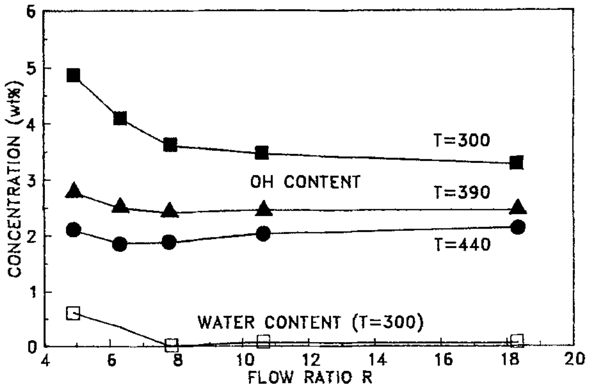

Fig. 7. OH and H_2O concentrations in as-deposited films vs. *R* for several deposition temperatures. Water content in films deposited at 390 and 440°C was zero for all values of *R*.

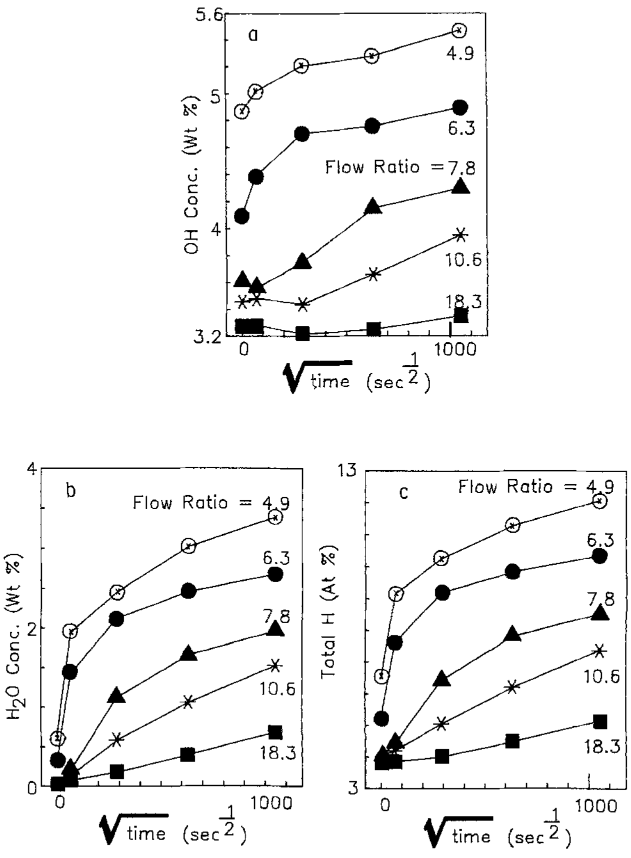

Fig. 8. a) OH concentration in films deposited at 300°C upon exposure at 62°C, 100% R.H. air vs. time for several values of *R*. b) H_2O concentration of films of Fig. 8 a vs. time for several values of *R*. c) H content of films vs. time for several values of *R*. Values derived from Fig. 8a and b.

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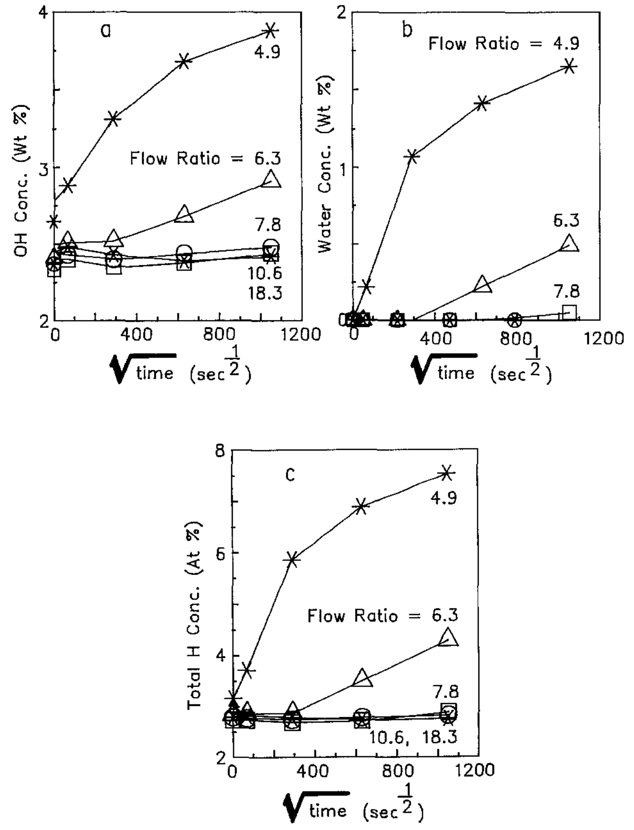

Fig. 9. a) OH concentration in films deposited at 390°C upon exposure at 62°C, 100% R.H. air *vs.* time for several values of *R*. b) H_2O concentration of films of Fig. 9a *vs.* time for several values of *R*. c) H content of films *vs.* time for several values of *R*. Values derived from Fig. 9a and b.

Some other features of interest observed in the spectra of the as-deposited oxides are illustrated in Fig. 11. At high R values, a narrow band (approximately 9 cm^{-1} FWHM) at 2340 cm^{-1}, was observed, which indicates that CO_2 was incorporated in these films.[19] While this band was largest for films deposited at 300°C, it was detectable at all temperatures. Within experimental error, there was no change in the CO_2 band after long-term atmospheric exposure. It seems likely, therefore, that incorporation of CO_2 occurs during deposition. Since the CO_2 concentration is highest in the film deposited at the highest R values, one may speculate that its presence is associated with extensive oxidation of organic by-products. In the spectra of films deposited using low R values, a weak, fairly broad peak near 2260 cm^{-1} could be seen, as well as another band at 890 cm^{-1}. These bands suggest a degree of oxygen deficiency in the films, since they are associated with Si-H and non-bridging oxygen, respectively.[20]

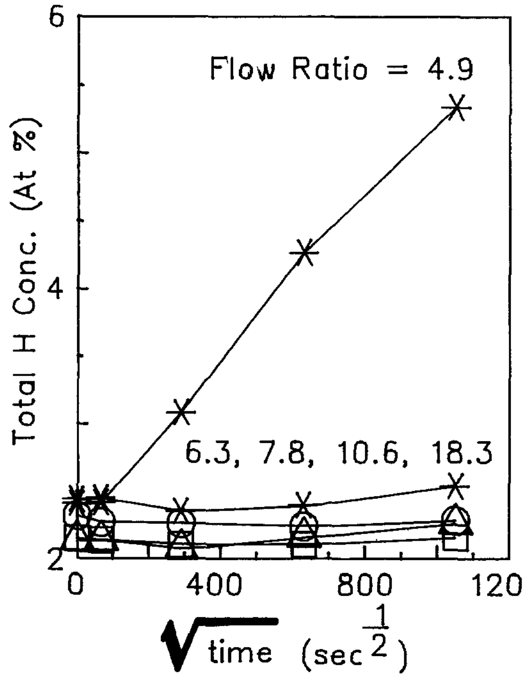

Fig. 10. H content of films deposited at 440°C upon exposure at 62°C, 100% R.H. *vs.* time for several values of *R*.

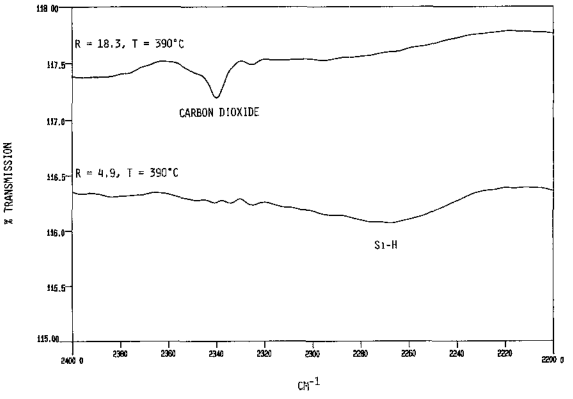

Fig. 11. IR absorption spectrum of a film deposited at 390°C between 2200 and 2400 wave numbers.

Correlations between properties.—A definite correlation exists between the dielectric constant and the total H, as is seen in Fig. 12. A linear relationship fits the data quite well (the square of the correlation coefficient is 0.91). The magnitude of the constant term in the regression (3.73) is surprisingly close to the dielectric constant observed after 1000°C nitrogen anneal. When the OH-content is high, its presence dominates the dielectric constant. When it is low, however, the scatter of the data suggests that other factors such as structure and other impurities may be significant in determining the value of the dielectric constant.

Dielectric breakdown.—General characteristics.—The dielectric breakdown field strength was studied, initially, for films deposited using the standard process. In the figures which illustrate the breakdown characteristics of the films, the cumulative percent failed is plotted as a function of the applied field, E (MV/cm), at which the first event occurred. Table I identifies and describes all of the samples for which breakdown distribution curves are shown and lists the values of the maximum breakdown field, E_{max}, the average breakdown field, E_{av}, and the standard deviation.

A breakdown distribution is often seen to consist of two regions: a high-field and a low-field one. Often there is no sharp distinction between the regions. An abrupt change in slope of the breakdown distribution may be taken as the dividing line, but it is often a subjective judgment. In Fig. 13a, the low-field region is very sparsely populated. In Fig. 13b and c, and in curve No. 10 of Fig. 13d, the regimes

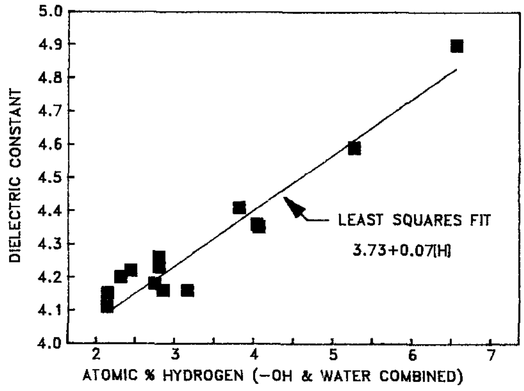

Fig. 12. Dielectric constant *vs.* total H content.

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Table I. Break-down statistics.

Figure #	Curve #	Description	Electrode area (cm^2)	E_{max}	E_{av}	Std. dev.
13	1	A	0.168	9.65	9.30	0.22
13	2	A	0.075	9.42	8.88	0.21
13	3	A	0.168	9.71	9.16	0.18
13	4	A	0.075	9.78	8.82	0.39
13	5	A	0.168	7.94	7.30	0.35
13	6	A	0.168	7.99	7.17	0.75
13	7	A	0.168	7.64	6.47	1.43
13	8	A	0.168	10.41	9.76	0.35
13	9	A	0.168	9.97	8.83	0.98
13	10	A	0.168	7.61	6.85	0.88
13	11	A	0.168	7.24	5.46	1.54
14	12	300°C[B]	0.168	9.62	7.79	1.15
14	13	330°C[B]	0.168	9.14	7.49	1.51
14	14	360°C[B]	0.168	8.39	7.73	0.48
14	15	390°C[B]	0.168	7.94	7.30	0.35
14	16	415°C[B]	0.168	7.35	6.86	0.33
14	17	440°C[B]	0.168	7.86	6.76	0.43
15	18	2540Å[C]	0.168	7.21	6.03	1.34
15	19	3990Å[C]	0.168	7.39	6.69	0.51
15	20	7900Å[C]	0.168	8.27	7.49	0.39
15	21	2010Å[C]	0.168	10.08	8.59	1.20
15	22	4020Å[C]	0.168	10.31	9.76	0.54
15	23	5850Å[C]	0.168	10.33	9.80	0.33
15	24	8215Å[C]	0.168	10.43	9.93	0.46
16	25	P-Si[D]	0.168	6.17	5.86	0.22
16	26	P-Si[D]	0.074	6.28	5.99	0.17
16	27	AlCu[D]	0.168	6.29	5.65	0.74
16	28	AlCu[D]	0.074	6.36	5.84	0.58
17	29	P-Si[B]	0.168	10.31	9.51	0.76
17	30	N-Si[B]	0.168	9.31	7.67	0.95
18	31	1 V/s[E]	0.018			
18	32	0.02 V/s[E]	0.018			
18	33	0.0004 V/s[E]	0.018			

[A] Standard deposition parameters film thickness 6000Å.
[B] Except for temperature, same as A.
[C] Standard deposition parameters.
[D] Standard deposition parameters film thickness 2800 Å.
[E] Standard deposition parameters 4 wafers combined.

are reasonably clear. Sometimes the distribution curve extends smoothly from the high-field to low-field regions, as seen in curve #11 in Fig. 13d. The processes involved in the breakdown in the two regions are the same, but breakdown occurs at different rates.[21] The low-field breakdowns are emphasized at low ramp rates of the applied voltage. Therefore, the results will differ at different ramp rates. They will also depend on the electrode area, but the differences may not be obvious if the distributions are very tight. Therefore, unless all measurements are made using the same test conditions, comparisons between different materials/processes may be difficult.

We hesitate to characterize the breakdown process. The high-field breakdowns have been called intrinsic, implying that the mechanism is understood, and this does not seem to be so. The low-field or rapid-rate breakdowns have been called "defect related;" they may be due to impurities or inclusions, or in the view of Av-ron and Shatzkes[22] regions of positive charge.

PECVD SiO_2 films deposited in rapid sequence usually had very similar breakdown characteristics; however, in general, the characteristics of the films prepared in this study were much more variable than the dielectric constant. Some of the PECVD oxides deposited in these reactors have exceptionally high values of E_{max} (>9 MV/cm) with a very tight distribution of events (Fig. 13a). If the low-field region is a measure of defects, this indicates a very low defect level as well as a very high ultimate strength. However, films of approximately the same thickness, deposited under presumably identical conditions, on substrates that were prepared in the same way, were often quite different, as previously mentioned and illustrated in Fig. 13 a-d. The variability of the results obtained for what we considered to be identical oxides indicates that there may be process differences that have gone undetected. Since plasma deposition is an extraordinarily complex process, involving impact ionization of the feed gases (so that both gas and electron distributions are important), free radical and metastable molecule formation, species transport, surface and gas phase reactions, etc., variability may not be altogether surprising.

Wafer preparation may be exceedingly important and may not have been controlled adequately. It has been reported that, for a material formed in a much simpler kinetic system, *i.e.*, thermally-grown SiO_2, the breakdown behavior depends on surface preparation, cleanliness of the reactor, electrode preparation, etc.[23]

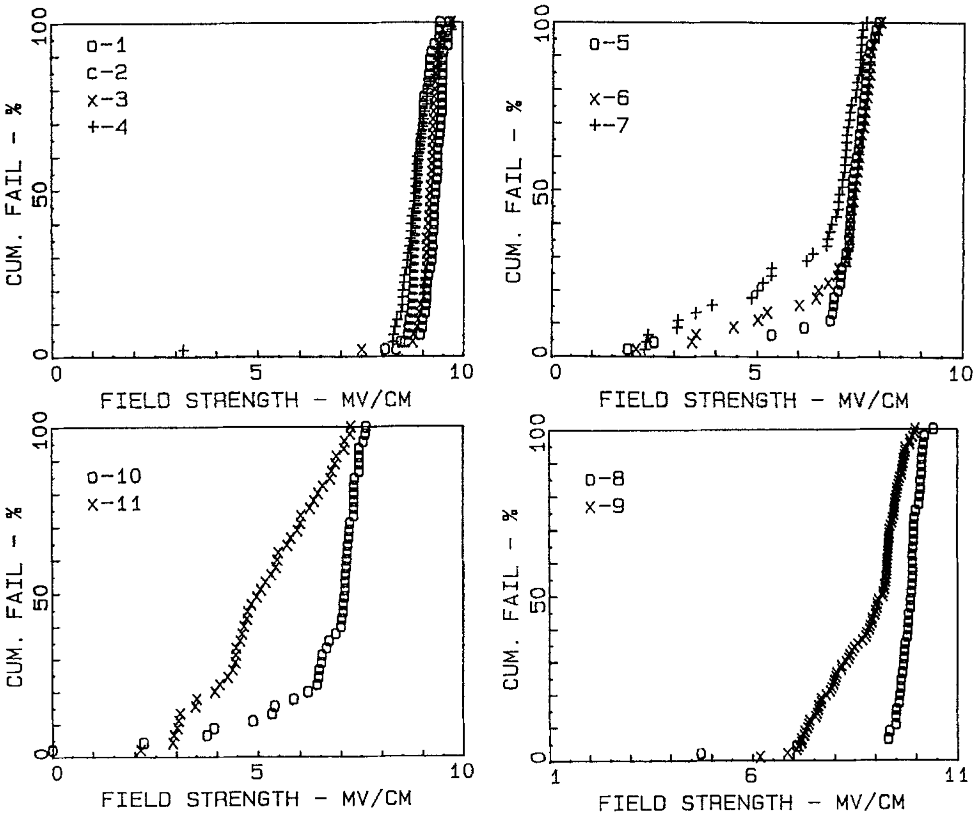

Fig. 13. Variable breakdown behavior of MOS capacitors (see Table I).

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As previous results on other oxides imply, and as we confirm here, it may be very difficult, and possibly meaningless, to specify a characteristic dielectric strength, even for a given material prepared in a given reactor according to a given recipe, although such a value is often referred to in the literature. E_{max} which is often reported as a measure of the quality of the insulator, is of little import in evaluating the usefulness or reliability of an insulator. It is the low-field breakdowns (uncovered using large electrodes, slow ramp rates and the first event criterion), that are the ones most important in evaluating the reliability of the insulator at use conditions.

Although we have cast doubt on the reproducibility and absolute value of the results of dielectric breakdown measurements, we feel that it is valid to report some trends we have observed in series of films, deposited in rapid succession, as we intentionally varied some of the deposition conditions or substrates, after annealing the films, and by varying the applied voltage ramp rate used in the measurements. We have attempted to explain the observations or correlate them to other results in the literature. However, at times we were unable to do so and preferred to avoid mere speculation.

Substrate temperature.—The effect of deposition temperature on the break-down characteristics is shown in Fig. 14. E_{max} increases monotonically with decreasing substrate temperature; but the low-field breakdown is degraded slightly at the lower temperatures. Since increasing the substrate temperature results in a denser film, one might expect that the dielectric break-down strength would be enhanced. It is possible that breakdown strength is sensitive to small decreases in the H-content produced by the temperature increase, due to the interaction between OH groups and strained Si-O bonds, and this has the more dominant role. An analogous result has been reported for films of PECVD SiO_2 deposited from SiH_4/N_2O [24] in a multiple-station system. The destructive breakdown voltage increased as the deposition rate was increased; at the higher deposition rates more H was incorporated into the films.

An interesting experiment which has not been performed but which might elucidate the role of H, is the comparison of films prepared sequentially under the same conditions but exposed to moisture for different periods to vary the OH-content. Another is the comparison of films deposited at different substrate temperatures, but exposed to moisture so that the OH-content is the same in both films.

Deposition rate (TEOS flow rate).—The results of only a single experiment were not as clear-cut as the ones in which the substrate temperature was changed. But the trend appears to be that the breakdown distribution is shifted to higher field strengths as the rate is increased. This agrees with the results reported above for the SiH_4-based SiO_2 [24] and with those obtained by changing the substrate temperature.

Power.—Increasing the rf power shifted the breakdown distribution to higher field strengths.

Film thickness.—The film thickness was varied by changing the deposition time at constant deposition conditions. We often observed that the breakdown curve for the thinner films was shifted to lower field values (lower E_{max}) and that the distribution became broader with more numerous low-field breakdowns (Fig. 15a). At other times the differences among them were less pronounced although the breakdown distribution for the thinnest film was significantly broader (Fig. 15b). For these film thicknesses (250-800 nm) we cannot explain the high-field shifts when they occur. For very thin thermally-grown SiO_2, when the low-field breakdowns were studied they were reported to increase, decrease, or remain constant as the thickness increased.[23] The high-field breakdown was unaffected.

Substrate.—When relatively thin (280 nm) films were deposited, in sequence, on silicon and blanket sputtered Al-0.5% Cu substrates about 500 nm thick, (Fig. 16), the high-field behavior was essentially identical; the low field breakdowns probably reflected the difference in the surfaces of the two substrates.

In one experiment, 200 nm of oxide was deposited on an Al-0.5% Cu grid (200 nm thick) which covered the entire wafer and the electrodes were evaporated as usual. The

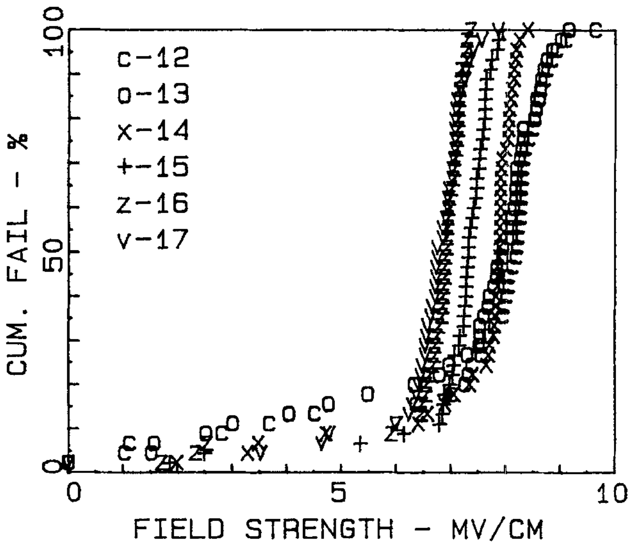

Fig. 14. Capacitor breakdown statistics for films deposited at different temperatures, *i.e.*, with different H content (see Table I).

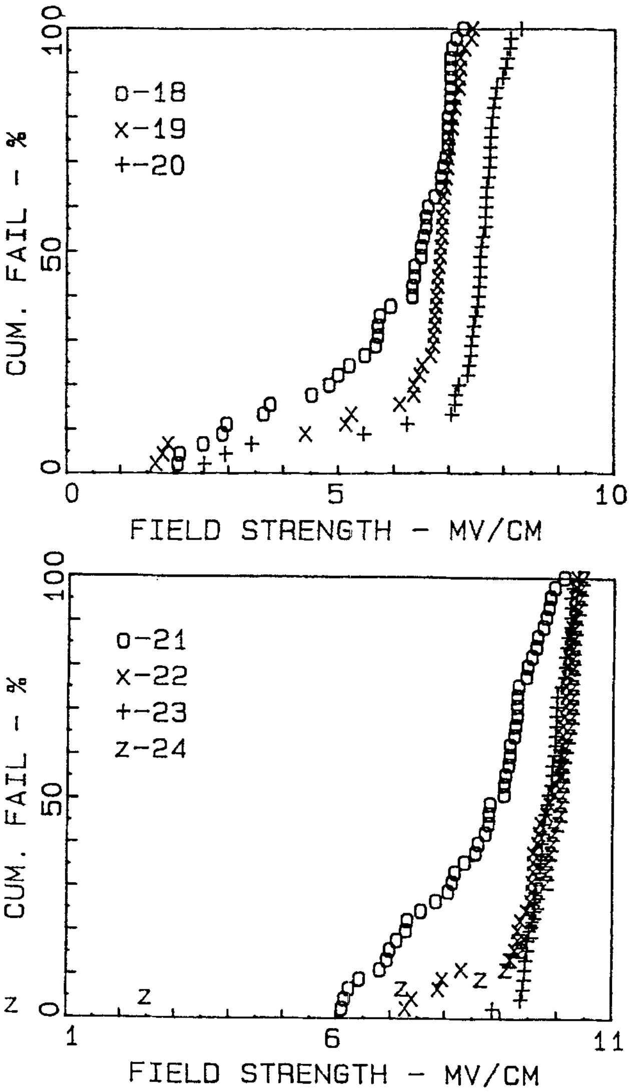

Fig. 15. Influence of film thickness on breakdown (see Table I).

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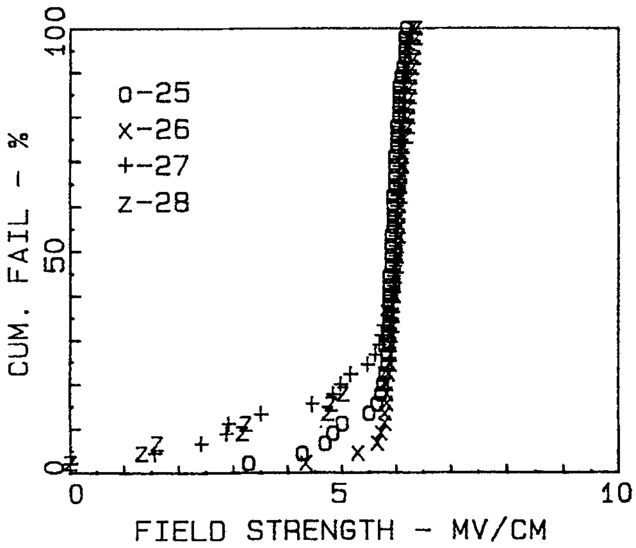

Fig. 16. Capacitor breakdown statistics for films deposited on bare silicon and on AlCu coated wafers (see Table I).

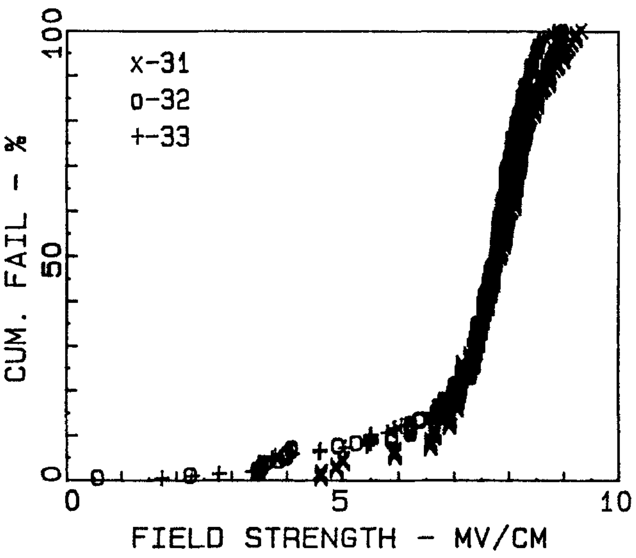

Fig. 18. Effect of test voltage ramp rates on breakdown statistics (see Table I).

breakdown characteristics of the oxide on this structure were somewhat degraded when compared to an oxide of the same thickness, deposited sequentially on a bare silicon wafer surface. We attributed the differences to the fact that the thickness of the oxide at the edges of the grid pattern was less than nominal. In addition, field concentration at the edges of the structure may enhance the tendency to break down.

As illustrated in Fig. 17, the breakdown curve of oxides deposited on n-type silicon was always shifted to lower fields than those deposited on p-type silicon; the electrodes were biased using the proper polarity for each type. This asymmetry has not been observed for thermally-grown SiO_2, and similar experiments have not been reported, to our knowledge, for PECVD oxide films deposited using TEOS or other sources.

Annealing.—Annealing the oxide films at 400°C for 30 min in forming gas minutes reproducibly shifted the entire distributions slightly to a lower field with no increase in the number of low-field breakdowns. The latter is not surprising, since no interaction between Al and SiO_2 is expected at 400°C after 1 h. However, an interaction, leading to shorts, was reported by Chou and Eldridge[25] after annealing at 500°C for 1 h.

Applied voltage ramp rate.—Figure 18 illustrates the effect of changing the applied voltage ramp rate in the measurement. In this study, measurements made on four wafers were combined; the electrode area was $0.018\ \text{cm}^2$. The high field regions are almost unchanged as the rate is reduced, but, as expected, the number of low-field breakdowns increased at the lower rates. This figure shows that the reproducibility, performance and reliability of these oxides are very good.

Oxide charge, I-V curve.—The charge in a typical oxide deposited in this system was $1.75 \times 10^{11}\ \text{cm}^{-2}$ This is considered to be an acceptable charge level for an interlevel dielectric. Figure 19 shows a typical I-V curve obtained using an as-deposited film about 600 nm thick. The high current at low field indicates the presence of positive charge. As the field is increased, the charge is eradicated. When the field is then decreased, two limiting curves, ob-

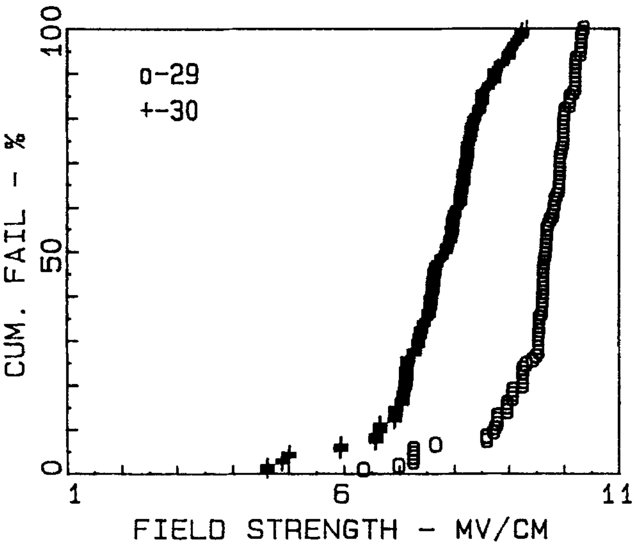

Fig. 17. Capacitor breakdown statistics for films deposited on n-type and p-type silicon (see Table I).

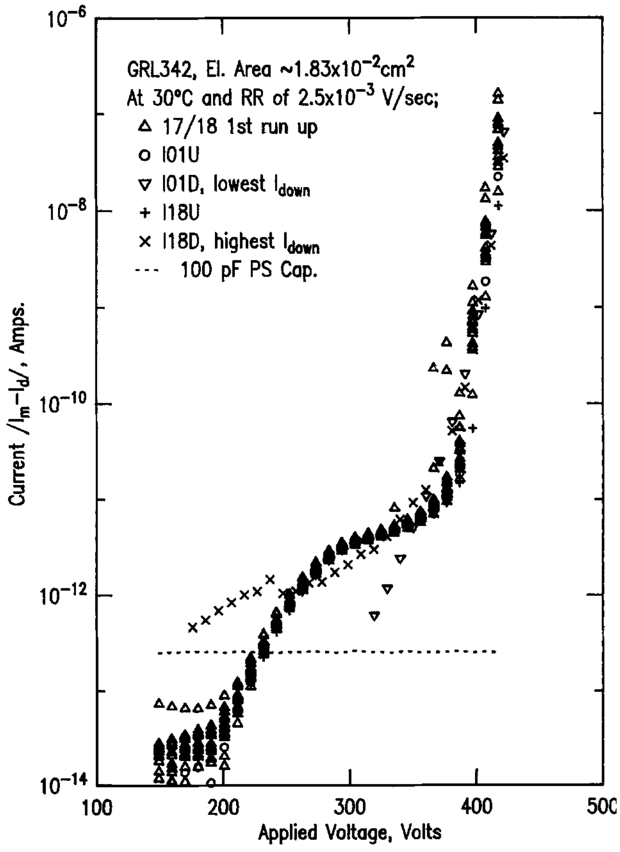

Fig. 19. I-V characteristics of MOS capacitors.

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tained for different electrodes, are shown. The one on the right indicates that the charge remained eradicated; the one on the left showed that the positive charge was enhanced.

Conclusions

TEOS-based PECVD SiO_2 films deposited under various operating conditions can pick up water in appreciable amounts. The presence of OH and H_2O results in an increase in the dielectric constant. However, films deposited using the standard conditions have relatively small amounts of OH and no detectable H_2O in the as-deposited state and show only slight tendency to pick up moisture during exposure to warm, high humidity ambients. Both the tendency to pick up water during exposure to the atmosphere and the dielectric constant of the as-deposited films are reduced if the films are deposited at higher temperatures. However, the increased occurrence of stress voids in Al-based conductors as the deposition temperature of the overlying insulator is raised limits the practical upper temperature. Even in oxides produced using the same, standard conditions, there is a variability in breakdown behavior. Despite these observations, these oxide films deposited at a high rate in a plasma reactor can be expected to perform well as interlevel dielectrics, once the proper deposition conditions are determined.

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Formation of Contacts in a Planarized $SiO_2/Si_3N_4/SiO_2$ Dielectric Structure

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ABSTRACT

The formation of vertical contact openings through planarized dielectric layers requires either very high etch selectivity between SiO_2 and silicon substrates or modification of the dielectric film structure to offset the need for extreme etch selectivity. A four-step process has been developed in an Applied Materials 8110 system to etch submicron contacts through a planarized $SiO_2/Si_3N_4/SiO_2$ layer in which the intermediate Si_3N_4 film acts as a buffer during the initial SiO_2 etching to compensate for the difference in SiO_2 thickness over planarized source/drain and polycrystalline silicon contact areas.

To achieve the maximum performance for integrated circuits with submicron devices and to minimize the area of such chips, the interconnecting metallization for these circuits must utilize small pitches and small overlap areas between levels. For example, as noted elsewhere,[1] whereas only 5-10% of the area of a static random access memory (SRAM) cell is active device area, as much as 40% of this cell area may be required for the interconnection of these devices. In general, the requirements for device interconnection compromise the increase in performance which may be achieved with smaller devices and higher feature density.[2]

Although processing limitations in photolithography and device isolation also contribute to these extra area requirements, progress has been made in both of these technologies. Hence, less area is needed to offset layer-to-layer

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