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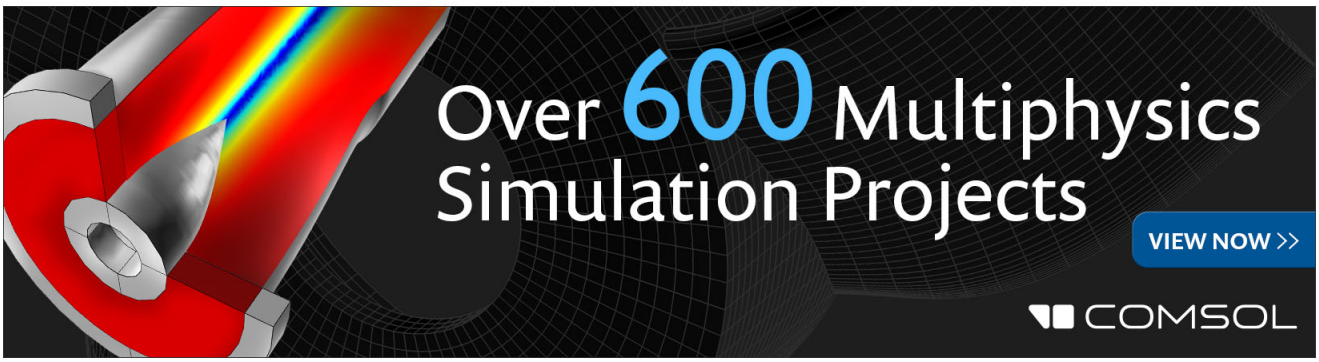

Compatibility of polycrystalline silicon gate deposition with HfO_2 and Al_2O_3/HfO_2 gate dielectrics

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Polycrystalline-silicon (poly-Si) gate compatibility issues with HfO_2 and Al_2O_3 capped HfO_2 gate dielectrics are reported. It can be generally stated that chemical vapor deposition (CVD) silicon gates using silane deposited directly onto HfO_2 results in electrical properties much worse compared to similar HfO_2 films using platinum metal gates. However, depositing CVD silicon gates directly onto Al_2O_3 capped HfO_2 showed greater than a 10^4 times reduction in gate leakage compared to the poly-Si/HfO_2 and poly-Si/SiO_2 controls of similar electrical thickness. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1499514]

Metal–oxide–semiconductor field-effect transistor devices have been aggressively scaled in order to improve performance, but the continuing push to decrease device feature size is limited by some of the physical properties of the current materials. Current technology forecasts show that deep submicron device scaling will soon require SiO_2 gate dielectrics be scaled to much less than 2 nm. It is generally accepted that such scaling will lead to increased tunneling currents from these very thin SiO_2 gate dielectrics resulting in an unacceptable power consumption and decreased reliability. One alternative is to replace SiO_2 with a material having a higher dielectric constant that will allow the use of a thicker, and therefore less leaky, gate dielectric. Towards this end, HfO_2 has been evaluated to replace SiO_2 as a gate dielectric due to its observed physical stability and calculated thermodynamic stability against silicon, and because it has a relatively high dielectric constant (~ 23)[1] and band gap (~ 5.8 eV).[2] However, we report herein physical and electrical results using metal–oxide–semiconductor capacitors (MOSCAPs) indicating an incompatibility of HfO_2 with a conventional polycrystalline silicon (poly-Si) gate process. Notably, chemical vapor deposition (CVD) poly-Si gate with a ZrO_2 gate dielectric has already been reported to show gross incompatibilities.[3,4] Although data on devices using HfO_2 gate-dielectric and silicon gates have been reported, the CVD silicon gates used are often deposited at low temperatures ($<\sim 580\,^{\circ}C$) resulting in amorphous silicon which can lead to unacceptable dopant depletion effects.[3] To circumvent the observed adverse results with the conventional poly-Si/HfO_2 gate stack, investigations of capping the HfO_2 with thin layers of atomic layer deposition (ALD)–Al_2O_3 before the poly-Si deposition were examined.

The HfO_2 gate dielectric was deposited on the silicon substrates by metalorganic chemical vapor deposition (MOCVD)[5] using hafnium-tertiary-butoxide precursor at 550 °C. Thin Al_2O_3 capping layers were deposited at 300 °C on top of some of the HfO_2 films using ALD[6] with trimethylaluminum (TMA) precursor. Low pressure chemical vapor deposition (LPCVD) silicon gates were deposited using silane (SiH_4) at 620 or 540 °C. The 620 °C LPCVD silicon process is conventionally used for poly-Si gated devices with SiO_2 dielectrics. The 540 °C LPCVD silicon process results in amorphous silicon films as-deposited which become polycrystalline during the subsequent processing anneals. The silicon gates were implanted with the appropriate dopants, MOSCAPs were then fabricated using sidewall spacers, Co–silicide, and forming gas anneal.

Transmission electron microscopy (TEM) studies of the interface between the poly-Si gate and HfO_2 gate dielectric indicate no evidence of gross interfacial reaction even after dopant activation anneals of 1025 °C. However, when depositing the poly-Si on top of HfO_2 at conventional temperatures of 620 °C, a low density of very large polysilicon grains is observed. The dark field optical microscope displays these inhomogeneous grains as a bright spots or "starlight" [Fig. 1(a)]. Cross-sectional TEM [Fig. 1(b)] indicates an accelerated grain growth of poly-Si and the nucleation of these features occurs at or very near the HfO_2 surface.

The $I-V$ electrical results for 620 °C poly-Si/HfO_2 MOSCAPs show very high leakage compared to similar electrical thickness HfO_2 films using platinum metal gates or similar electrical thickness poly-Si/SiO_2 controls. Use of

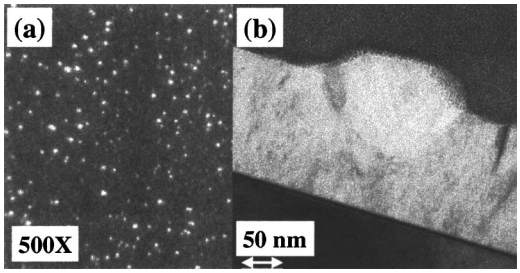

FIG. 1. (a) Dark-field optical image (500×) showing observed poly-Si starlight inhomogeneous grain growth. (b) Cross-sectional (XTEM) of a poly-Si starlight grain.

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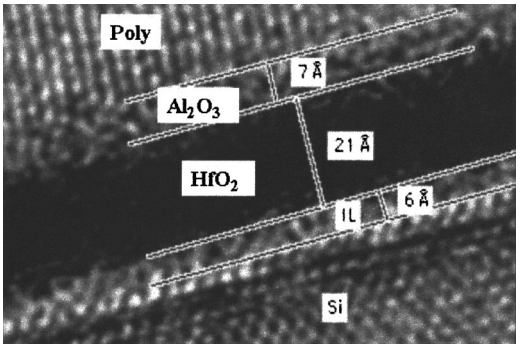

FIG. 2. XTEM of the poly-Si/Al_2O_3 capped HfO_2 gate stack after a 1000 °C 30 s anneal.

poly-Si deposited at 540 °C on top of HfO_2 resulted in improved electrical properties compared to 620 °C poly-Si/HfO_2 and no inhomogeneous silicon grain growth was observed. However, leakage for these films was also very high compared to the platinum metal gate/HfO_2 results. Due to the very high leakage for 620 °C poly-Si/HfO_2 stacks, the capacitance–voltage curve is often anomalous and the maximum capacitance (C_{max}) becomes undeterminable.

Similar to poly-Si on HfO_2, cross-sectional TEM studies (Fig. 2) of poly-Si deposited on top of Al_2O_3 capped HfO_2 indicate no evidence of gross interfacial reaction even after dopant activation anneals of 1000 °C. Figure 3 shows the relationship of the observed inhomogeneous grain growth, or starlights (see Fig. 1), to the number of ALD cycles of Al_2O_3 applied on top the HfO_2. Ten cycles of ALD–Al_2O_3 is estimated to be close to one complete monolayer of Al_2O_3. Thus, Fig. 3 indicates that one monolayer of Al_2O_3 is sufficient to prevent the observed poly-Si inhomogeneous grain growth seen with the poly-Si/HfO_2 gate-stack. Figure 4 shows the $I-V$ electrical results for boron-implanted 620 °C deposited poly-Si gate/ALD–Al_2O_3 capped MOCVD–HfO_2 MOSCAPs. Upon adjusting for flatband-voltage (V_{fb}) differences, an observed leakage reduction greater than a 10^4 times is measured for ALD–Al_2O_3 capped HfO_2 compared to films with the 620 °C poly-Si gate deposited directly on to HfO_2 or SiO_2 controls of similar electrical thickness.

We speculate that the observed inhomogeneous grain growth is caused by a low density of locally hafnium rich sites on the polycrystalline HfO_2 surface which promote poly-Si nucleation and rapid grain growth. These hafnium rich sites are attributed to local reduction of the HfO_2 surface in the poly-Si deposition ambient. The inhomogeneous grain

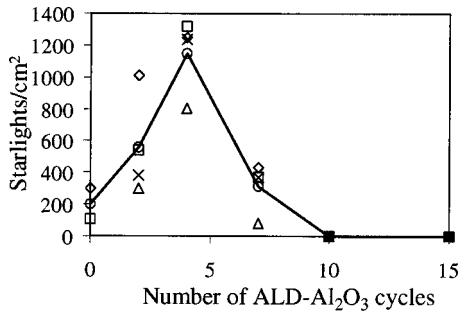

FIG. 3. Density of observed starlight inhomogeneous grains vs the number of ALD–Al_2O_3 cycles (1 cycle = TMA pulse + H_2O pulse).

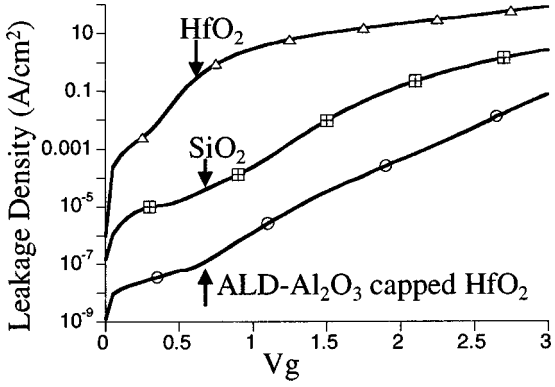

FIG. 4. $I-V$ data for similar electrical thickness films with 620 °C LPCVD Si-gate and HfO_2, SiO_2, or ALD–Al_2O_3 capped HfO_2 dielectrics.

growth is thought to be related to the reported metal induced lateral crystallization of amorphous silicon films in which contact of the amorphous film with metals causes very large grains to grow.[7,8] Partial coverage of HfO_2 by amorphous Al_2O_3 can cover some of these hafnium rich sites (i.e., local HfO_2 sites susceptible to reduction during poly-Si deposition) but also adds nucleation sites at the Al_2O_3/HfO_2 border. As the amorphous Al_2O_3 approaches complete coverage of the HfO_2, the density of available sites for rapid poly-Si growth decreases until at approximately one monolayer Al_2O_3 coverage, none of these sites are available and no starlight is observed.

Thermodynamic calculations using bulk material data do not predict a reaction for HfO_2 with silicon[9] or SiH_4[10] at the process temperatures and pressures used. However, bulk thermodynamic values are not generally applicable to atoms at grain boundaries or surfaces of ultrathin films. The high leakage current may be related to a partial reduction of HfO_2 at grain boundaries and more probably, at grain boundary triple points where bonding is least perfect. Thus, one plausible reaction could be a reduction of HfO_2 at the grain boundaries during the CVD–Si process by SiH_4, or its decomposition by-products, which leads to high leakage currents perhaps by trap assisted tunneling. When the HfO_2 is capped with a thin amorphous Al_2O_3 layer, the adverse reaction between HfO_2 and SiH_4 is prevented resulting in the low leakage expected for an insulating film.

In summary, it can be generally stated that LPCVD silicon gate using SiH_4 deposited directly onto HfO_2 resulted in (1) a low density of large poly-Si grains and (2) much higher leakage compared to similar HfO_2 films using Pt metal gates and poly-Si/SiO_2 controls. However, conventional LPCVD silicon gates deposited at 620 °C on ALD–Al_2O_3 capped HfO_2 resulted in the absence of large inhomogeneous poly-Si grains and well behaved capacitors with greater than a 10^4 times reduction in gate leakage compared to films with the 620 °C poly-Si gate deposited directly on to HfO_2 or 620 °C poly-Si/SiO_2 controls of similar electrical thickness. We attribute the two observed adverse phenomena for conventional poly-Si deposited directly on HfO_2 to a partial reduction of the HfO_2 by the poly-Si deposition ambient. In the first case (1) the partial reduction occurs locally on the HfO_2 surface, while in the second case (2) the partial reduction occurs at grain boundary triple points.

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