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Observation of memory effect in germanium nanocrystals embedded in an amorphous silicon oxide matrix of a metal–insulator–semiconductor structure

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The memory effect of a trilayer structure (rapid thermal oxide/Ge nanocrystals in SiO_2/sputtered SiO_2) was investigated via capacitance versus voltage ($C-V$) measurements. The Ge nanocrystals were synthesized by rapid thermal annealing of the cosputtered $Ge+SiO_2$ films. The memory effect was manifested by the hysteresis in the $C-V$ curve. Transmission electron microscope and $C-V$ results indicated that the hysteresis was due to Ge nanocrystals in the middle layer of the trilayer structure. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1459760]

The increasing use of portable electronics and embedded systems has resulted in a need for low-power high-density nonvolatile memories. Current floating-gate flash memory cells use a relatively thick tunnel oxide to prevent direct tunneling current leakage to ensure a good data retention capability and to reduce the off-state power consumption of the memory array. However, such a thick tunnel oxide means that the write and erase pulse durations during programming of the flash memory are relatively long and these compromise the programming speed of the device. Tiwari *et al.*[1] proposed a silicon (Si) nanocrystal memory device that can be programmed at fast speeds (hundreds of nanoseconds) using low voltages for direct tunneling and storage of electrons in Si nanocrystals. By using nanocrystal charge storage sites that are isolated electrically, charge leakage through localized oxide defects is reduced. King *et al.*[2,3] also demonstrated a germanium (Ge) nanocrystal memory device that can be programmed at low voltages and high speeds. This device was fabricated by implanting Ge atoms into a Si substrate. However, the implantation process can cause Ge to locate at the silicon–tunnel oxide interface, forming trap sites that can degrade device performance.

Recently, we reported structural results of Ge nanocrystals synthesized by the rapid thermal annealing (RTA) technique.[4,5] We showed that Ge nanocrystal growth is critically dependent on the Ge concentration and the RTA conditions. In this letter, we report observations of memory effect of Ge nanocrystals fabricated using a trilayer structure.

The devices used in this work have a metal–insulator–semiconductor (MIS) structure. The insulating layer consists of a trilayer structure. A thin (5 nm) SiO_2 layer was grown on a *p*-type silicon substrate in dry oxygen ambient using rapid thermal oxidation at 1000 °C. A $Ge+SiO_2$ layer of thickness 20 nm was then deposited by the radio frequency (rf) cosputtering technique. Details of the cosputtering process can be found in our previous paper.[4] The sputtering target was a 4 in. SiO_2 (99.999% pure) disk with six pieces of undoped Ge ($10\ mm\times 10\ mm\times 0.3\ mm$) attached. The argon pressure and rf power were fixed at 3×10^{-3} mbar and 100 W, respectively. A third pure SiO_2 layer (50 nm) was then deposited by rf sputtering in argon at rf power of 100 W and sputtering pressure of 3×10^{-3} mbar. The trilayer structure was then rapid thermal annealed in argon ambient at 1000 °C for 300 s. The RTA ramp-up and ramp-down rates were fixed at 30 °C/s.

Figure 1 shows the capacitance versus voltage ($C-V$) characteristics of a trilayer structure device (device A). It can be seen that device A exhibits counterclockwise hysteresis (~6 V). Note that all our A devices (25 devices tested) showed hysteresis larger than 4 V. Wahl *et al.*[6] and Shi *et al.*[7] observed hysteresis of ~2–2.5 V (for a voltage sweep of −5–+5 V) for a Si nanocrystal transistor structure with 1.8 (Ref. 6) and 2.4 nm (Ref. 7) tunnel oxide layers, respectively. Note that the hysteresis width depends on the range of the voltage sweep in the $C-V$ measurements and on the device structure.

Figure 1 also shows the $C-V$ curve of another trilayer structure device (device B) with the middle layer consisting of 20 nm thick pure sputtered oxide. Counterclockwise hysteresis was also observed but was of smaller width (0.73 V).

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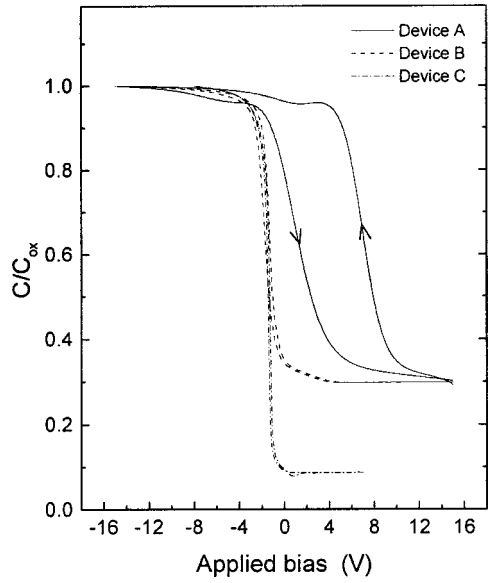

FIG. 1. Capacitance vs voltage characteristics of trilayer structure devices: device A [RTO SiO_2 (5 nm)–Ge+SiO_2 (20 nm)–sputtered SiO_2 (50 nm)] and device B [RTO SiO_2 (5 nm)–sputtered SiO_2 (20 nm)–sputtered SiO_2 (50 nm)], and two-layered structure device C [RTO SiO_2 (5 nm)–Ge+SiO_2 (20 nm)].

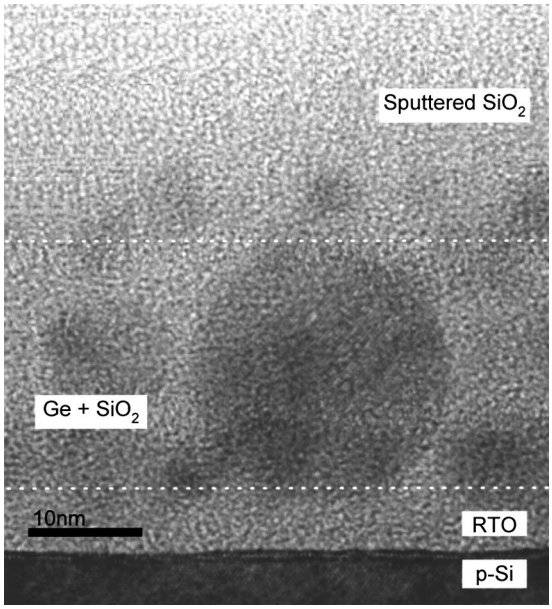

FIG. 2. Transmission electron micrograph of the trilayer structure rapid thermal annealed at 1000 °C for 300 s. The trilayer structure consists of 5 nm of RTO SiO_2, 20 nm of a cosputtered Ge+SiO_2 layer, and a 50 nm of pure sputtered SiO_2 (device A).

Note that a trilayer structure similar to device B, but with no RTA step, showed hysteresis of 1.09 V. This means that the RTA process improved the sputtered oxide's quality and reduced the trapped charge density in device B from 3.62×10^{11} (as prepared) to 1.98×10^{11} cm^{-2} (after RTA). The pronounced hysteresis exhibited by device A must therefore be due to charge storage in the Ge nanocrystals located in the middle layer. Note that Shi *et al.*[7] attributed the memory effects of their metal–oxide–semiconductor memory devices to charge stored at deep traps in Si nanocrystals. We are presently investigating this as the possible charge storage mechanism in our devices. The existence of Ge nanocrystals in the middle layer will be discussed further in the transmission electron microscope (TEM) results that will be presented later.

Note that device A also shows a significant positive shift (~4 V) and a $C-V$ curve with a gentler slope compared to device B. Since the hysteresis width is approximately 6 V, this means that device A has better charge storage capability than device B. Ahn *et al.*[8] suggested that, in a system that contains Si–O–Si and Si–O–Ge bonds, the Ge–O bond is weaker and can be broken easily, leaving a Si–O–dangling bond structure. We have shown in our previous x-ray photoelectron spectroscopy (XPS) results[5] that the 1000 °C annealed sample contained a substantial amount of GeO_x bonds. This dangling bond structure can then trap an electron and become negatively charged. The significant positive shift of the $C-V$ curve of device A may be due to the trapping of electrons by dangling bonds. The gentler slope of the $C-V$ curve of device A is a result of the large voltage shift induced by the charge stored in the nanocrystals. This was verified by $C-V$ measurements at different delay times, i.e., to simulate different sweep rates.

Figure 2 shows a TEM micrograph of device A. It can be seen from this micrograph that the middle layer consists of Ge nanocrystals of different sizes. It is interesting to note that Ge nanocrystals of diameter (δ) ~20 nm formed near the RTO SiO_2-sputtered Ge+SiO_2 interface and smaller Ge nanocrystals with δ of ~6 nm formed at the RTO SiO_2-sputtered Ge+SiO_2 and the sputtered Ge+SiO_2-pure sputtered oxide interfaces. There seem to be more Ge nanocrystals near the RTO SiO_2-sputtered Ge+SiO_2 interface than near the sputtered Ge+SiO_2-pure sputtered oxide interface. The center region of the middle layer contains many fewer Ge nanocrystals. Fukuda *et al.*[9] pointed out that, at 1000 °C, Ge can diffuse significantly in oxide. Heinig *et al.*[10] suggested that, since the concentration of Ge dissolved in SiO_2 is lower than the solubility at the Si–SiO_2 interface and higher at the bulk of the oxide, the concentration gradient can lead to diffusion flux, resulting in an accumulation of Ge at the interface. We suggest that when device A was annealed at 1000 °C, significant Ge diffusion towards the two interfaces took place. The process described by Heinig *et al.*[10] can account for the larger number of Ge nanocrystals near the two interfaces and the smaller number of Ge nanocrystals in the center region of the middle layer. We are, however, not able to provide a reason presently for the preferential formation of big nanocrystals or the higher number of smaller nanocrystals at the RTO SiO_2-sputtered Ge+SiO_2 interface.

Figure 3 shows a TEM micrograph of a two-layered device (device C) that consists of a 5 nm RTO SiO_2 layer and a 20 nm Ge+SiO_2 layer. The device was rapid thermal annealed at 1000 °C for 300 s. It can be seen from this Fig. 3 that Ge nanocrystals are only located at the RTO SiO_2-sputtered Ge+SiO_2 interface. Because this device was fabricated without an oxide cap layer, it is reasonable to expect significant outdiffusion of Ge to occur during RTA at 1000 °C.

The $C-V$ characteristic of device C in Fig. 1 exhibits small hysteresis of <0.5 V. The smaller normalized minimum capacitance of device C compared to the other devices in Fig. 1 is due to a thinner total oxide thickness (25 nm) in

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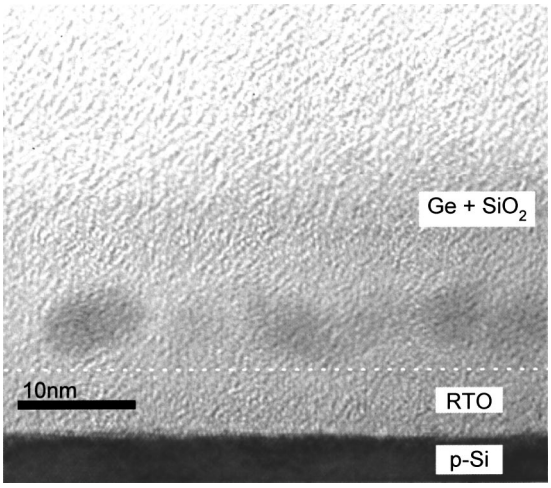

FIG. 3. Transmission electron micrograph of the two-layered structure rapid thermal annealed at 1000 °C for 300 s. The two-layered structure consists of 5 nm of RTO SiO_2 and 20 nm of a cosputtered $Ge+SiO_2$ layer (device C).

device C. Since the Ge nanocrystals are much fewer in number in device C, it is reasonable to expect the charge storage capacity of this device to be more reduced compared to in device A. Note that the leakage current density ranged between 10^{-8} and 10^{-9} A cm^{-2} with 3 V applied to the gate electrode. We feel that this leakage current density is relatively low for this trilayer structure with a 5 nm RTO layer.[11] We are currently experimenting with devices of different geometries, RTA conditions, and Ge concentrations to optimize performance of the device.

In conclusion, we have demonstrated a trilayer structure with Ge nanocrystals embedded in the middle SiO_2 layer that has potential for application in memory devices. This layer is formed via cosputtering of a $Ge+SiO_2$ target. The Ge nanocrystals were synthesized by the RTA method.

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