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High quality Ge on Si by epitaxial necking

T. A. Langdo,[a] C. W. Leitz, M. T. Currie, and E. A. Fitzgerald
Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139

A. Lochtefeld and D. A. Antoniadis
Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139

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We show that pure Ge grown selectively on SiO_2/Si substrates in 100 nm holes is highly perfect at the top surface compared to conventional Ge lattice-mismatched growth on planar Si substrates. This result is achieved through a combination of interferometric lithography SiO_2/Si substrate patterning and ultrahigh vacuum chemical vapor deposition Ge selective epitaxial growth. This ''epitaxial necking,'' in which threading dislocations are blocked at oxide sidewalls, shows promise for dislocation filtering and the fabrication of low-defect density Ge on Si. Defects at the Ge film surface only arise at the merging of epitaxial lateral overgrowth fronts from neighboring holes. These results confirm that epitaxial necking can be used to reduce threading dislocation density in lattice-mismatched systems. © *2000 American Institute of Physics.* [S0003-6951(00)01425-X]

Heteroepitaxial growth can be used to fabricate many modern semiconductor devices where lattice-matched substrates are not commercially available or to potentially achieve monolithic integration with silicon microelectronics.[1] For heteroepitaxial layers grown beyond a critical thickness, misfit dislocations are formed at the substrate/film interface and typically terminate at the film surface as threading dislocations. The threading dislocation segments can degrade physical and electrical properties of device material and can lead to premature device failure and poor performance. As a result there has been much effort to eliminate threading dislocations in lattice-mismatched epitaxy, most notably in the recent development of GaN devices. Defect densities have been greatly reduced in GaN growth by a combination of substrate patterning and epitaxial lateral overgrowth (ELO) techniques[2,3] leading to fabrication of laser diodes with record lifetimes.[4] This process eliminates defects in ELO regions but highly defective seed windows remain, necessitating repetition of the lithography and epitaxial steps to eliminate all substrate defects. In a competing scheme, pendeo-epitaxy eliminates all substrate interface defects but requires one lithography and two epitaxial growth steps.[5] Furthermore, both techniques require the increased lateral growth rate of GaN, which has not been demonstrated in all heteroepitaxial systems.[3,5] A general defect-reduction process utilizing a minimum of lithography/epitaxy steps that does not rely on increased lateral growth rates would be very advantageous. Such a process would both minimize process complexity and allow application to many materials systems.

We present experimental demonstration of defect blocking by epitaxial necking resulting in a defect-free top Ge surface on Si. Epitaxial necking offers process simplicity by eliminating all defects from the substrate interface in one substrate lithography and epitaxial growth step over both the seed window and ELO regions without relying on increased lateral growth rates. This result is achieved through a combination of selective epitaxial growth and defect crystallography to force defects to the oxide sidewall, resulting in a perfect top film.[6] In the (111)⟨110⟩ diamond cubic slip system misfit dislocations lie along ⟨110⟩ directions in the (100) growth plane while the threading segments rise up on (111) planes in ⟨110⟩ directions. Threading segments in ⟨110⟩ directions on the (111) plane make a 45° angle to the underlying Si(100) substrate. Thus, if the aspect ratio of the holes in the oxide mask is greater than 1, crystallography dictates that threading segments will be blocked by the oxide sidewall resulting in a defect-free top Ge surface on Si as shown in Fig. 1.[6] This process is analogous to bulk Si Czochralski crystal growth where the seed crystal is first necked to eliminate defects before the boule is pulled.[7] Furthermore, epitaxial necking can be used to eliminate defects in any lattice-mismatched materials system in which threading dislocations are not parallel to the growth directions. Submicron lithography offers the possibility of achieving this goal in a reasonably small film thickness, thus minimizing thermal mismatch and cracking problems between the film and substrate.

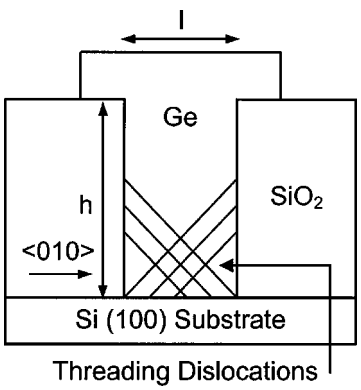

FIG. 1. Cross-section diagram demonstrating the principles of epitaxial necking showing zero threading dislocations at the Ge film surface.

[a]Electronic mail: tlangdo@mit.edu

Finally, an additional benefit of using submicron lithography is that defects have an extremely high energy in small volumes.[8] Therefore, small volumes tend to be perfect crystals. Results on relaxed films in slightly larger patterns from microns to hundreds of microns show that through dislocation travel and escape at pattern edges, misfit and threading dislocation densities can be controlled.[9–13] In terms of selective growth, several groups have demonstrated selective growth of Si and SiGe in submicron features by chemical vapor deposition (CVD)[14,15] and gas source molecular beam epitaxy.[16,17] However, there has been no previous motivation for combining selective growth and threading dislocation control at these dimensions.

The substrates in this experiment were 4 in. *p*-type 10–20 Ω cm Si (100) wafers with 120 nm thermal oxide. Substrate patterning was performed by a 351 nm interferometric lithography trilevel resist process and subsequent reactive ion etching to form wafer scale coverage of 100 nm holes.[18] The patterned substrates were cleaned with a 10 min piranha etch ($3\,H_2SO_4$:$1\,H_2O_2$), 30 s $50\,H_2O$:1 HF dip, and de-ionized water rinse/spin dry immediately before loading in the ultrahigh vacuum CVD (UHVCVD) loadlock. Selective growth was carried out in a turbo pumped hot-walled UHVCVD reactor with UHV loadlock with an 850 °C base pressure of 1×10^{-9} Torr. Prior to growth, substrates were desorbed for 10 min at 850 °C under UHV to remove any remaining native oxide from the substrate surface. A 25 nm selective Si buffer was grown at 650 °C with SiH_4/H_2 at a pressure of 0.8 mTorr to obtain a clean surface for Ge growth and improve Ge quality by minimizing stacking fault and twin formation. Ge was then selectively grown at 650 °C with GeH_4/H_2 at a pressure of 1 mTorr until coalescence of ELO fronts from neighboring holes. ⟨110⟩ oriented cross-section transmission electron microscopy (TEM) samples were prepared by mechanical polishing and Ar ion milling. TEM images were taken on a JEOL 2000FX microscope operating at 200 kV. Triple axis x-ray diffraction scans were preformed on a Bede D^3 x-ray diffractometer with a Rigaku rotating anode source.

Figure 2 shows termination of a stacking fault from the Si/Ge substrate interface at the SiO_2 sidewall resulting in a perfect top Ge surface on Si. There is no defect generation at the oxide sidewall or by merging of ELO fronts. Furthermore, there is no evidence of defect interactions causing substrate defects to be deflected and thus zigzag out of the hole. The observed defect reduction could occur by other mechanisms in addition to epitaxial necking. The stress state of the Ge in the small holes can be altered due to edge effects[6] or image forces could force defects to glide to the sidewall where they are removed.[8] However, at this point it is unclear which mechanism is dominant.

Figure 3 shows the film morphology arising from coalescence of multiple Ge ELO fronts and the selected area diffraction pattern. The extra diffraction twin spots show the predominance of microtwin defects that have been commonly found in ELO fronts in Si.[19] Defects propagating into the coalesced Ge film only occur sporadically at the merging of ELO fronts as twins and stacking faults, not as threading segments from the lattice-mismatched interface with the Si substrate or from the oxide sidewall. Note that all the Ge

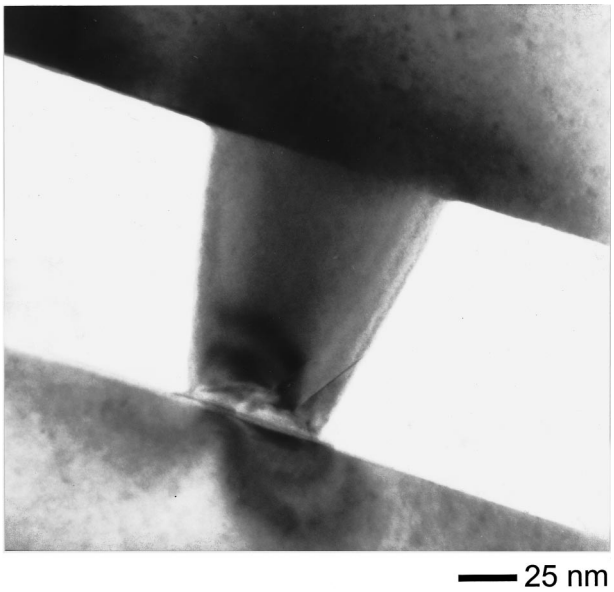

FIG. 2. Cross-section TEM image showing stacking fault blocked by the oxide sidewall and defect free Ge seed and ELO regions.

pillar ''seeds'' lack propagating threading dislocations. Furthermore, since only half of the ELO boundaries exhibit defects, these are encouraging results for potentially creating defect-free blanket Ge on Si. There are several possible causes of the observed defects upon coalescence. Defects similar to these in Si ELO have been attributed to insufficient time for adatoms to reach stable atomic arrangements because of complex faceting[20,21] or oxide surface roughness resulting in lattice misregistry at the merging fronts.[21,22] Another possible explanation is that defects between growth fronts are caused by stresses from superposition of the Ge lattice on the underlying Si lattice. Once growth fronts from neighboring holes coalesce, the Ge lattice must bridge the distance between holes over the SiO_2/Si substrate. However, the distance between holes in the SiO_2/Si substrate is not necessarily an integral number of Ge unit cells. The lattices could differ by a Ge unit cell resulting in a strain measured

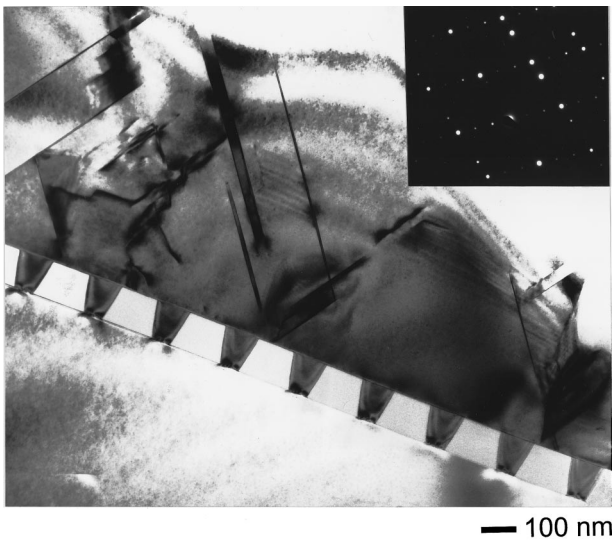

FIG. 3. Cross-section TEM image showing Ge film morphology and selected area diffraction pattern. All Ge seeds lack propagating defects; the defects in the image originate from ELO coalescence.

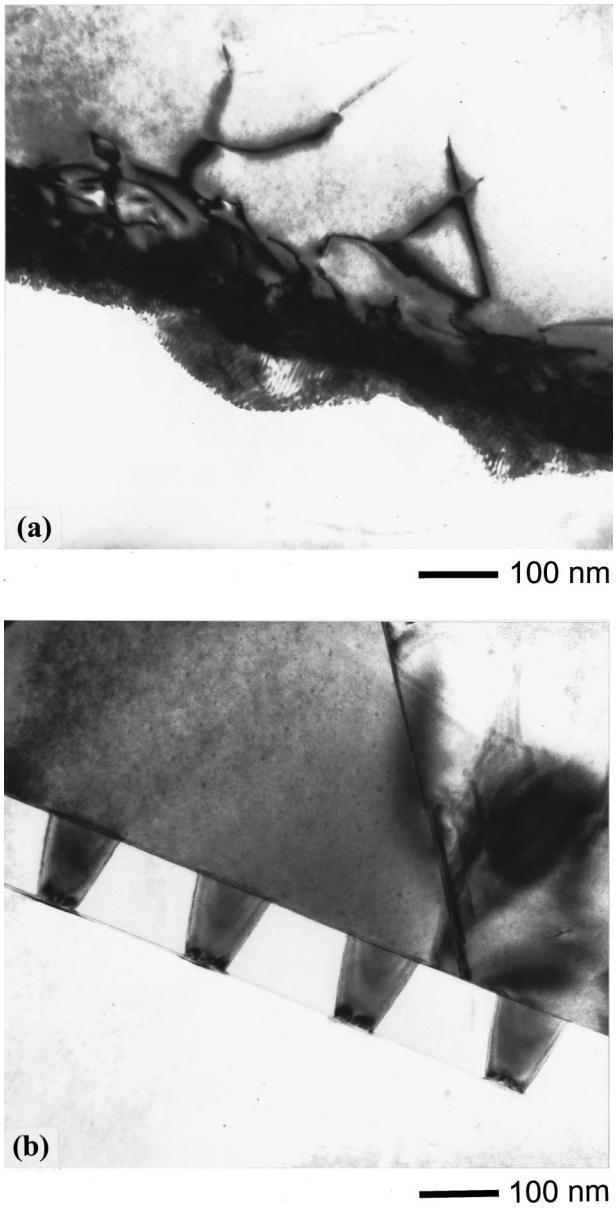

FIG. 4. (a) Control Ge/Si substrate interface on unpatterned Si. (b) Ge/Si substrate interface on interferometric lithography patterned substrates, shown at the same magnification as the control sample image in Fig. 4(a). Note the lack of a thick interfacial dislocation region as in Fig. 4(a).

as $\Delta L/L$ on the order of 0.5% causing defect formation (where ΔL is a Ge unit cell and L is the 100 nm spacing between holes). Growing in similarly sized holes with a wider hole spacing increases L, thus decreasing the strain, $\Delta L/L$. If this mechanism is responsible, sufficiently increasing the hole spacing should eliminate these defects.

Figures 4(a) and 4(b) compare the defect morphology between identical Ge growth on unpatterned Si and Ge growth in 100 nm features. Triple axis x-ray diffraction indicates that both Ge films are fully relaxed. By cross-sectional TEM the Ge film on unpatterned Si has a threading dislocation density greater than $10^8/\mathrm{cm}^2$, whereas substrate related defects are eliminated by growth in the nanoholes. Also, we observe that the Ge film on unpatterned Si has a defective interface region about 250 nm thick. In contrast, Ge grown in nanoholes exhibits a much simpler defect morphology resulting in a 25 nm thick region containing all misfit dislocations. The improved defect morphology shows that an interface array that locally relieves the mismatch is generated very soon upon Ge growth in the nanoholes.

We have demonstrated the feasibility of low defect density Ge on Si via epitaxial necking on SiO_2/Si substrates patterned by interferometric lithography. All defects viewed in cross-section TEM that originate from the Si substrate/Ge film interface are blocked by the oxide sidewalls. Dislocations are occasionally observed at the merged ELO interfaces between highly perfect Ge seeds. Investigations into the origins of ELO Ge defects are ongoing with hopes of realizing high quality Ge on Si. This approach allows the elimination of all substrate interface defects in one lithography and selective epitaxial growth step and shows promise for defect engineering in any lattice-mismatched materials system.

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