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# Ge nanocrystals in SiO<sub>2</sub> films

Takamitsu Kobayashi, Toshiaki Endoh, Hisashi Fukuda,<sup>a)</sup> Shigeru Nomura, Akira Sakai, and Yuji Ueda

Department of Electrical and Electronic Engineering, Faculty of Engineering, Muroran Institute of Technology, 27-1 Mizumoto, Muroran, Hokkaido 050, Japan

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SiO<sub>2</sub>/Ge nanocrystal/SiO<sub>2</sub> structures have been fabricated by deposition of Ge film on a SiO<sub>2</sub> layer and subsequent oxidation of the structure at a temperature between 800 °C and 1000 °C. Secondary ion mass spectrometry results indicate that the Ge precipitates into the bulk SiO<sub>2</sub> at a density of  $1 \times 10^{12} \text{ cm}^{-2}$ . Raman spectra show a sharp peak at  $300 \text{ cm}^{-1}$  for the nanocrystallized Ge. The nanocrystal diameter is determined to be 5 nm on average. In the metal-insulator-silicon structure, electron storage occurs in the SiO<sub>2</sub>/Ge/SiO<sub>2</sub> potential well via electron tunneling into the oxide film. Capacitance-voltage measurements indicate that flatband voltage ( $V_{\text{FB}}$ ) shifts to 0.91 V after the electron injection. The  $V_{\text{FB}}$  shift is attributed to the charge storing for a single electron per potential well. © 1997 American Institute of Physics. [S0003-6951(97)01035-8]

During the past few years, a considerable amount of attention has been focused on the strong photoluminescence (PL) in the visible wavelength range from nanostructures made of group IV elements, such as porous Si,<sup>1,2</sup> Si,<sup>3,4</sup> and Ge<sup>5-7</sup> nanocrystals prepared by various methods. To obtain three dimensionally confirmed systems, several groups have experimented with various techniques, for example, pyrolysis,<sup>8,9</sup> cosputtering,<sup>5,10,11</sup> pulsed-laser ablation,<sup>12</sup> spark processing,<sup>13</sup> and ion implantation.<sup>14</sup> For the Ge nanocrystals, most reports of visible PL from low-dimensional structures have involved Ge nanocrystals embedded in SiO<sub>2</sub>. To our knowledge, although the optical properties of these nanostructures have been extensively investigated, there are few studies on their electrical properties. Recent reports have been focused on room-temperature observation of negative differential conductance in a structure consisting of a SiC/Si/SiC<sup>15</sup> or SiO<sub>2</sub>/Si/SiO<sub>2</sub><sup>16</sup> matrix. For the SiO<sub>2</sub>/Si/SiO<sub>2</sub> system, the anomalous steps in the current-voltage ( $I$ - $V$ ) characteristics have been described.<sup>17</sup>

In this study, we fabricated Ge nanocrystals embedded in a SiO<sub>2</sub> matrix, and evaluated the crystallinity, distribution and electrical properties of the SiO<sub>2</sub>/Ge nanocrystal/SiO<sub>2</sub> structure. The Ge crystals of nanometer size were obtained using the conventional silicon fabrication process which is the primary process of the integrated circuit industry.

In the growth of the Ge nanocrystals in the SiO<sub>2</sub> film, 4-nm-thick tunnel SiO<sub>2</sub> film was first grown on a  $p$ -type 1-2  $\Omega \text{ cm}$  Si (100) substrate in a dry oxygen (O<sub>2</sub>) ambient at 900 °C for 5 min. Then, 10-nm-thick Ge film was deposited on the tunnel oxide using electron-beam evaporation at a substrate temperature of 60 °C and a base pressure of  $2 \times 10^{-7}$  Torr. The Ge layer was then annealed a temperature between 800 and 1000 °C for 1 h in a dry O<sub>2</sub> ambient. It is believed that due to the rapid diffusion of O<sub>2</sub> molecules through the Ge grain boundaries, the Ge became crystallized and embedded in the SiO<sub>2</sub> during high temperature oxidation. The total film thickness of the SiO<sub>2</sub> layer was 20 nm, determined by ellipsometry with a fixed refractive index of

1.460. The depth profile of Ge in the SiO<sub>2</sub> film was evaluated by secondary ion mass spectrometry (SIMS) using O<sub>2</sub><sup>+</sup> as a primary ion at 8 keV. Raman spectra were obtained using the 496.5 nm line of an Ar<sup>+</sup> laser as the excitation source. A cooled photomultiplier tube and photon counting electronics interfaced to a microcomputer were used to collect and analyze the data. For electrical measurements, aluminium (Al) gate electrodes (0.1 mm  $\phi$ ) were deposited after etching away of the SiO<sub>2</sub> on the wafer backside. An automatic semiconductor parameter analyzer was used in the capacitance-voltage ( $C$ - $V$ ) measurements of the metal-insulator-semiconductor (MIS) structures.

Typical SIMS depth profiles of Ge in the SiO<sub>2</sub> films are shown in Fig. 1. The Ge depth profiles seemed to be strongly dependent on the oxidation temperature. For the oxidation at 800 °C, Ge remains at the surface of the oxide with a small hump in the bulk oxide. In contrast, Ge near the surface of the oxide disappears upon oxidation at 1000 °C. In addition, the maximum concentration of Ge ( $2 \times 10^{18} \text{ atoms/cm}^3$ ) is

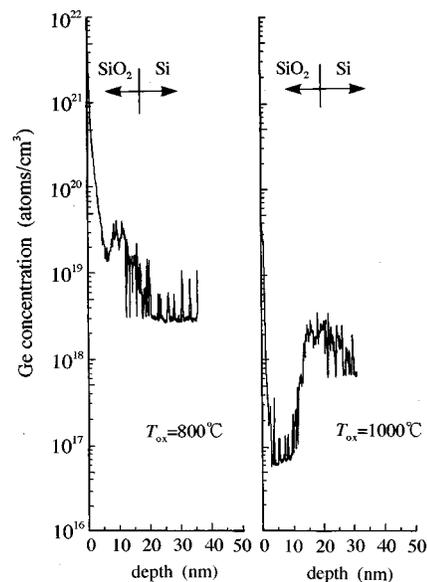


FIG. 1. The depth profiles of Ge in SiO<sub>2</sub> films after oxidation at 800 and 1000 °C.

<sup>a)</sup>Electronic mail: fukuda@waspet.cc.muroran-it.ac.jp

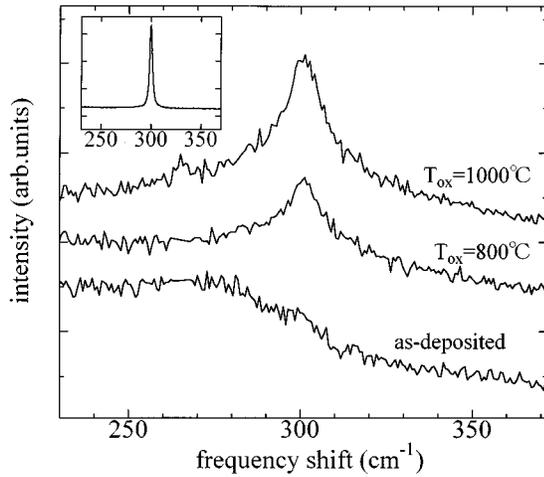


FIG. 2. Raman spectra for Ge layers as-deposited and oxidized at 800 and 1000 °C. The inset shows a Raman spectrum for unstrained Ge sample.

found near the SiO<sub>2</sub>/Si interface for the 1000 °C annealed sample. In our experiment, the Ge layer was initially deposited on a 4-nm-thick SiO<sub>2</sub> layer on a Si substrate, and then oxidized at a high temperature. It is interesting that diffusion of Ge in the SiO<sub>2</sub> layers is minimal during the oxidation. Moreover, a rapid nucleation of Ge occurs depending on the oxidation temperature. In oxidation at 800 °C, which is below the melting temperature of Ge (938.3 °C), the Ge nucleation process is in a period of transition where the Ge remains near the top oxide layer. With increasing oxidation temperature, Ge precipitates in the bulk SiO<sub>2</sub> layer, as shown in Fig. 1. The out-diffusion of Si from the substrate could influence the Ge nucleation and growth processes. It has been reported that the diffusion of Si atoms from the substrate enhances the precipitation of Ge in SiO<sub>2</sub>.<sup>18</sup> It is known that Ge oxide is thermodynamically less stable than SiO<sub>2</sub>.<sup>19</sup> Therefore, it should be easier for Ge than for Si to precipitate in SiO<sub>2</sub>. However, further investigation on the specific distribution of Ge nucleation sites after oxidation is required.

We measured Raman spectra for as-deposited and oxidized samples to determine the size of the Ge nanocrystals formed in SiO<sub>2</sub>. As shown in Fig. 2, the Raman spectrum of the as-deposited sample has a broad peak at around 270 cm<sup>-1</sup> attributed to the amorphous Ge-Ge mode. The crystallization of the amorphous Ge is evidenced by the narrowing and disappearance of the broad peak at around 270 cm<sup>-1</sup> and the onset of the sharp  $\Gamma_{25'}$  phonon peak at around 300 cm<sup>-1</sup> for the oxidized samples. In the Raman spectra of the bulk unstrained Ge crystals, the Ge-Ge peak is symmetric and centered at 300.5 cm<sup>-1</sup> with a full width at half maximum (FWHM) of 2.7 cm<sup>-1</sup>. The peak intensity ratio of the unstrained Ge to nanocrystalline Ge in SiO<sub>2</sub> was 18:1. With increasing oxidation temperature, a sharp Raman peak with an asymmetric shoulder at the low frequency side is found, as shown in Fig. 2. The average particle size was determined by use of a model of the Raman line shape of semiconductor nanocrystals, in which the half width of the maximum peak<sup>18</sup> and the peak shift<sup>20</sup> of the Raman peak are fitted to the data. The size of the Ge nanocrystals embedded in the SiO<sub>2</sub> is estimated to be 5 nm on average. The size of the Ge nanocrystals is in good agreement with the results

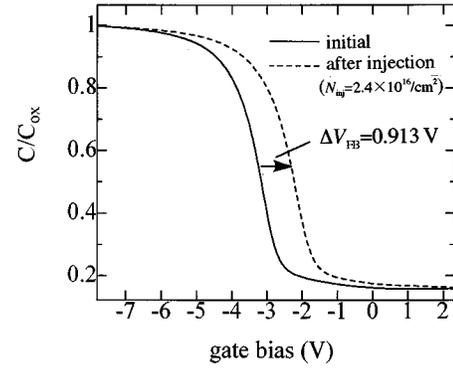


FIG. 3. Capacitance-voltage curves for the initial state and after electrons at  $N_{inj}=2.4 \times 10^{16}/\text{cm}^2$  were injected.

reported elsewhere in the previous literature.<sup>18,20</sup>

The multiple confinement of free carriers in quantum wells has led to several significant observations of physical phenomena and demonstrations of the usefulness of in electronic and optoelectronic devices.  $C-V$  measurement before and after forward constant voltage ( $V_{ap}$ ) stress was used to investigate charge storage in the Ge nanocrystals. As shown in Fig. 3, a positive voltage shift in the  $C-V$  curve is observed upon electron injection at  $N_{inj}=2.4 \times 10^{16}/\text{cm}^2$  with application of a bias of  $V_{ap}=15$  V. No flatband voltage shift ( $\Delta V_{FB}$ ) occurs upon electron injection in MIS capacitors without Ge nanocrystal in SiO<sub>2</sub>. Moreover, no distortion of the  $C-V$  curve after the injection due to of interface-trapped charge is observed. The number of electrons ( $N_{inj}$ ) that were injected into the oxide during stress was calculated by integration of the injected gate current density  $I_{ap}$  at constant stress voltage  $V_{ap}$  over the injection time.  $\Delta V_{FB}$  is defined as the flatband voltage point in the  $C-V$  curve measured between the initial state and after the electron injection. After the electron injection,  $V_{FB}$  shifts to 0.91 V, in a positive direction. This means that the negative charge buildup into SiO<sub>2</sub> occurs due to electron tunneling in electron traps from the substrate. If the charge buildup is significant, the experimental  $C-V$  curve will be shifted from the ideal theoretical curve, in which the magnitude of  $\Delta V_{FB}$  for a single electron per nanocrystal is approximately given by<sup>21</sup>

$$\Delta V_{FB} = \frac{qn_{\text{well}}}{\epsilon_{\text{ox}}} \left( t_{\text{ox}} + \frac{\epsilon_{\text{ox}} t_{\text{well}}}{2\epsilon_{\text{Si}}} \right), \quad (1)$$

where  $t_{\text{ox}}$  is the thickness of the oxide under the gate,  $t_{\text{well}}$  is the linear dimension of the nanocrystal well,  $\epsilon$ 's are the permittivities,  $q$  is the magnitude of the electronic charge, and  $n_{\text{well}}$  is the density of the nanocrystals. For the 5-nm-diam Ge nanocrystals located, i.e., a nanocrystal density of  $1 \times 10^{12} \text{ cm}^{-2}$  as estimated by SIMS, and an oxide thickness of 20 nm, the shift is calculated to be 0.9 V for one electron per nanocrystal. This value is in good agreement with the  $\Delta V_{FB}$  determined from the  $C-V$  curves. The Coulomb blockade effect can also be very significant at these dimensions. The Coulomb charging energy ( $q^2/2C_n$ , where  $C_n$  is the nanocrystal capacitance) for a 5-nm-diam nanocrystal of Ge in SiO<sub>2</sub> is about 74 meV. Not only is it larger than the thermal energy, but it also limits additional injection of carriers in to the nanocrystal.

In summary, we have fabricated a Ge nanostructure embedded in SiO<sub>2</sub> by deposition of Ge on SiO<sub>2</sub> and subsequent high temperature oxidation. SIMS revealed that the out-diffusion of Ge toward the SiO<sub>2</sub> layer was minimal. At the temperature of 1000 °C, the Ge layer in the SiO<sub>2</sub> grew with a concentration of  $1 \times 10^{12}$  atoms/cm<sup>2</sup>. Raman spectra showed that after oxidation the Ge layer precipitated and crystallized in the SiO<sub>2</sub>. The *C*–*V* measurement results indicate that after the electron injection into SiO<sub>2</sub>, electrons are captured in each SiO<sub>2</sub>/Ge/SiO<sub>2</sub> quantum well.

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