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Structural and Electrical Properties of Low-Temperature, Low-Pressure SiO_2 on Si

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ABSTRACT

The physical and electrical properties of SiO_2 deposited on Si at low pressure (2-10 Torr) and low temperature (100-300°C) are reported. Fourier transform infrared spectroscopy (FTIR) is used to examine the chemical nature of the deposited oxide as a function of deposition and anneal temperature. Films deposited at $T<200$°C reveal partially oxidized silicon along with water and silanol groups. As the deposition temperature is raised to 300°C, the FTIR spectra resemble that of thermal oxide. Annealing of films deposited at lower temperatures significantly improves the films, also causing the FTIR peaks to resemble those of thermal oxide. Capacitance-voltage measurements are used to extract fixed-charge and interface-state densities. Fixed-charge densities below 1×10^{11} cm^{-2} and interface-state densities below 5×10^{10} cm^{-2} eV^{-1} are obtained after rapid thermal annealing of SiO_2 on Si. Bias-temperature stressing is used to investigate slow trapping instabilities observed after rapid thermal annealing.

Advances in silicon device technology have fueled research in low-temperature insulating film deposition. Submicron devices in ultra-large-scale integrated circuits require precise placement of dopant impurities, restricting process temperatures in order to reduce impurity diffusion. Multilayer interconnect technologies require insulator deposition temperatures compatible with semiconductor contact processing. New silicon technologies such as self-aligned silicide (1) and lightly-doped drain structure (2) require the lowest possible processing temperatures. Other applications of deposited oxides exist in silicon-on-insulator technologies, where a large quantity of bulk silicon for thick oxide growth is simply not available. In addition to silicon electronic device applications, the increasing importance of III-V materials for opto-electronic devices has intensified the need for an integrable dielectric passivation technology. The native oxides of InP and GaAs lack the electrical, mechanical, and interfacial properties necessary for making usable devices (3); therefore silicon dioxide, with its excellent electrical and mechanical properties and thoroughly studied deposition technologies, would seem to be an attractive alternative. However, traditional SiO_2 deposition technologies require temperatures well above the dissociation point of the group V element in many III-V compounds.

Various methods of low temperature SiO_2 deposition have been studied recently, including pyrolytic decomposition (4, 5), plasma-enhanced chemical vapor deposition (PECVD) (6), remote plasma-enhanced chemical vapor deposition (RPECVD) (7), and photo-enhanced chemical vapor deposition (Photo-CVD) (8, 9). These techniques involve the excitation of gas species by heat, electrical discharge, or ultraviolet light, resulting in complex reactions both in the gas phase and on the surface. In most processes the oxidizing species is excited, resulting in enhanced native oxide growth prior to deposition (10). In some cases the excited gas molecules can attain enough energy to irreversibly damage the substrate upon impact.

We have chosen to investigate low-temperature (100-300°C), low-pressure (2-10 Torr) chemical vapor deposition

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(CVD). Silane and oxygen are mixed prior to entering a radial flow reactor and deposition is achieved by a pyrolytic process at the substrate surface. No additional reaction enhancement is necessary. Similar work on atmospheric-pressure CVD of borophosphosilicate glass showed improved reaction efficiency and lower particle contamination by lowering deposition temperature and increasing oxygen/hydride ratio (11). By adjusting deposition parameters, homogeneous gas phase nucleation can be minimized and the heterogeneous CVD reaction maximized. Previous work done on characterization of our SiO_2 process includes analysis of optimal deposition parameters at various temperatures. It was found that deposition between 2-10 Torr occurred controllably down to 100°C over a broad range of O_2:SiH_4 ratios (12). Preliminary electrical measurements showed that our oxides have low fixed-charge densities (1×10^{11} cm^{-2}). Films deposited at temperatures between 150 and 300°C exhibited breakdown field strengths of 8-10 MV/cm, resistivities greater than 10^{15} Ω-cm, and refractive indices of 1.46 ± 0.01. Films deposited at 90-100°C exhibited breakdown field strengths of 5-8 MV/cm, resistivites of 10^{12}-10^{13} Ω-cm, and refractive indices of 1.44 ± 0.01 (13). Using this technique, SiO_2 films have been deposited on organic/inorganic diodes (14) and InP (15) as well as Si.

In this paper we determine the effects of deposition and processing parameters on the bulk structural, electrical, and interfacial properties of SiO_2 films deposited on silicon by our low-temperature, low-pressure technique. FTIR is used to examine the chemical nature of the deposited films and structural changes induced by post-deposition annealing. Ellipsometry is used to investigate densification and refractive index changes. Capacitance-voltage (C-V) techniques are used for the extraction of interface-trap density and determination of fixed-oxide charge density. Bias-temperature stressing (BTS) is used to determine the electrical stability of metal-oxide-semiconductor (MOS) structures after rapid thermal annealing.

Experimental

The deposition apparatus and method have been reported previously (12). The chamber has a base pressure of 50 mTorr. The deposition gases are electronic grade (99.999%) O_2 and 5.0% SiH_4 in N_2. Samples were deposited at temperatures between 100 and 300°C, with optimal pressures and gas flows (See Table I). Immediately prior to deposition, substrates used for infrared spectroscopy, ellipsometry, and etch rate studies were cleaned with MOS grade trichloroethylene, acetone, and methanol, after which the surface oxide layers were removed with dilute hydrofluoric acid. Samples were then rinsed in deionized water and dried with nitrogen.

FTIR spectroscopy was performed to investigate the effects of deposition temperature and annealing on the structure of deposited SiO_2 films. A Perkin-Elmer 1600 FTIR was used in the transmission mode for all spectra. Silicon substrates, polished on both sides, were used to minimize back surface scatter. A similar bare Si wafer was used in the background scan in order to compensate for the substrate lattice absorption bands. Since vibrational frequencies vary with thickness (16) films of similar thickness were used in comparative studies. Ellipsometric data was collected on a Gaertner model L116B auto-gain ellipsometer at a wavelength of 632.8 nm. Oxides at or near a half-cycle thickness were used.

Table I. Deposition conditions for low temperature SiO_2.

Temperature (°C)	Pressure (Torr)	SiH_4 (5%) Flow rate (sccm)	O_2 Flow rate (sccm)
100	6.5	100	20
150	4.0	100	50
200	3.0	100	50
300	3.0	100	50

Substrates used for electrical measurements were (100) p^+-Si with 10 μm, $p = 2 \times 10^{16}$ cm^{-3} epitaxial layers. Wafers were subjected to an RCA clean, dilute hydrofluoric acid dip, and deionized water rinse. Immediately after cleaning, the samples were loaded into the deposition chamber. After oxide deposition, the samples were annealed at various temperatures and times in a HeatPulse 210 rapid thermal anneal (RTA) system. After post-deposition annealing, Al electrodes were deposited on the oxide layer and backside. After metallization, the samples were subjected to a one min, 300°C anneal to ensure ohmic contact was made to the substrate.

High-frequency C-V measurements were made with an HP 4275A LCR meter and quasi-static C-V measurements with a Keithley 595 meter. Ion-current measurements were also performed with the quasi-static meter operating in the current measurement mode. BTS measurements were performed as a function of field strength, substrate temperature, and time. Bias was applied at room temperature and remained on until the completion of the temperature cycle. The hot chuck consisted of a thin brass plate heated from behind by a 750 W tungsten-halogen lamp. Temperature was monitored by a small-bead chromel-alumel thermocouple positioned on the surface of the brass plate within 5 mm of the sample.

Results and Discussion

Structural characterization.—Figure 1 shows FTIR scans of SiO_2 films deposited at 100, 200, and 300°C. The films deposited at 100°C exhibit water (absorption at 3330 cm^{-1}), silanol groups (absorption at 3650 and 950 cm^{-1}), and partially oxidized Si (absorption at 880 cm^{-1}). At 200°C, there is a decrease in the amount of water and silanol groups, as well as in partially oxidized Si. At 300°C, the spectrum resembles that of thermal SiO_2 with the excep-

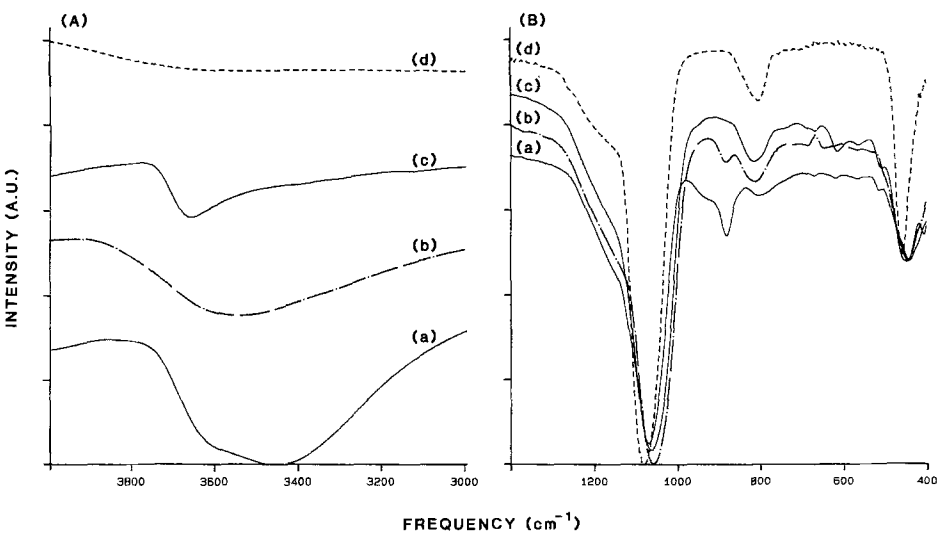

Fig. 1. FTIR spectra of SiO_2 (a) T_{dep} = 100°C, P_{dep} = 6.5 T, d_{ox} = 3166 Å, n_f = 1.43; (b) T_{dep} = 200°C, P_{dep} = 3 T, d_{ox} = 3710 Å, n_f = 1.462; (c) T_{dep} = 300°C, P_{dep} = 3 T, d_{ox} = 3640 Å, n_f = 1.460; (d) Thermal oxide, T_{dep} = 1100°C, n_f = 1.464, d_{ox} = 3000 Å.

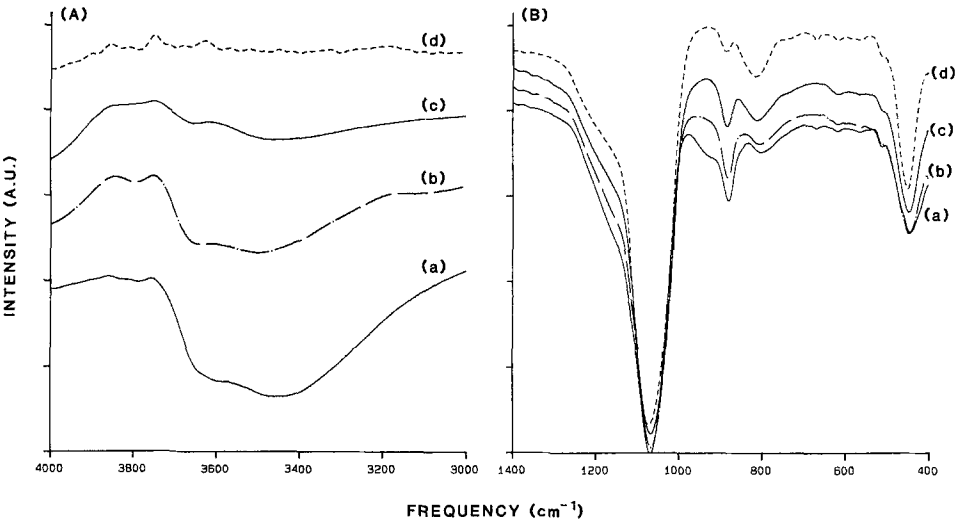

Fig. 2. FTIR spectra of SiO_2 deposited at 100°C, 3 *T*, for different anneals. a) no anneal, $n_f = 1.430$; b) anneal 400°C, 10 s in N_2, 3% densification, $n_f = 1.427$; c) anneal 600°C, 10 s in N_2, 5% densification, $n_f = 1.415$; d) anneal 800°C, 10 s in N_2, 9% densification, $n_f = 1.414$.

tion of a small amount of silanol groups present. Note the strong bands at approximately 1058, 812, and 450 cm^{-1} for the 300°C sample, due to Si-O bond stretching, bending, and rocking modes, respectively. Thus, as the deposition temperature is raised, less water is found in the films, they become more stoichiometric, and the bands become closer to those of thermal oxide (17).

Pliskin has done quantitative analysis of the water and silanol content of deposited SiO_2 films as a function of the 3650 and 3330 cm^{-1} band intensities (18). He found the water content of the films is given by

$$W = (-14A_{3650} + 89A_{3330})(2.2/\rho) \quad [1]$$

and the silanol content is given by

$$S = (179A_{3650} - 41A_{3330})(2.2/\rho) \quad [2]$$

where W is the weight percent of water, S is the weight percent of OH present as silanol, ρ is the density of the film, and A_{3650} and A_{3330} are the absorbance per micron of film at 3650 and 3330 cm^{-1}, respectively. For SiO_2 deposited at 100°C, the water and silanol content were estimated to be 6.6 and 6.3%, respectively. The effects of annealing the 100°C film are shown in Fig. 2. A 600°C, 10 s anneal in nitrogen reduced both water and silanol to approximately 1.6%. Films deposited at 200°C have less water and silanol, which also decreases to 1.6% upon annealing at 600°C. Films deposited at 300°C showed only a small amount of silanol groups with no water absorption band visible. The silanol absorption was easily removable by annealing above 600°C.

The main stretching frequency of Si-O (1062 cm^{-1}) in films deposited at 200 and 300°C is the same for films of the same thickness, (Fig. 3a) while both are lower than the stretching frequency for a thermal oxide (1082 cm^{-1}) of equal thickness. Films deposited at 100°C have a higher Si-O stretching frequency (1070 cm^{-1}) than the 200 and 300°C films. While it is a general trend for the stretching frequency to increase with increasing density, we know from refractive indices (Fig. 3b) and P-etch (19) rates (Fig. 3c) that the films deposited at 100°C are less dense and more porous than films deposited at higher substrate temperatures. The presence of −OH groups in low T films appears to increase the stretching frequency of the Si-O group. Note that, with annealing, the Si-O stretching frequency of the 100°C oxide decreases and it can be seen in the infrared spectra of Fig. 2 that this corresponds to a removal of much of the water and bound silanol groups. Once the majority of the water and silanol groups have been removed, further annealing results in increased Si-O stretching frequency, probably due to increased density, as seen in the etch rate studies.

The refractive indices of films deposited at various temperatures for different annealing conditions are shown in Fig. 3b. Films deposited at 100°C have lower indices than films deposited at 200 and 300°C. As the annealing temperature is increased, the refractive index decreases. Pliskin, in his review of dielectric films deposited by various methods (20), has reported that more porous, less dense films tend to have lower refractive indices, while incorporation of water in the film tends to raise the refractive indexes. He also reported that annealing increased the density, which in turn increased the refractive index. We believe the lower refractive index of films deposited at 100°C is due to their decreased density, which is demonstrated by their increased P-etch rate (Fig. 3c). However, the low temperature films also have increased amounts of water and silanol groups, as seen in infrared spectra (Fig. 1). Initial annealing tends to decrease the amount of water and silanol incorporation, resulting in a corresponding decrease in refractive index, even though thickness measurements indicate the films are densifying. Measurement of film thickness by ellipsometry before and after annealing shows films deposited at 100°C densify by as much as 11% for a 10 s anneal at 800°C while films deposited at 300°C densify by only 3% for the same anneal conditions.

Analysis of our optical measurements indicates that films deposited at 100°C are less dense, oxygen-deficient, and have more adsorbed water and silanol groups than films deposited at T>200°C. The adsorbed water could be incorporated in the film during deposition, or become adsorbed by the film once removed from the deposition chamber. Annealing removes adsorbed species and causes the films to densify. Effective refractive index changes after annealing are primarily dependent on dehydration and elimination of silanol groups.

Electrical characterization.—Optical characterization of deposited oxides measures bulk physical properties. Interfacial properties are better characterized with electrical measurements such as C-V analysis (21). Typical C-V curves for films deposited at 150 and 300°C are shown in Fig. 4. Lower temperature depositions result in higher densities of fixed-charge. The spatial location of oxide charge can be determined from the dependence of flatband voltage (V_{FB}) on oxide thickness (22)

$$V_{FB} = -\frac{1}{\epsilon_{ox}}\left[Q_i d_{ox} + \int_0^{d_{ox}} \rho_{ox} x dx\right] + \phi_{ms} \quad [3]$$

where Q_i is the sheet charge density at the interface, ϵ_{ox} is the oxide permittivity, ρ_{ox} is the distributed charge density in the oxide, d_{ox} is the oxide thickness measured from the metal-oxide interface, and ϕ_{ms} is the work function difference between the metal and the semiconductor. Samples with charge located only at the oxide-semiconductor interface will demonstrate a flatband voltage linearly dependent on thickness. Interface charge is associated with dangling silicon bonds in the case of thermal oxides. In CVD oxides, interface charge depends strongly upon the chemistry and composition of the initial surface prior to deposi-

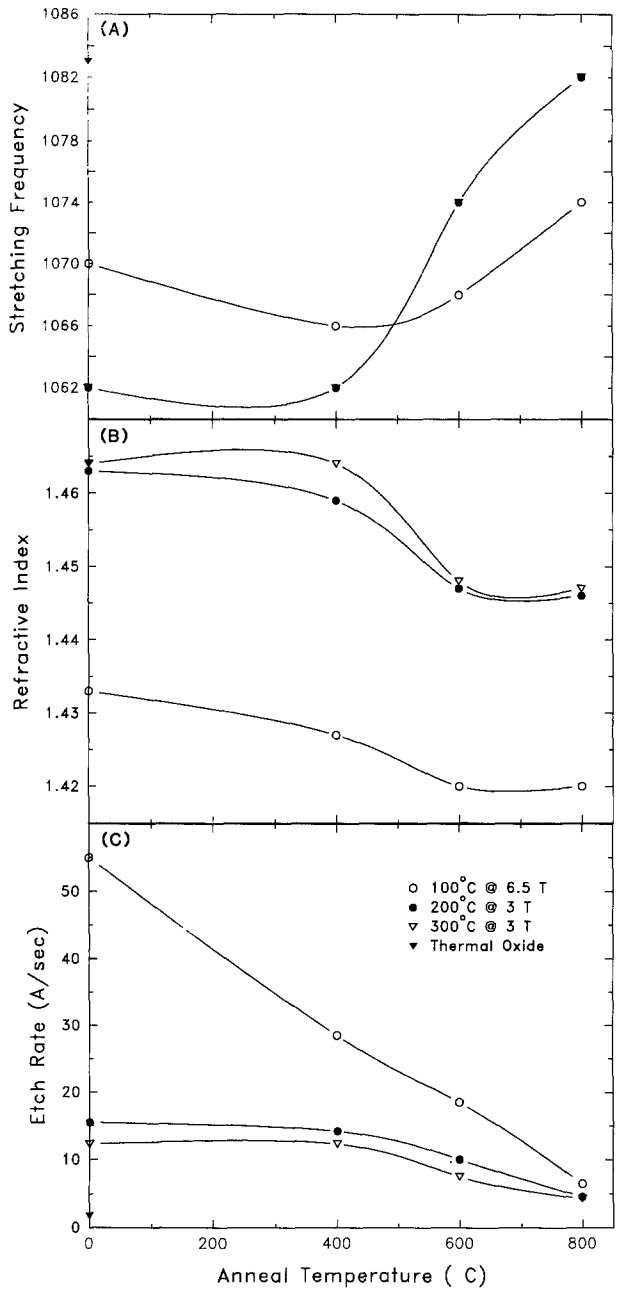

Fig. 3. The effect of annealing on a) Si-O stretching frequency, b) refractive index, and c) P-etch rate.

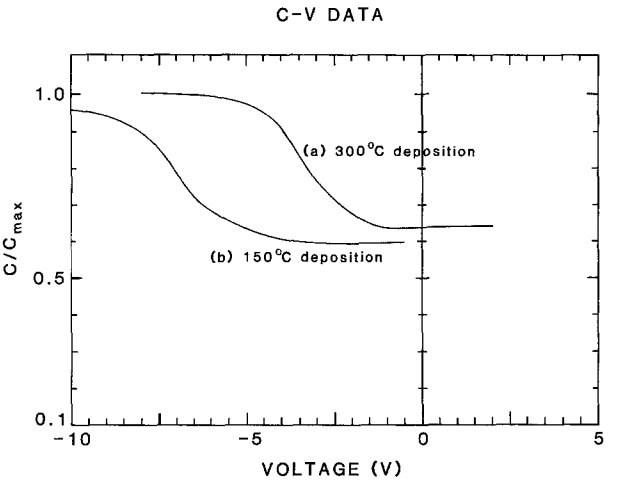

Fig. 4. 1 MHz capacitance-voltage data. (a) 300°C, 3 Torr, 8 min deposition, d_{ox} = 1437 Å, (b) 150°C, 4 Torr, 15 min deposition, d_{ox} = 1409 Å.

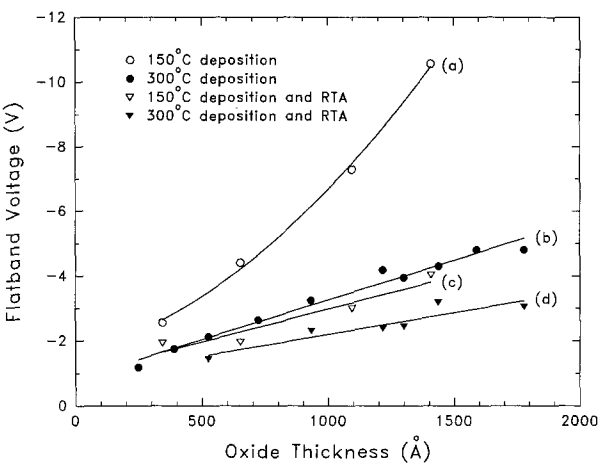

Fig. 5. Flatband voltage as a function of oxide thickness. (a) 300°C deposition, (b) 300°C samples after 650°C, 15 s RTA. (c) 150°C deposition, (d) 150°C samples after 650°C, 15 s RTA.

tion. Oxides deposited by CVD techniques are also susceptible to a distributed charge density. Under a constant reaction rate, or deposition rate, a uniform charge distribution is predicted, which will result in a quadratic increase in flatband voltage with oxide thickness. Samples prepared for determining the location of oxide charge were deposited at both 150 and 300°C. A constant deposition rate was confirmed by post-growth ellipsometric thickness measurements. A plot of V_{FB} as a function of oxide thickness is shown in Fig. 5. For samples deposited at 300°C, a linear dependence on thickness is evident (curve b), allowing us to conclude that the majority of the observed charge is located at the semiconductor-insulator interface. After these samples were subjected to a 650°C, 15 s anneal in nitrogen they showed a significant reduction in charge density (curve d). To determine whether the reduction in charge density results from changes in the density of fixed or mobile charges, stress bias measurements were performed. To rule out the possibility that the change in V_{FB} is a result of sodium contamination, unannealed samples (Fig. 6, curve a) were stressed with negative gate bias at elevated temperature. If the observed change in charge density was a result of Na^+ movement from the semiconductor-insulator interface to the metal-insulator interface, a large change in V_{FB} would be expected. The flatband voltage showed small shifts to the right (curve b), an indication of a low level of Na^+ contamination. By measuring the change in V_{FB} caused by positive stress fields at vari-

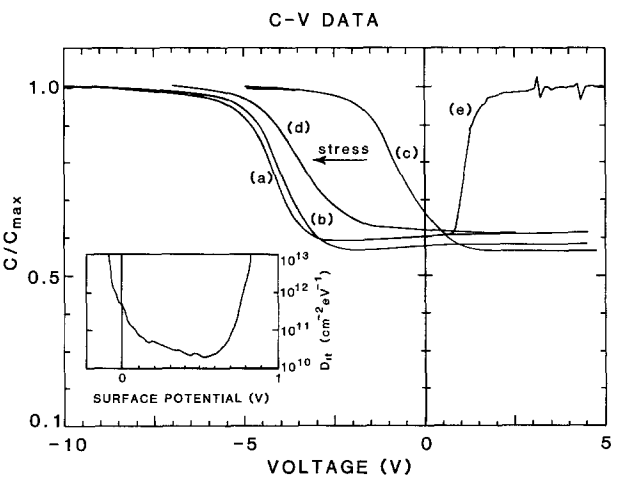

Fig. 6. Capacitance-voltage data for sample deposited at 300°C. (a) deposited, (b) after stress, (c) 800°C, 5 s RTA, (d) annealed sample after stress, (e) quasi-static data for annealed sample. Insert is D_{it} calculation using the high and low frequency data of (c) and (e).

ous temperatures, Na^+ levels below 1.2×10^{11} cm^{-2} were determined. Some devices were subjected to Triangular Voltage Sweep (TVS) measurements at 200°C (21). The stated levels of mobile ions were confirmed by integrating the I-V response, after subtracting the displacement current. The majority of sodium detected in our films appears to be introduced during metallization. When annealed samples (curve c) were stressed at elevated temperatures with negative bias, the flatband voltage shifted to the left (curve d)—the opposite direction expected from simple Na^+ contamination. A negative bias will hold the Na^+ at the metal-insulator interface during the stress, permitting the investigation of oxide trapping instabilities.

V_{FB} for samples deposited at 150°C shows a strong quadratic dependence on thickness (Fig. 5, curve a), implying the incorporation of a uniformly distributed charge during film deposition. After a 650°C, 15 s anneal in nitrogen, a more linear dependence is evident (curve c). The 150°C oxide had similar behavior in TVS and BTS measurements as the 300°C films.

To further investigate the effects of RTA treatment on oxide charge, wafers were prepared with 1000 Å oxides deposited at 150 and 300°C. The wafers were cleaved into several pieces after deposition. Samples were annealed in forming gas (3% H_2, 97% N_2) or nitrogen at 600°C for 30 s. Fixed-charge density showed no dependence on gas for this set of conditions and nitrogen was used during all other anneals. Fixed-charge densities are shown as a function of anneal time and temperature in Fig. 7. The minimum level of fixed charge obtainable appears to be a stronger function of anneal temperature than anneal time: the higher the anneal temperature, the lower the minimum fixed charge density. The response of our oxides to rapid thermal annealing is consistent with an interface-reaction-rate-limited process, and is not limited by the transport of hydrogen to the interface (23). Small amounts of hydrogen could exist in the bulk of the deposited film. This presumption is supported by two facts; silanol detected by FTIR measurements, and the independence of charge density with respect to anneal ambient.

High- and low-frequency C-V curves are shown in Fig. 6, curves c and e, with the corresponding interface-state density (D_{it}) calculated by the method of Castagne and Vapaille (24). D_{it} as low as 2×10^{10} $cm^{-2}eV^{-1}$ at midgap and Q_f as low as 8×10^{10} cm^{-2} are obtained after an 800°C, 5 s anneal. Thermal oxides, grown at 1150°C, exposed to the same metallization and contact anneal had Q_f of 5×10^{10} cm^{-2} and D_{it} below 2×10^{10} $cm^{-2}eV^{-1}$. Rapid thermal annealing is effective in removing interface fixed charge and interface traps for 150 and 300°C films. With annealing, unbound Si is tied to available hydrogen, resulting in low fixed-charge and interface-state densities. Annealing also appears to remove the high level of distributed fixed charge found in 150°C films.

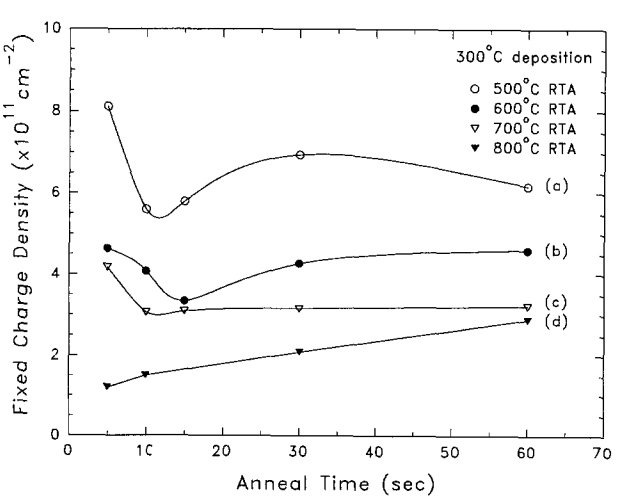

Fig. 7. Fixed charge density as a function of anneal time, for samples deposited at 300° (a) 500°, (b) 600°, (c) 700°, and (d) 800°C anneals.

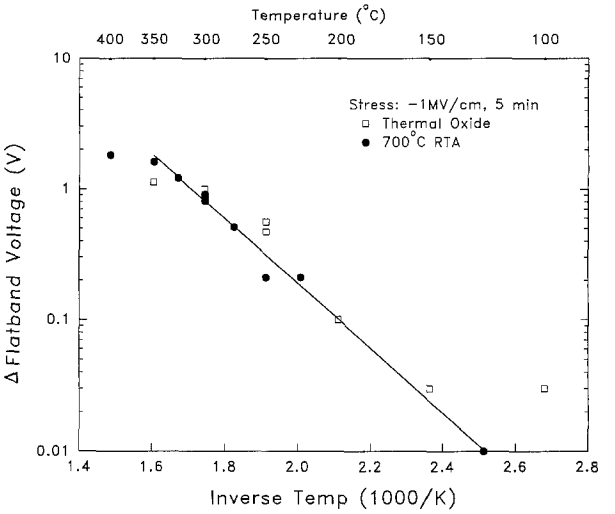

Fig. 8. Change in flatband voltage as a function of stress temperature. The sample was deposited at 300°C and annealed at 700°C for 5 s. The stress period was 5 min and the stress field was +1 MV/cm.

To investigate oxide trapping instabilities, annealed samples were subjected to bias stressing. For negative-field, room-temperature stress, little or no charge trapping was observed. Field strengths up to 7×10^6 V/cm could be applied before destructive breakdown occurred. For positive-field, room-temperature stress, trapping is observed above 6×10^6 V/cm. Trapping at these field levels does not constitute abnormal behavior (25). Negative bias stressing was further investigated as a function of stress temperature, field strength, and time. Figure 8 displays the change in flatband voltage as a result of varying stress temperature with constant field (−1 MV/cm) and constant stress time (5 min). The oxide was deposited at 300°C and annealed at 700°C for 5 s. Below 350°C the change in flatband voltage plotted against inverse temperature approximates a straight line, a least squares fit gives an activation energy of 0.44 eV. Above 350°C the flatband voltage saturates (after a relatively short time) within the 5 min period of the experiment. Thermal oxide subjected to the same stress resulted in similar flatband voltage shifts. Figure 9 shows results of varying stress period with constant field (−1 MV/cm), and constant temperature (250°C). The oxide was deposited at 300°C and annealed at 800°C for 5 s. For the fixed field and temperature of this experiment the flatband voltage begins to saturate after a 10 min stress period. The linear region (0-5 min) of the log plot reveals a $t^{0.28}$ dependence. Thermal oxide subjected to the same stress resulted in flatband voltage shifts an order of magni-

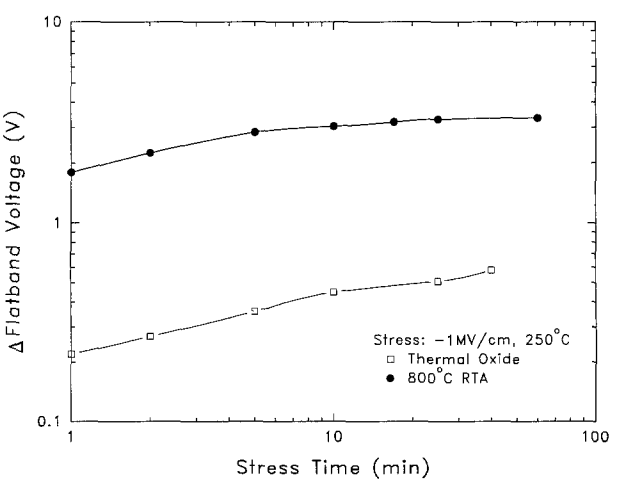

Fig. 9. Change in flatband voltage as a function of stress period. The sample was deposited at 300°C and annealed at 800°C for 5 s. The stress temperature was 250°C and stress field was 1 MV/cm.

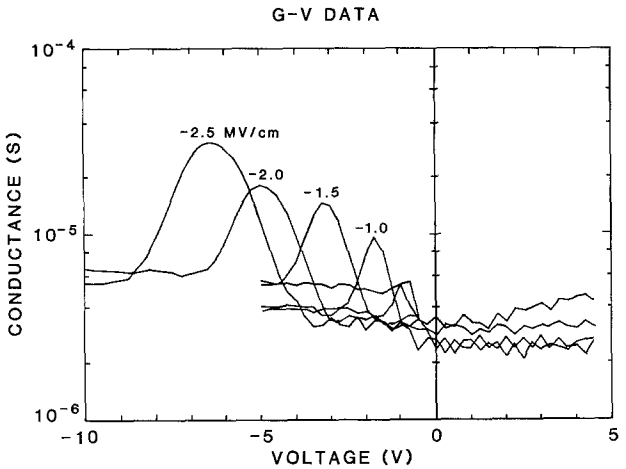

Fig. 10. Conductance-voltage data as a function of stress field. The sample was deposited at 300°C and annealed at 800°C for 5 s. The stress temperature was 200°C and stress time was 5 min.

tude lower. In Fig. 10 the conductance-voltage response of the same sample is shown as a function of stress field. The stress temperature was 200°C and the stress period was 5 min. The position of the peak corresponds to the amount of fixed charge, while the magnitude of the peak is related to the interface-state density. Both exhibit a pronounced increase with stress. Data from this experiment resulted in an $E^{1.8}$ dependence. The flatband voltage shift for our CVD oxides can be described by the equation

$$\Delta V_{FB} \propto E^{1.5} t^{0.27} e^{-0.44/kT} \quad [4]$$

Similar relationships are routinely observed for thermal oxides (26). The magnitude of the shift is also dependent on the post-deposition anneal of the sample. For identical stress conditions (−1 MV/cm, 5 min, 250°C), the sample of Fig. 6, before anneal, does not show a significant build-up of positive charge, the sample of Fig. 8, annealed at 700°C, shows a 0.2 V shift, and the sample of Fig. 9, annealed at 800°C, shows a 2.0 V shift. For thermal oxides, slow-trapping is more pronounced for samples with initially higher densities of fixed charge and interface states. One model describing slow trapping instability is structural rearrangement at the Si/SiO_2 interface. An oxygen atom bridging two Si atoms is displaced by stress, resulting in Si dangling bond states and a positively-charged oxygen center. In RTA-treated oxides the instabilities can be aggravated by strain induced at the Si/SiO_2 interface (27). The shift in flatband voltage with BTS cycle has also been correlated with the dissociation of the relatively weak Si-H bond (28). After stressing, hydrogen is removed from these sites, increasing both the fixed-charge and interface-state density. A combination of these effects explains the response of our oxides to negative BTS measurements.

Conclusions

The film microstructure of silicon dioxide deposited by low-temperature, low-pressure CVD on silicon has been studied by infrared spectroscopy, ellipsometry, P-etch rates, and C-V techniques. Films deposited at 100°C were found to have markedly different characteristics from films deposited at 200 and 300°C. The lower-temperature films were characterized by water and silanol groups incorporated in the films, along with decreased density, increased porosity, and oxygen deficiencies. The water/silanol content of 100°C films is reduced from 6.6%/6.3% to about 1.6% for both after annealing at 600°C for 10 s. Ellipsometry shows the refractive index decreased from 1.46 to 1.45 for films deposited T = 300°C after annealing at 600°C or greater while, for films deposited at T = 100°C, the refractive index decreased from 1.43 to 1.42 for the same annealing conditions. Films deposited at 100°C showed a densification of 11% after a 10 s, 800°C anneal while films deposited at higher temperatures densified by only 3%. The film structure was shown to improve with annealing. Fixed-charge densities of 8×10^{10} cm^{-2} and interface-state densities below 2×10^{10} cm^{-2} eV^{-1} are obtained after rapid thermal annealing. The slow-trapping instability of annealed samples is observed with negative BTS measurements. The trapping behavior could be modelled in a form identical to trapping in thermal oxide MOS devices.

In this paper we have demonstrated the ability to deposit high quality SiO_2 layers on silicon substrates at temperatures below 300°C. After rapid thermal annealing, resistivity, breakdown strength, fixed-charge, and interface-state densities are equivalent to or better than values found in oxides deposited at much higher temperatures. The possible applications of this technology vary from passivation to the more demanding role of a gate insulator. Low-temperature SiO_2 deposited at 100°C has been shown to be a suitable passivating layer for organic/inorganic diodes (14). A deposition temperature of 300°C would be appropriate for structures requiring lower interface-state densities and higher breakdown strengths, such as insulated gate devices. The consistent deposition rate and high uniformity of this method also suggest its potential success in thin oxide applications.

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Surface Modification of Base Materials for TEOS/O_3 Atmospheric Pressure Chemical Vapor Deposition

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ABSTRACT

Atmospheric pressure tetraethyloxysilicane (TEOS)/O_3 chemically vapor deposited provides excellent step coverage for submicron device structures; however, the properties of the deposited films depend on the surface characteristics of the base materials being used. To illustrate this dependence, the deposition rate of nondoped silicon dioxide obtained on a thermal oxide surface is significantly lower than the deposition rate obtained on a bare silicon surface. A new method to eliminate this base material dependence involving plasma treatment has been investigated. The optimum treatment consists of exposing the base materials to a nitrogen plasma for 1 min while maintaining the base materials at 250°C. Films deposited on thermal oxide base materials which have first been treated by this new method were found to have the same deposition rate, aqueous HF etch rate, and surface morphology as those films deposited on untreated bare silicon. In addition to a nitrogen plasma, oxygen and argon plasmas were studied and found to produce similar results when the base material temperature was raised to 350°C. The elimination of base material dependence through the use of this new plasma treatment technique has resulted in higher integrity TEOS/O_3 oxides and has also expanded the range of applications for this unique planarizing technology for very large scale integrated device fabrication.

Tetraethoxysilane (TEOS) is increasingly being used as a silicon (oxide) source material for atmospheric pressure, low pressure, and plasma techniques of chemical vapor deposition because it provides better step coverage and meets tighter safety requirements. In particular, atmospheric pressure TEOS/O_3 CVD is a promising technology for advanced very large scale integrated (VLSI) device fabrication because it offers superior step coverage and improved safety of TEOS along with low deposition temperatures (1-3).

TEOS/O_3 atmospheric pressure chemical vapor deposition (APCVD) provides excellent step coverage due to the surface-limited nature of its reaction kinetics, but because of this surface-limited nature, the nature of the surface being deposited on represents an important factor. When a TEOS/O_3 film is deposited on polysilicon, aluminum, or borophosphosilicate glass (BPSG) using 5% ozone in oxygen a high-quality film is obtained; but when the same chemistry is used to deposit a TEOS/O_3 film on thermal oxide, the surface morphology and film quality are poor. This phenomenon has been correlated to the hydrophobic/hydrophilic nature of the substrate material (4). The thermal oxide surface is hydrophilic and has a contact angle of 10°. The bare silicon surface is hydrophobic and has a contact angle of 50°. This base material dependence phenomenon has been described previously in conjunction with another method for elimination base material dependence which uses a two-step deposition sequence (4).

A new method for eliminating base material dependence which incorporates the use of a plasma treatment is presented in this paper. Exposure time, substrate temperature, and gas ambient were optimized in an anode-coupled plasma system in order to obtain superior quality silicon dioxide films on thermal oxide base materials.

Experimental

The apparatus and procedure for TEOS/O_3 silicon dioxide deposition have been described previously (3). The TEOS/N_2 flow rate was 2 slpm. The plasma treatment system is a conventional parallel plate, anode-coupled system which contains a heater with a 200 mm diam anode capable of heating a silicon substrate to 450°C. In this paper, the process temperature during plasma treatment refers to the anode temperature which is assumed to be equal to the substrate temperature. One hundred nanometer thermal oxide films on 150 mm silicon wafers were used in this study. The thermal oxide films were formed at 1000°C in dry oxygen. The plasma treatment was applied only to the thermal oxide samples. The bare silicon substrates were used as reference wafers and did not receive a plasma treatment. Following the plasma treatment of the thermal oxide wafers, nondoped silicate glass (NSG) films were then deposited on both types of substrates. The deposition rate, aqueous HF etch rate, and surface morphology of the films deposited on the plasma-treated thermal oxide wafers were compared with those deposited on the bare silicon material.

The plasma treatment conditions are shown in Table I. The wet etching was done using a 2.4% aqueous HF solution at 24°C. As a reference, the thermal oxide etch rate under these conditions was 17.9 nm/min.

Results and Discussion

In Fig. 1, the effects of plasma exposure time on the deposition rate were studied. For this series of tests the substrate temperature was held constant at 350°C during plasma treatment. Following plasma treatment, NSG films were deposited at 400°C using 4.2% ozone. In the figure, the deposition rate ratio is defined as the ratio of the deposition rate obtained on the plasma-treated thermal oxide to that obtained on bare silicon without the plasma treatment. When no plasma treatment is applied, the ratio is very low, 0.48. When a 1 min plasma treatment was applied, the ratio increases to 0.96 and remained approximately 1.0 when longer exposure times were used.

Figure 2 shows the dependence of etch rate on plasma exposure time using the same conditions used to generate

Table I. Standard conditions of plasma treatment.

RF frequency	13.56 MHz
Power	200 W
Pressure	1 Torr
Gas and Flow Rate	Nitrogen, 400 sccm
Duration	1 min