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$HfSiO_4$ Dielectric Layers Deposited by ALD Using $HfCl_4$ and $NH_2(CH_2)_3Si(OC_2H_5)_3$ Precursors

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The physical and electrical properties of $HfSiO_4$ dielectric layers deposited by atomic layer deposition (ALD) are reported. The precursor chemistries used for deposition were $HfCl_4/H_2O$ for HfO_2 and $NH_2(CH_2)_3Si(OC_2H_5)_3/O_3$ for SiO_2. Two processes with $HfCl_4:NH_2(CH_2)_3Si(OC_2H_5)_3$ precursor pulse ratios of 5:1 (''HfO_2-rich'') and 1:1 (''SiO_2-rich'') are investigated. Measurements with X-ray photoelectron spectroscopy and channeling Rutherford backscattering spectrometry show that these processes result in layers with Hf/(Hf + Si) ratios of 0.56 and 0.34-0.37, respectively. X-ray diffraction measurements showed formation of a HfO_2 cubic phase in HfO_2-rich layers starting at 850°C. In SiO_2-rich layers, no crystallization was detected up to 1100°C. Metal oxide semiconductor (MOS) capacitors with polysilicon electrodes were used for electrical characterization. The *k*-value of the SiO_2-rich layers was found to be 4.8-5.4 and that of the HfO_2-rich layers 12.5-15.1, both with an experimental error of 10%. The leakage currents of both types of layers were comparable to SiO_2 reference data and increased with polysilicon activation anneal. A high-resolution transmission electron microscopy study revealed phase segregation in thick SiO_2-rich layers. In HfO_2-rich layers, the phase segregation was less clear, but upon annealing, composition variations at the interfaces were detected. Given the experimental errors, no impact of phase segregation on the *k*-values of both types of layers could be detected. It is concluded that postdeposition annealing of $HfSiO_4$ layers for application as gate dielectrics applications in advanced complementary MOS technologies is essential to optimize stoichiometry and reduce leakage currents.
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For many years, silicon dioxide (SiO_2) has been the gate dielectric in complementary metal-oxide silicon (CMOS) technologies. Scaling of the lateral dimensions of MOS-field-effect transistors (MOSFETs) in CMOS technologies has led to scaling of the gate dielectric thickness to values below 2 nm. When the gate length of MOSFETs is scaled down, short channel effects (SCEs) become dominant. Therefore, scaling of the gate dielectric thickness is required to maintain control of the gate voltage over the inversion charge at the Si/SiO_2 interface.[1] However, the SiO_2 thickness reduction results in high leakage currents and degraded reliability. Incorporating nitrogen into SiO_2 increases the relative permittivity (*k*-value) from 3.9 for SiO_2 to about 5-7 for nitrided SiO_2, *i.e.*, SiON. This means that at the same equivalent oxide thickness (EOT), the leakage current through SiON layers is much smaller than through SiO_2 layers.[2]

It is expected, however, that even SiON gate dielectrics will not meet many requirements for aggressively scaled CMOS. Therefore, dielectric layers with a high *k*-value, *i.e.*, high-*k* dielectrics, are gaining increasing attention for application as a gate dielectric in advanced CMOS technologies. Several alternative gate dielectric materials such as Y_2O_3,[3] Ta_2O_5,[4] ZrO_2, and HfO_2 have been investigated.[5-7] Also, rare-earth metal oxides like La_2O_3, PrO_2, and CeO_2 have received considerable attention.[8-10] However, finding a replacement dielectric for SiO_2, which exhibits a sufficiently high *k*-value, large band offsets, thermodynamic stability, high crystallization temperature, low charge trapping properties, and good mobility properties appears challenging.[11]

Hafnium-based dielectrics are expected to be thermodynamically stable on Si. HfO_2 has a *k*-value in the range of 18-22 and a bandgap of about 6 eV, dependent on the deposition technique and applied postdeposition anneals (PDAs).[12] In order to improve the relatively low crystallization temperature of around 600°C of pure HfO_2, alloying HfO_2 with Al_2O_3 and SiO_2 has been proposed.[13-15] The advantage of alloying HfO_2 with SiO_2 lies in the improved thermodynamic stability of the dielectric layer, the increased conduction- and valence-band offsets, and the higher carrier mobility in the inversion layer of MOSFETs.[16-19] Recently, promising MOSFET properties have also been obtained with HfSiON gate dielectrics. In particular, it was shown that adding nitrogen to the silicate layer considerably reduced the charge trapping properties and improved the threshold voltage stability.[20,21]

Both the chemistry and the deposition technique are crucial parameters for obtaining the desired layer composition of ternary high-κ gate dielectrics. An advanced technique to deposit high-κ dielectrics is atomic layer chemical vapor deposition (ALCVD™)[d] or atomic layer deposition (ALD).[1] In this technique, the reactants are pulsed in separate sequences into the reaction chamber and the saturating surface reactions are self-limited. Because of this, the surface preparation is of utmost importance for the quality of ALD layers. Electrical and physical properties of $ZrSiO_4$ layers deposited by ALD were reported elsewhere.[22,23] In the present work, $HfSiO_4$ layers deposited by ALD are investigated. The surface preparation prior to $HfSiO_4$ deposition was changed by one or more start pulses. This procedure results in different starting surfaces, which may affect the properties of the $HfSiO_4$ layers. Reference HfO_2 layers were deposited using $HfCl_4/H_2O$ chemistry on a 1 nm SiO_2 layer. In the following sections, the details of the layer deposition process and experimental results from physical and electrical analysis are presented and discussed.

Experimental

Hafnium-silicate ($HfSiO_4$) layers were deposited with various growth starting conditions, both on 1-3 Ω cm p-type or 1-8 Ω cm n-type 4 in. single-crystal Si(100) substrates in a flow-type F-450 ALCVD reactor located in a laboratory environment (clean room class 100000) at ASM Microchemistry, Ltd., Finland. The deposition temperature was 300°C. Precursors used were trimethylaluminum $Al(CH_3)_3$ (TMA), $HfCl_4$, and 3-aminopropyltriethoxy si-

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[d] ALCVD™ is a trademark of ASM International. Inc.

lane $NH_2(CH_2)_3Si(OC_2H_5)_3$ (APTES). Ozone and water were chosen as the oxygen sources. The composition of the layers was varied by changing the $HfCl_4$:APTES pulse sequence ratio. Two different processes were investigated

$$N \times (HfCl_4 + H_2O + APTES + O_3) \quad (SiO_2\text{-rich}) \qquad [1]$$

$$N \times [(HfCl_4 + H_2O) \times 5 + (APTES + O_3)] \quad (HfO_2\text{-rich}) \qquad [2]$$

where N is the number of cycles. Here, a precursor pulse followed by an O_3- or H_2O pulse is referred to as one (pulse/purge) sequence. The number of cycles N of the SiO_2-rich layers was 32, 85, or 170, and for HfO_2-rich layers N was 3, 6, 11, or 20. The number of sequences, defined as $N \times 2$ (SiO_2-rich) and $N \times 6$ (HfO_2-rich), was hence 64, 170, and 340 for the SiO_2-rich layers, and 18, 36, 66, and 120 for the HfO_2-rich layers, respectively. Prior to deposition, a 5 min 0.5% HF dip was followed by a 10 min O_3 start pulse, or ten cycles of TMA/H_2O. The latter results in a 0.8-0.9 nm thick Al_2O_3 film. Reference HfO_2 layers with a thickness of 40 Å were deposited on 8 in. p-type Si(100) wafers with a thin (~1 nm) oxide layer in a Pulsar 2000 reactor (ASM Belgium).

Thickness measurements were done using a UV-visible spectroscopic reflectometer NanoSpec AFT/4000. The standard deviation for the thicknesses of thin $HfSiO_4$ layers was around 7% and for the HfO_2 layers smaller than 3%. For thicker layers ($t_{ox} > 20$ nm), the standard deviation was in some cases 10-15%, most likely due to CVD-like deposition as a result of inhomogeneous precursor flows inside the chamber.[22] X-ray diffraction (XRD) measurements were done in the same system. Diffraction patterns were determined after heating the samples for 30 min at a given temperature. The composition of the layers was determined by X-ray photoelectron spectroscopy (XPS, Quantum 2000 from Phi) using Al Kα radiation with a spot size of 100 μm^2. For comparison with the XPS results, channeling Rutherford backscattering spectrometry (RBS) measurements were taken from relatively thick (24-31 nm) layers which had received various PDAs. A high-resolution transmission electron microscopy (HR-TEM, TECNAI F30ST) study was done to study the $HfSiO_4$ dielectrics and the $HfSiO_4$/silicon and $HfSiO_4$/polysilicon interfaces as a function of annealing temperature.

MOS capacitors were fabricated by depositing 100 nm *in situ* p-doped low-pressure chemical vapor deposited (LPCVD) polysilicon and subsequent wet etching in HF/HNO_3. The deposition temperature of the polysilicon layer was 590°C. Activation of the polysilicon and PDAs were done in a Mattson SHS1000 rapid thermal anneal (RTA) system with a ramp rate of 50°C/s in flowing nitrogen. A 30 ft H_2/N_2 forming gas anneal (FGA) at 420°C was done after patterning and polysilicon activation. The capacitor areas varied between 20×20 and 200×200 μm^2. Capacitance-voltage (C-V) measurements were done at 10 and 100 kHz using a HP4284A impedance analyzer. For current-voltage (I-V) measurements, an HP4155 analyzer was used. All electrical measurements were done on a four-point probe station at constant temperature and under constant N_2 flow.

Results

Thickness and growth rates.—Figure 1 and 2 show the thickness of the SiO_2-rich and HfO_2-rich $HfSiO_4$ layers as a function of the total number of ALD pulse/purge sequences and for different starting conditions. Here the thickness was determined with an ellipsometer (NanoSpec AFT/4000). The average growth rate per single pulse/purge sequence was determined from the slope of the linear fit. As-determined average growth rates of SiO_2-rich mixed layers range from 0.84 Å/sequence (on Al_2O_3) to 0.82 Å/sequence (with O_3 start pulse). For HfO_2-rich layers, growth rates of 2.25 Å/sequence (on Al_2O_3) and 2.1 Å/sequence (with O_3 start pulse) were found. Estimated errors in the growth rates are around 10%, considering nonuniformity of the layer thickness and inaccuracies due to composition variations. The ellipsometer thickness values were typically 2-20% higher than thickness values determined with HR-TEM. Therefore, the growth rates determined here are likely overestimated by the same percentage.

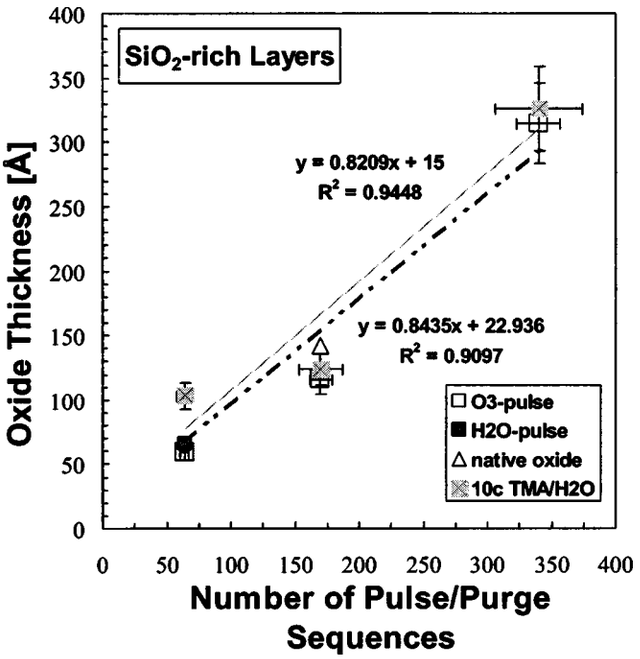

Figure 1. Thickness of SiO_2-rich silicate layers for various starting conditions. Average growth per pulse/purge sequence is 0.82-0.84 Å/pulse/purge sequence.

Composition measurements.—The composition of the layers, in particular the Hf/(Hf + Si) and the O/(Hf + Si) ratios, were deter-

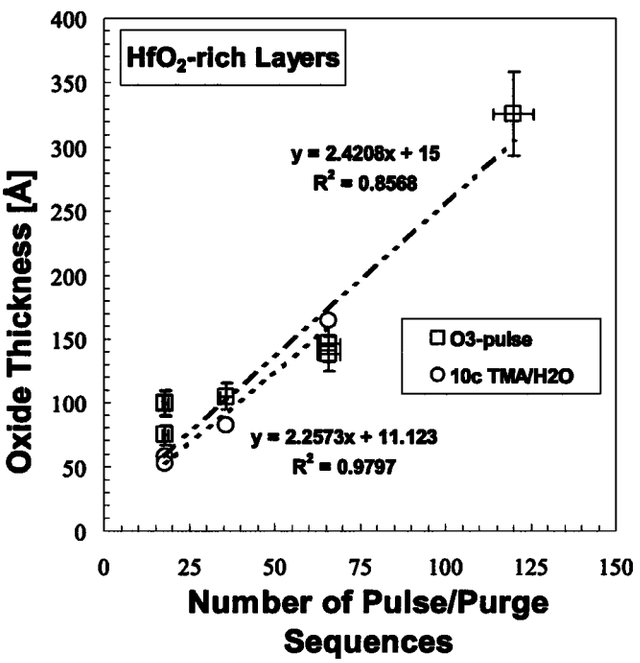

Figure 2. Thickness of HfO_2-rich silicate layers for various starting conditions. Average growth per pulse/purge sequence is 2.26-2.42 Å/pulse/purge sequence.

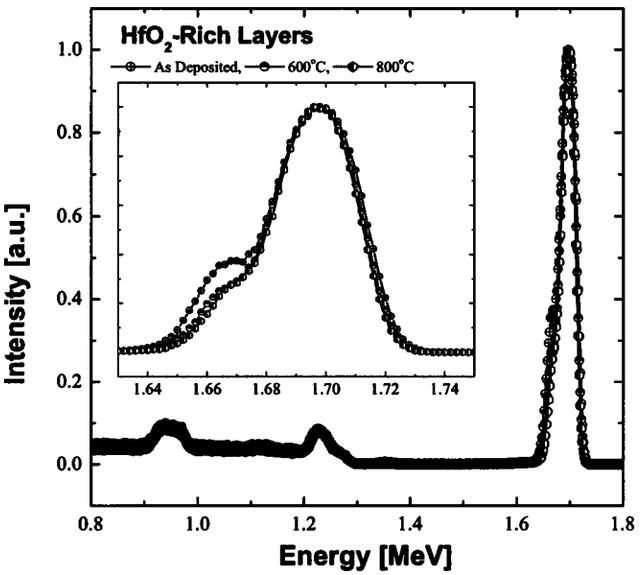

Figure 3. RBS measurements of HfO_2-rich silicate layers with various PDAs.

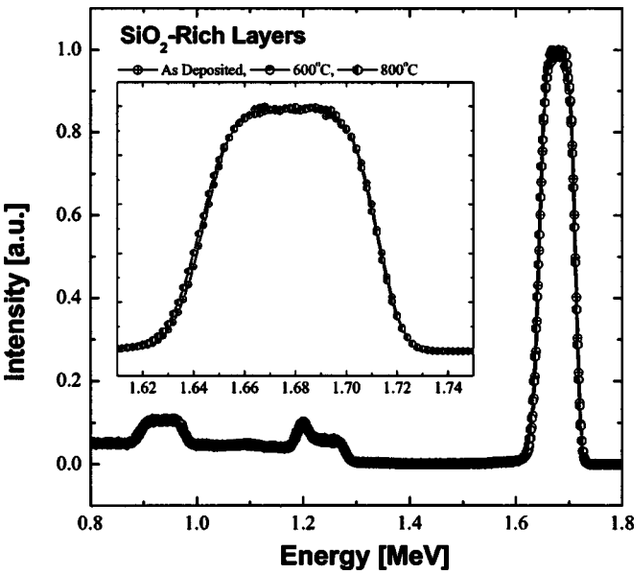

Figure 4. RBS measurements of SiO_2-rich silicate layers which received as-indicated PDAs.

mined with XPS and with RBS measurements. Figure 3 and 4 show RBS spectra of two $HfSiO_4$ layers (HfO_2-rich and SiO_2-rich, respectively). The thicknesses of these two layers were 241 ± 17 and 315 ± 41 Å, respectively. Both layers were measured before and after four different PDAs in the range 600-1000°C. The measurements reveal that the Hf/(Hf + Si) ratio is not constant over the entire layer thickness and that this ratio changes as a function of the PDA temperature. In particular, the spectra show that as-deposited layers exhibit an initially HfO_2-rich lower interface, whereas after PDA it tends to become SiO_2-rich. Furthermore, simulations on these spectra indicate that after a PDA at 600°C or higher in O_2, the top layer becomes HfO_2-rich. Similar trends are observed for SiO_2-rich layers; however, here the variations become visible after PDA at 800°C or higher.

The RBS measurements were compared with XPS measurements for a 90° incident angle of the beam. The penetration depth at this angle is estimated to be 9 nm. In Table I a summary of both XPS and RBS composition data is given for as-deposited layers and for layers with different PDAs. As can be seen, for all PDA conditions good agreement is obtained between the XPS and RBS data.

As can be seen from Table I, both SiO_2-rich and HfO_2-rich as-deposited layers appear to be oxygen-rich, *i.e.*, the O/(Hf + Si) ratio is higher than two. The RBS measurements show a tendency toward more stoichiometric layers after annealing in the range of 600-800°C for 10 s in O_2. After a 600°C, 10 s anneal, O/(Hf + Si) = 2.08, and after a 800°C, 10 s anneal O/(Hf + Si) = 2.00 (RBS values for SiO_2-rich layers). The increase of the O/(Hf + Si) ratio to 2.26 after a 1000°C, 1 s PDA in O_2 might be due to reoxidation of the $HfSiO_4$/Si interface. The fact that XPS does not confirm this trend can be related to the depth resolution of about 9 nm, while the layer is 6-7 times as thick.

Crystallization and interfaces (XRD,HR-TEM).—In Fig. 5, XRD spectra of $HfSiO_4$ layers are shown. The HfO_2-rich layer was 11 cycles [11 × (5:1) ($HfCl_4/H_2O$:APTES/O_3)], t_{ox} = 16.2 nm, and the SiO_2-rich layer 32 cycles [32 × (1:1) ($HfCl_4/H_2O$:APTES/O_3)], t_{ox} = 10.1 nm, both on native oxide.

In the HfO_2-rich layer, the HfO_2-cubic phase is detected around 850°C. In the SiO_2-rich layer, no crystallization could be identified (with a detection limit of 1 mass %). The SiO_2-rich sample was measured up to three times and on different spots of the wafer and after stabilizing the temperature at 1100°C for 30 min, but no peak could be detected. As compared to a binary HfO_2 reference sample, the $HfSiO_4$ layers showed an improvement of the amorphous dielectric phase by more than 250°C. Clearly, this can be attributed to the presence of SiO_2 in the layers.

A series of HR-TEM photographs of $HfSiO_4$ layers are shown in Fig. 6. In the left column, the as-deposited layers are shown. In Fig. 6 (1) and (2), two HfO_2-rich layers are shown, and in Fig. 6 (3) and (4), two SiO_2-rich layers. In both cases, the layer was investigated immediately after polysilicon deposition and after annealing the polysilicon for 1 s at 1000°C. These photographs were taken at the

Table I. Summary of XPS and RBS composition data.

Pulse ratio		XPS		RBS	
$HfCl_4$:APTES	PDA	Hf/(Hf + Si)	O/(Hf + Si)	Hf/(Hf + Si)	O/(Hf + Si)
1:1	As-deposited	0.35	2.21	0.38	2.27
	600°C, 10 s O_2	0.37	2.27	0.40	2.08
	800°C, 10 s O_2	0.38	2.22	0.37	2.00
	1000°C, 0 s O_2	0.38	2.19	0.34	2.26
5:1	As-deposited	0.56	2.11	0.57	2.29
	600°C, 10 s O_2	0.58	2.19	0.50	2.20
	800°C, 10 s O_2	0.56	2.04	0.54	1.87
	1000°C, 0 s O_2	0.57	2.14	0.59	2.16

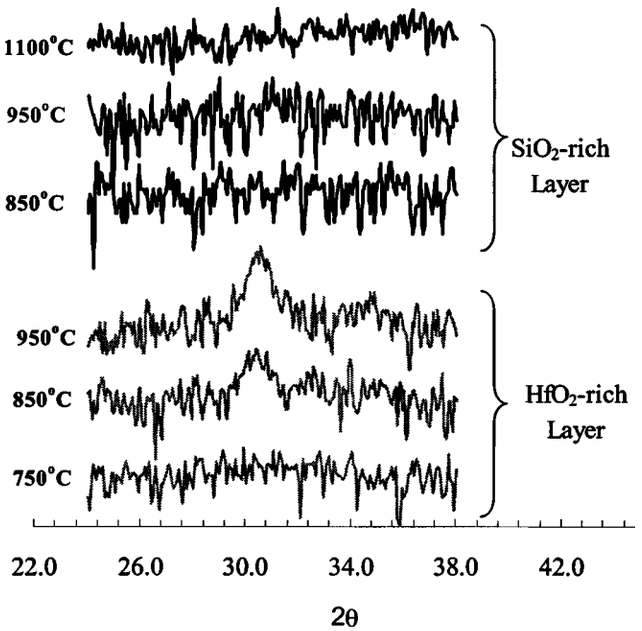

Figure 5. XRD results for HfO_2-rich and SiO_2-rich layers.

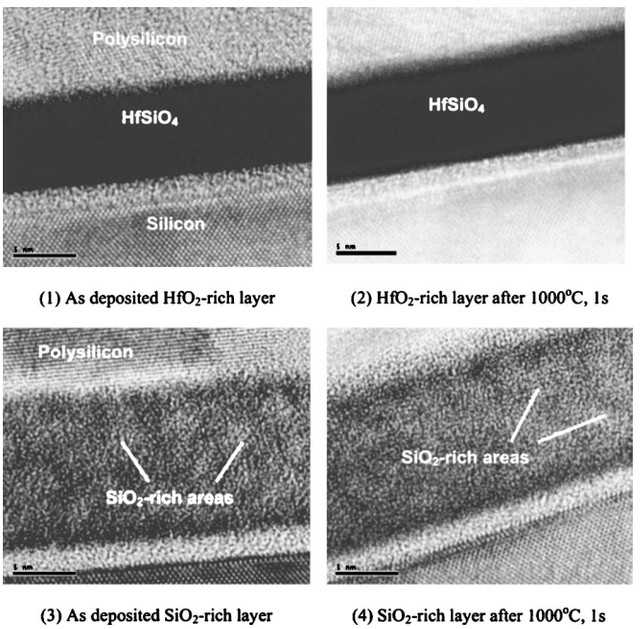

Figure 6. Series of HR-TEM photographs of $HfSiO_4$ dielectric layers with polysilicon electrodes: (1) HfO_2-rich layer (as deposited), t_{ox} = 94 Å, t_{il} = 19 Å; (2) HfO_2-rich layer (1000°C RTA), t_{ox} = 107 Å, t_{il} = 14 Å; (3) SiO_2-rich layer (as deposited), t_{ox} = 143 Å, t_{il} = 17 Å; and (4) SiO_2-rich layer (1000°C RTA), t_{ox} = 161 Å, t_{il} = 15 Å.

middle of large-area capacitors ($1000 \times 1000\ \mu m^2$), and therefore it is assumed that lateral oxidation effects play no role. A clearly observed difference between the HfO_2-rich and the SiO_2-rich layer is the appearance of areas with lighter contrast in the latter. These seem to become larger after anneal. In a number of previous publications, several authors have discussed the phase segregation in $HfSiO_4$ and $ZrSiO_4$ dielectric layers.[24-26] The dielectric constant is not only determined by the SiO_2/HfO_2 ratio, but also by the shape and the size of phases inside the dielectric.[27,28] The observed phase segregation might therefore have consequences for the effective dielectric constant of the layers.

A detailed overview of the changes in the thickness of the individual layers is presented in Table II. A number of observations were made. First of all, it is found that the overall thickness, *i.e.*, the dielectric thickness including both interface layers, increases after polysilicon anneal. Second, the lower interface of HfO_2-rich layers grown with an O_3 start pulse or on native oxide tends to become more diffuse after anneal. That is, on top of a bright, SiO_2-rich interface layer, a grayish layer with a slightly brighter contrast than the bulk layer is observed. Furthermore, considerable changes at the polysilicon/$HfSiO_4$ interface were observed. An increase of the interface layer between the dielectric and the polysilicon after anneal is observed for all deposition starting conditions. For HfO_2-rich layers, this increase is typically on the order of 3-6 Å. With the exception of layers grown with a H_2O start pulse, the dielectric/polysilicon interface layer is less distinct for as-deposited SiO_2-rich layers as compared to HfO_2-rich layers. However, its thickness increases relatively more after polysilicon activation anneal than in the case of HfO_2-rich layers. After anneal, the thickness of this interface was found to be as large as 18 Å.

The differences between as-deposited and annealed layers suggest that the interface between (as-deposited) $HfSiO_4$ dielectrics and polysilicon are stable during the polysilicon deposition process itself (at 590°C), and that reactions take place during polysilicon activation temperatures at around 1000°C. Possibly, reactions already occur at lower temperature. A possible explanation for the interface variations might be that the excess O present in the layers diffuses toward the interfaces and oxidizes the polysilicon and the silicon substrate. It remains unclear how the phosphorous doping in the polysilicon affects the stability of the interface layer.

Electrical characterization.—Figure 7 shows a number of C-V measurements of a SiO_2-rich $HfSiO_4$ layer after various polysilicon

Table II. Comparison of HR-TEM thickness data with NanoSpec thickness data.

			NanoSpec	Thickness (TEM)[a]		IL (TEM)[b]	
Layer ID	Startpulse	Pulse ratio	As-deposited (Å)	As-deposited (Å)	1000°C (Å)	As-deposited (Å)	1000°C (Å)
B1_D02	Native oxide	5:1	62	48	51	9	8
B1_D11	H_2O pulse	5:1	159	94	107	19	14
B1_D18	Al_2O_3	5:1	52	47	39	17	16
B2_D04	O_3 pulse	1:1	59	49	60	14	12
B2_D06	H_2O pulse	1:1	66	75	80	12	11
B2_D07	Native oxide	1:1	142	143	161	17	15
B2_D10	Al_2O_3	1:1	103	78	81	11	14

[a] Total thickness of the dielectric, including top and bottom interface layers.
[b] Thickness of the bright bottom interface layer.

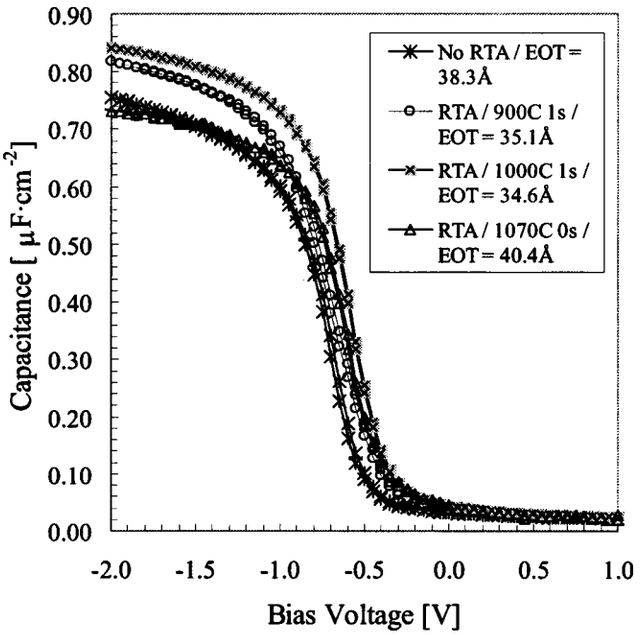

Figure 7. C-V characteristics of SiO_2-rich $HfSiO_4$ (64 cycles 1:1 with O_3 start pulse) for various polysilicon anneals (silicate layer is as-deposited). EOTs range from 38.3 (as-deposited) to 40.4 Å (1070°C spike anneal).

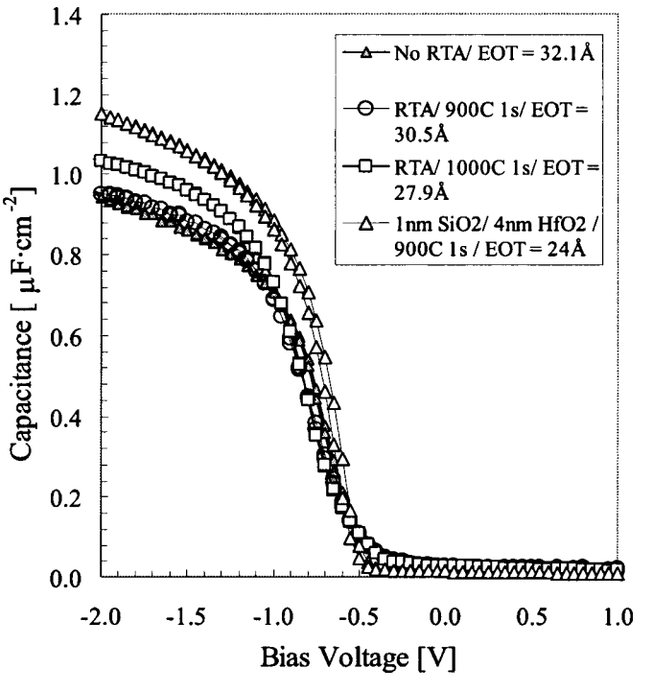

Figure 9. C-V measurements of HfO_2-rich layer on Al_2O_3 start surface, including reference HfO_2 with polysilicon after 900°C activation anneal.

activation anneals. These SiO_2-rich layers received no PDA prior to polysilicon deposition. The equivalent oxide thickness (EOT) of this layer varied between 38.3 (as-deposited) and 34.6 Å (1000°C, 1 s RTP). After a 1070°C, 0 s RTA step, the capacitor appears to break down; the observed increase of the EOT is most likely due to interface oxide growth. The EOT values were obtained using a MOS C-V simulation program, taking into account quantum-mechanical corrections and polysilicon depletion effects.[29] For the four shown measurements, the flatband voltage V_{FB} changed from −580 (as deposited), −554 (900°C), and −469 (1000°C), to −481 mV (1070°C). Assuming this shift is completely due to fixed charge Q_{fix} located at the interfaces, this corresponds to an increase from 3.5 to 5.8×10^{11} cm^{-2} in the range "as-deposited, 1000°C." The leakage currents of equally sized capacitors is shown in Fig. 8. In the range as-deposited to 1000°C RTA, the current density at $|V_{FB} - 1|$ in-

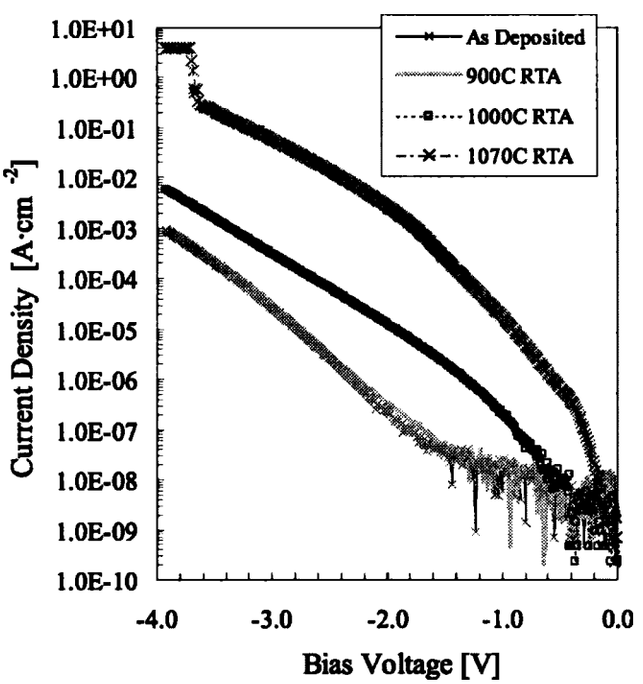

Figure 8. I-V characteristics of SiO_2-rich $HfSiO_4$ layers for various polysilicon anneals (same layer as in Fig. 7).

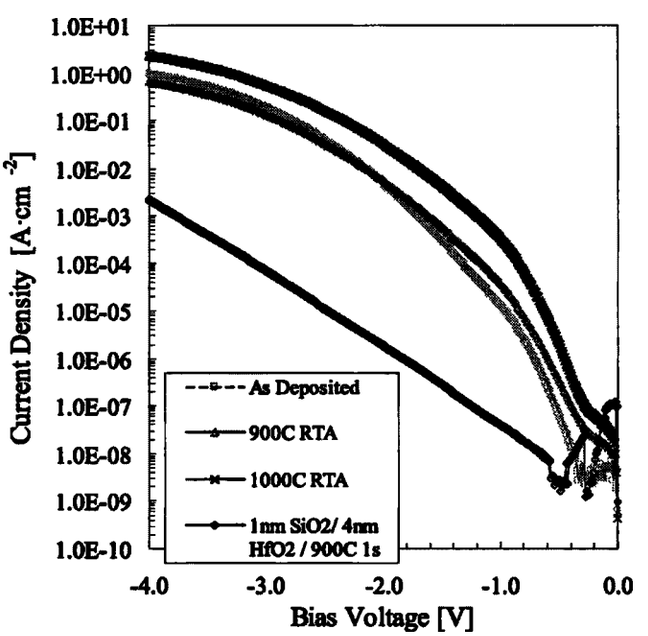

Figure 10. I-V measurements of HfO_2-rich $HfSiO_4$ layer on Al_2O_3 start surface, including reference data of 4 nm HfO_2.

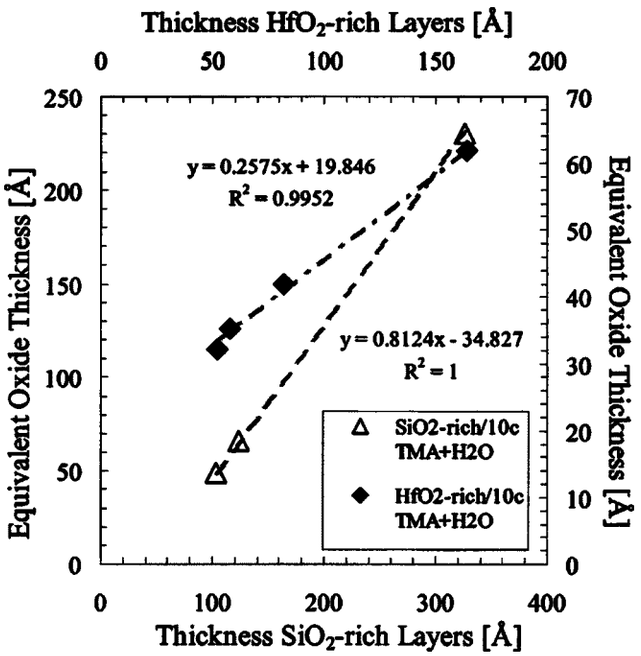

Figure 11. EOT of silicate layers *vs.* gate dielectric thickness. EOT *vs.* oxide thickness (NanoSpec data). The *k*-value for SiO_2-rich layers equals 4.8; for HfO_2-rich layers the *k*-value is 15.1.

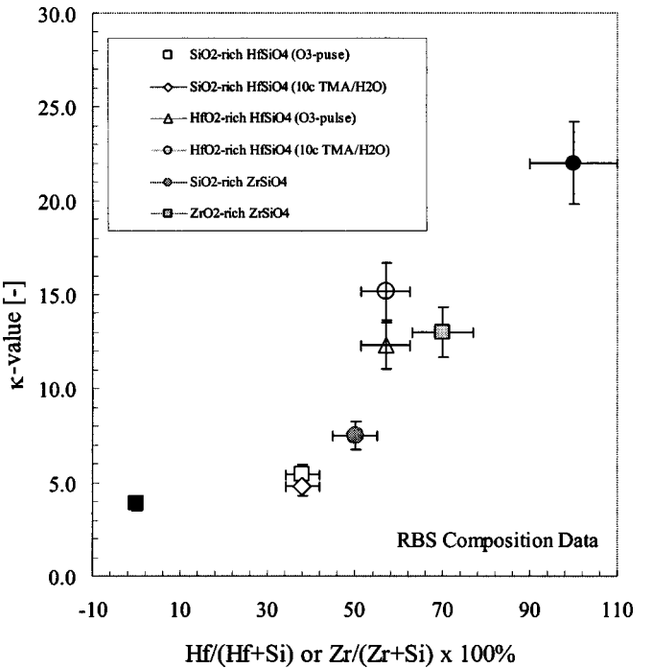

Figure 12. As-determined *k*-values of $HfSiO_4$ layers *vs.* Hf/(Hf + Si) ratio. Data of ALD $ZrSiO_4$ layers from previous work included.[23]

creases from 3.1×10^{-8} to 1.4×10^{-6} A cm^{-2}, *i.e.*, two orders of magnitude. After anneal at 1070°C, the current density increases another two orders of magnitude.

In Fig. 9 and 10, C-V- and I-V measurements of a 52 Å thick HfO_2-rich layer grown on Al_2O_3 are shown. Measurements of 1 nm SiO_2/4 nm HfO_2 with no PDA and the same polysilicon electrode are included as reference. The thinnest EOT of this HfO_2 layer was 27.9 Å after 1000°C, 1 s activation anneal and subsequent 420°C, 20 min N_2/H_2 anneal. The flatband voltage V_{FB} of this layer shifted from −582 to −666 mV (with increasing RTA temperature), *i.e.*, shifted by 336-260 mV from the ideal V_{FB}. The V_{FB} of the reference HfO_2 was shifted by 392 mV ($V_{FB} = -485$ mV). It was found that the V_{FB} of this HfO_2 layer could be shifted 100 mV toward the ideal value with a 600°C, 10 s PDA in O_2, without an increase in the EOT. Annealing a 75 Å thick HfO_2-rich mixed layer at higher temperature, *i.e.*, in the range 800-1000°C for 10 s in O_2, showed that the V_{FB}, with as-deposited polysilicon, could be improved from −603 mV (as-deposited) to −722 mV (1000°C, 1 s O_2), however, at the expense of a considerable increase in EOT. The hysteresis, measured at V_{FB}, in the layers was typically on the order of 5-15 mV for thin layers (52 Å HfO_2-rich on Al_2O_3) and up to 138 mV for thick layers (B2_D10, $t_{ox} = 103$ Å), with no clear trend difference between SiO_2-rich and HfO_2-rich layers. The EOT values of all investigated as-deposited $HfSiO_4$ layers without polysilicon activation varied between 38 and 230 Å for SiO_2-rich layers and between 32 and 164 Å for HfO_2-rich layers. After activation anneals, EOT values decreased typically by 5-15% of the as-deposited value, while the total dielectric thickness increased (see HR-TEM results, Table II).

The *k*-values of the layers were found using a linear fit of EOT *vs.* physical thickness

$$\text{EOT} = \frac{\kappa_{SiO_2}}{\kappa_{IL}} t_{IL} + \frac{\kappa_{SiO_2}}{\kappa_d} t_d \qquad [3]$$

where *t* is physical thickness of the layer and the subscripts refer to the (lower) interface layer (IL) and the high-κ dielectric (d). In Fig. 11, the EOT of the $HfSiO_4$ layers is plotted *vs.* the thickness of the layers (ellipsometer data, as-deposited polysilicon). The as-determined *k*-values of SiO_2-rich layers are $k = 5.5$ (O_3 start pulse, not shown) and $k = 4.8$ (Al_2O_3 start surface), and of HfO_2-rich layers with identical start conditions $k = 12.3$ and 15.1, respectively.

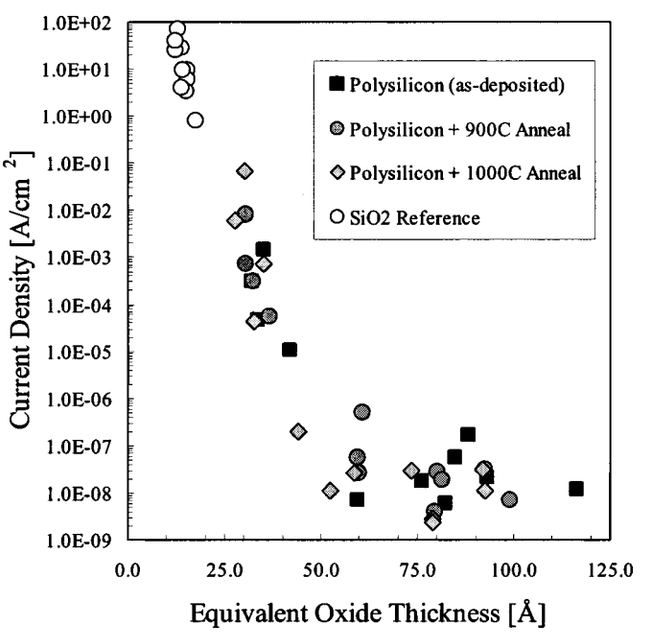

Figure 13. Leakage current densities at $|V_{FB} - 1|$ as function of EOT (both SiO_2-rich and HfO_2-rich layers).

According to Table II, the thickness of the layers as found with NanoSpec is overestimated by roughly 10% as compared to HR-TEM, so that the *k*-values given here are possibly overestimated by the same percentage. The possible *k*-value variation as a function of the annealing temperature and the phase segregation as discussed previously could not be accurately determined, mainly because of the uncertainty in the physical thickness of the layers after annealing. Considering errors in fitting the C-V data and variation in the thickness and composition, the estimated overall error in the given *k*-values is around 10%.

It has been suggested in the past that the *k*-values of HfO_2/SiO_2 vary superlinearly as a function of the Hf:Si composition ratio.[30] In Fig. 12, the *k*-values of $HfSiO_4$ are plotted *vs.* the Hf/(Hf + Si) composition ratio (RBS data). In this figure, two data points of ALD ZrO_2/SiO_2 layers have been included.[23] Clearly, we observe a sublinear scaling behavior of the *k*-value as function of the composition.

Figure 13 shows that the leakage currents measured at $|V_{FB} - 1|$ are higher than the SiO_2 reference. This indicates that both types of $HfSiO_4$ layers are rather poor dielectrics. The high leakage currents might be due to the intrinsic roughness in the silicon substrates (see HR-TEM in Fig. 6) or abundant bulk or interface defects. Both types of defects result in defect-assisted tunneling through the bulk of the layers. This was investigated by measuring the I-V characteristics in the range 25-150°C. An increase of the leakage current at higher substrate temperature could indicate the presence of shallow defects, which are thermally activated. Here it was found that an increase of the temperature had only a minor effect (<0.5 order of magnitude) on the leakage current through thin layers, whereas one to two orders of leakage current increase could be observed for thicker layers. This would indicate direct tunneling through thinner layers and defect-assisted tunneling through the thicker layers.

Conclusions

The physical and electrical properties of $HfSiO_4$ layers deposited by ALD using $HfCl_4$ and APTES as precursors were reported. An $HfCl_4$:APTES ALD pulse ratio of 1:1 resulted in a SiO_2-rich $HfSiO_4$ dielectric layer with a Hf/(Hf + Si) ratio of around 0.36. The average deposition rate of this type of $HfSiO_4$ layer is 0.82-0.84 Å/sequence. A $HfCl_4$:APTES ALD-pulse ratio of 5:1 resulted in a HfO_2-rich layer with a Hf/(Hf + Si) ratio of 0.56 and an average deposition rate of 2.25-2.42 Å/sequence. In both types of layers, roughly 10% excess oxygen was found ($O/(Hf + Si) \sim 2.2$). In the first, no crystallization was found up to 1100°C, and in the latter the HfO_2-cubic phase was detected at 850°C. As-determined *k*-values range from 4.8 (SiO_2-rich) to 15.1 (HfO_2-rich). Both values were determined within approximately 10-15% error. RBS, XPS, and HR-TEM analysis revealed substantial changes in the homogeneity of the layers upon RTA, both with and without a polysilicon layer on top. No dependence of the *k*-value on the annealing temperature could be determined, mainly because of the uncertainty in the thickness of the layers after anneal. The leakage currents through annealed layers increase more with temperature than those through as-deposited layers. This observation suggests that trap-assisted tunneling is the dominating leakage current mechanism. Therefore, optimizing the stoichiometry of the $HfSiO_4$ layers without compromising the EOT seems crucial for improving both the thermodynamic and the electrical properties of ALD $HfSiO_4$ layers deposited using this chemistry.

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