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S. B. Herner, M. Mahajani, M. Konevecki, E. Kuang, S. Radigan, and S. V. Dunton

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Polycrystalline silicon/$CoSi_2$ Schottky diode with integrated SiO_2 antifuse: a nonvolatile memory cell

S. B. Herner,[a] M. Mahajani, M. Konevecki, E. Kuang, S. Radigan, and S. V. Dunton
Matrix Semiconductor, Santa Clara, California 95054

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A Schottky diode consisting of doped polycrystalline silicon (polysilicon) and $CoSi_2$ films is described. When an SiO_2 antifuse thin film is grown in between the polysilicon and $CoSi_2$, the film stack can function as a nonvolatile one-time programmable memory cell. The cell is programmed when the SiO_2 that insulates the doped polysilicon from the $CoSi_2$ is broken down by applying a large biasing field, and unprogrammed when the antifuse is not broken down. By taking advantage of the ability to grow SiO_2 directly on $CoSi_2$, the entire device can made with only two masking steps and relatively simple tool set, while achieving high density. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1581364]

We describe a nonvolatile cell for one-time field-programmable read-only memories. The device described in this paper is a Schottky diode made from *in situ* doped-polycrystalline silicon (polysilicon) and $CoSi_2$. A thin SiO_2 antifuse is grown on top of the $CoSi_2$, followed by doped polysilicon deposition and then another film of $CoSi_2$. The $CoSi_2$ film forms the interconnection to the cell. A diode is formed when enough voltage is applied across the SiO_2 film to break it down and create a metal–semiconductor junction. Other forms of this device have been presented. De Graaf *et al.* described a diode-programmable read-only memory cell based on n^+/p^- diodes using a combination of polycrystalline and single-crystal silicon with integrated antifuses.[1] More recently, Crowley *et al.* described a p^+/n^- diode cell based completely on polysilicon with integrated SiO_2 antifuse.[2] By using polysilicon, the cells could be stacked above the transistor drivers in single-crystal silicon, and one another, reducing die size compared to single crystal silicon-based cells. Both of the cells achieved a high density with relatively few masking steps. However, both the cells required *n*- and *p*-type doping of silicon, and placed the antifuse in between two silicon films. The Schottky diode-based cell described in this letter achieves the same high density, but at lower cost with simplified fabrication. The cell described here requires only one type of doped silicon, and the antifuse (SiO_2) is grown directly on the interconnection ($CoSi_2$) for the cell. By taking advantage of *in situ* doping of silicon to vary depth profile concentration instead of ion implantation, process complexity is minimized. We describe device fabrication, breakdown properties of the antifuse related to growth conditions, and cell operation.

Devices were fabricated on 200-mm oxide-coated silicon wafers using 0.22-μm lithography. Silicon was deposited with a low-pressure chemical vapor deposition (CVD) furnace operating at 400 mTorr, 540 °C, using helium-diluted SiH_4 and doped with PH_3 (bal. He). The first silicon film was phosphorus-doped to a concentration of $1.3\times10^{20}/cm^3$, as measured by secondary ion mass spectrometry. The amorphous n^+-doped silicon film was patterned using standard lithographic techniques, and then etched to produce 0.22-μm-wide lines. After silicon was etched and photoresist was stripped, high-density plasma CVD SiO_2 was deposited to isolate the silicon lines. The wafers were chemomechanically polished to remove SiO_2 from the top of the silicon lines, producing a planarized surface [Fig. 1(a)].

A selective process was used to form $CoSi_2$ on top of the silicon, forming the bit lines. After an HF dip to clean the silicon of any native oxide on the silicon lines, cobalt and titanium were sputtered in a cluster tool. Wafers were rapid thermally annealed (RTA) to form $CoSi_x$. Unreacted Co + Ti were then removed by wet etching. A second RTA at 740 °C converted the remaining $CoSi_x$ to $CoSi_2$. Resulting $CoSi_2$ was approximately 50 nm thick. Antifuses were grown on the $CoSi_2$ by oxidation in a RTA chamber using 5 liters of oxygen gas (99.9999% purity) at various temperatures and times [Fig. 1(b)]. A second PH_3-doped silicon deposition was then done, doping the first 100–300 nm to a concentration of $1-3\times10^{17}$ phosphorus/cm^3, and the final 100–200 nm to a concentration of 1.3×10^{20} phosphorus/cm^3. Steps were then repeated to form a second set of silicon lines orthogonal to the first, with SiO_2 gap-fill and $CoSi_2$ conductive lines on top (the word lines). The anneals crystallized the amorphous silicon and activated the dopants. Chemomechanical overpolish of the gap-fill SiO_2 on top of silicon was carefully controlled to leave at least 10 nm of n^+-doped silicon on top of the second polysilicon lines [Figs. 1(c) and 1(d)]. This ensures an ohmic contact between the silicon and $CoSi_2$. Antifuses were not grown on top of the second film of $CoSi_2$. Thick oxide was then deposited by plasma-enhanced CVD, and tungsten vias connected the second $CoSi_2$ film to aluminum pads on top of the thick oxide (''top metal''). A cross-sectional transmission electron microscope (TEM) micrograph of four cells is shown in Fig. 2.

Single diodes were tested using an Agilent 4156C semiconductor parameter analyzer. Voltage was applied in ''sweep'' fashion, using a sweep rate of 3 V/s from 0 to +10 V, and then back to 0 V, and from 0 to −6.5 V and then back to 0 V. TEM was used to measure SiO_2 antifuse film thickness. Areas of the TEM foil where the $CoSi_2$ film is orthogo-

[a]Electronic mail: brad@matrixsemi.com

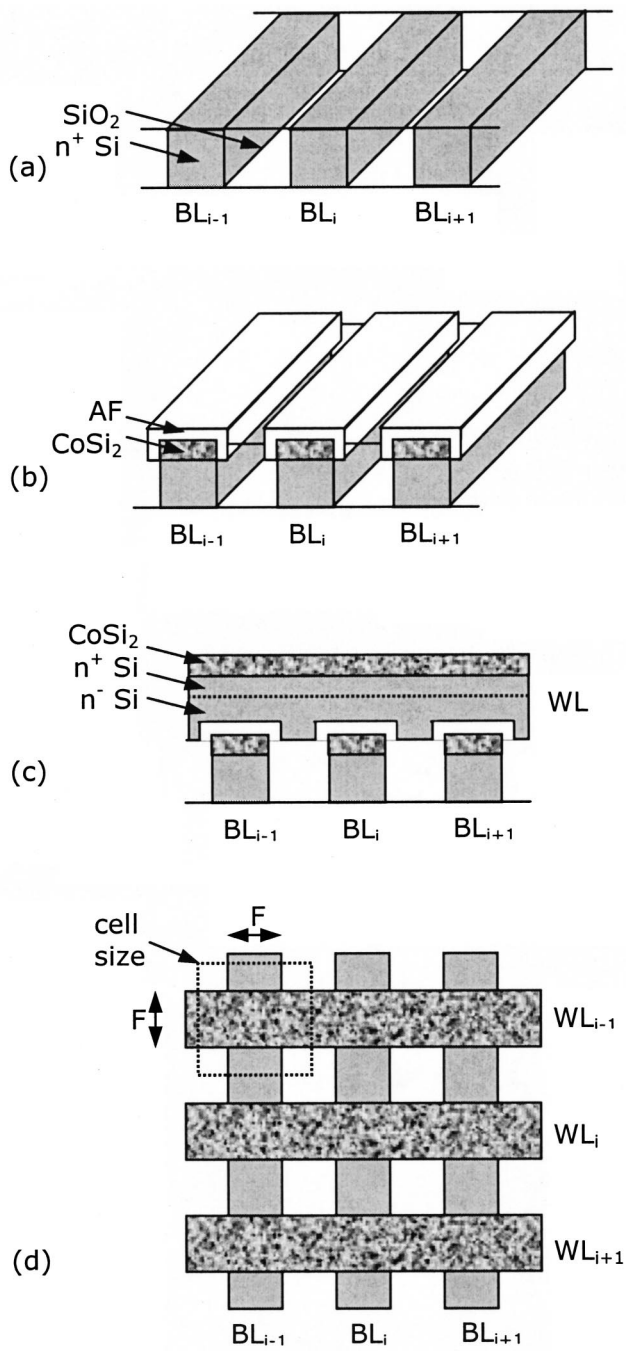

FIG. 1. Schematic flow of the process steps to make the memory cell. (a) bit-line (BL) formation: doped silicon lines with SiO_2 insulation in between; (b) formation of $CoSi_2$ and SiO_2 antifuse on top on BLs; (c) word line (WL) formation: doped silicon lines orthogonal to the BLs underneath, with $CoSi_2$ on top; and (d) plan view of the cells (F = feature size).

nal to the foil were selected for thickness measurement to minimize error from the rough $CoSi_2$/poly-Si interface.

The breakdown voltage of the SiO_2 film was found to correspond generally to the thickness of the oxide film, and was not a strong function of the doping concentration or the thickness of either the lightly or heavily doped polysilicon films (Table I). Previous work has shown that oxides grown on $CoSi_2$ are stoichiometric SiO_2, although this has been confirmed only on much thicker SiO_2 films (> 20 nm).[3] The only report of very thin oxides grown on $CoSi_2$ could not confirm that the films were stoichiometric SiO_2.[4] Cross-sectional TEM imaging shows that the SiO_2 films have uniform thickness over the $CoSi_2$, even as they transition over $CoSi_2$ grain boundaries (Fig. 3). Thickness uniformity of the antifuse film is important to achieve uniform breakdown voltage for all devices.

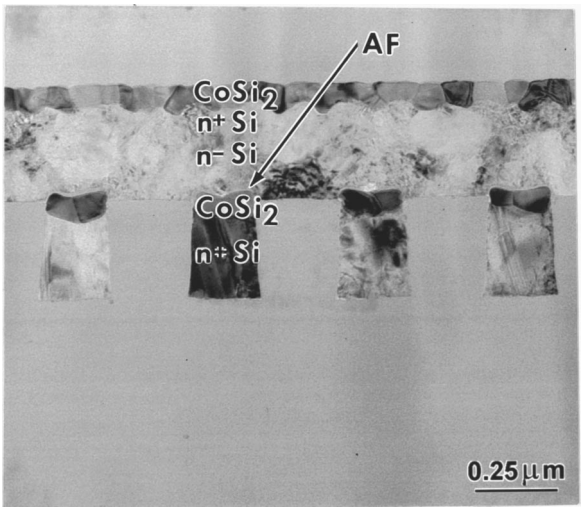

FIG. 2. Cross-sectional transmission electron micrograph, using bright-field conditions, of four bit lines and a word line (the location of the antifuse film, AF, is indicated, but is too thin to be visible in this image).

The rough interface between polysilicon and $CoSi_2$ is typical for this film stack. Silicide grain boundary grooving occurs as a result of the reduction in surface and interfacial energy during anneal at elevated temperature.[5] Silicide grain boundary grooving results in a rough $CoSi_2$ surface on which the SiO_2 antifuse film is grown. The median breakdown voltage for the antifuses grown at 700 °C for 20 s was found to be 5.7 V with a 1-sigma variation of 0.5 V for 20 cells tested. The median breakdown voltage for the antifuses grown at 800 °C for 30 s was 8.5 V. We extract a breakdown field of 7.6 (5.7) MV/cm for the oxides grown at 700 °C/20 s (800 °C/30 s) on $CoSi_2$, compared with reported values 12.6–14.0 MV/cm for high-quality SiO_2 grown on single-crystal silicon.[6] The relatively rough $SiO_2/CoSi_2$ interface shown in Fig. 3, compared to SiO_2 grown on single-crystal silicon undoubtedly leads to a greater density of defects at the interface, particularly at $CoSi_2$ grain boundaries. The roughness increases the local electric field.[7] Interface roughness increases with increasing SiO_2 growth temperature, with silicide grain grooving occurring simultaneously. The lower breakdown field of the SiO_2 antifuse film grown at 800 °C compared to the one grown at 700 °C (Table I) is consistent with higher local fields produced by a rougher $CoSi_2$ film.

A typical $(I-V)$ curve for the memory cell is shown in

TABLE I. Properties of the SiO_2 antifuse film with growth conditions (N/A = not available).

SiO_2 growth conditions (5-L O_2 flow)	SiO_2 thickness by TEM (nm)	Breakdown voltage (V)	Breakdown field (MV/cm)
670 °C/20 s	N/A	5.0	N/A
700 °C/20 s	7.5±0.5	5.7	7.6±0.5
700 °C/40 s	8.2±0.5	N/A	N/A
700 °C/120 s	9.0±0.5	N/A	N/A
800 °C/30 s	15.0±0.5	8.5	5.7±0.2

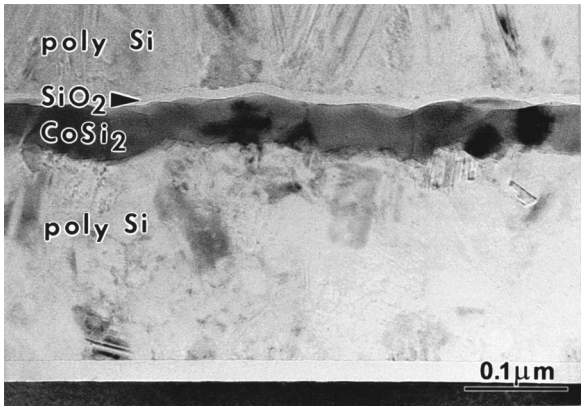

FIG. 3. Transmission electron micrograph, using bright-field conditions, of SiO_2 film on $CoSi_2$. Oxide growth was done at 700 °C, 760 Torr, in 5 L of O_2 flow for 120 s. The SiO_2 film has been ''capped'' with polysilicon to provide better contrast.

Fig. 4. The selected cell has a high voltage applied to the bit line while the word line is held at ground. The unselected bit and word lines are biased in the opposite polarity. The large increase in forward current at +5.5 V is indicative of breakdown of the SiO_2 film separating the $CoSi_2$ on the bit line and n^--doped silicon film in the word line. To minimize power consumption during device operation, high forward current at low voltage is preferred during read of the cell.

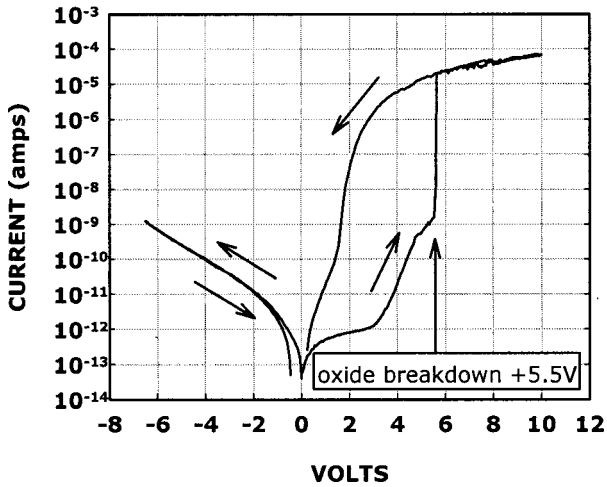

FIG. 4. Typical $I-V$ curve for Schottky diode with SiO_2 breakdown at +5.5-V forward bias voltage.

Low reverse current (''leakage'') minimizes current loss and prevents breakdown in nonselected bit lines. The ''programming'' voltage (+5.5 V in this example) of the cell is much higher than the ''read'' voltage (+3 V) to avoid conflicts between programming and reading the device. The current difference at +3 V equivalent to six orders of magnitude between a programmed cell and an unprogrammed cell provides the ability to ''sense'' individual programmed and unprogrammed cells within relatively large arrays of cells.

We have developed a low-cost, field-programmable memory cell device based on $CoSi_2$/polysilicon Schottky diodes with integrated SiO_2 antifuses. The ability to grow thin, high-quality SiO_2 films directly on $CoSi_2$ allows cells to be formed using a polysilicon deposition doped with a single dopant type. The entire cell is formed with two masking steps and a simple tool set. The cell is programmed when the antifuse that insulates the doped polysilicon from the $CoSi_2$ is broken down by applying a large biasing field, and unprogrammed when the antifuse is not broken down. The breakdown field of the SiO_2 film was found to be 5.6–7.6 MV/cm compared to 12.6–14.0 MV/cm for high-quality gate oxide grown on single-crystal silicon. Cell performance is based on a difference in current of over six orders of magnitude between a programmed and unprogrammed bit at +3-V read voltage.

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