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Fabrication of Silicon-Submicron-Wire-Based Solar Cells on UMG-Si Substrates Using Nickel Catalyst

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Solar cells based on arrays of vertical Si submicron or nano-sized wires are promising candidates for lowering production-related material costs while still obtaining efficiencies competitive with those of planar multicrystalline Si cells. To the best of our knowledge, our study is the first to examine the growth of silicon submicron wires on upgraded metallurgical-grade Si (UMG-Si) substrates catalyzed by nickel (Ni) using the chemical vapor deposition technique. We examined which conditions are most favorable for the growth of silicon submicron wires by varying the annealing temperature and the annealing time duration: Ni film was annealed with a temperature range of 900–975°C and a time range of 2-12 min. We subsequently analyzed and compared the output characteristics of the silicon submicron-wire-based (Si-SMW-based) solar cells. Our results indicate that silicon wires with diameters ranging from 0.2 to 0.8 μm could be grown with the present technique. Moreover, a conversion efficiency of greater than 1% was achieved for the Si-SMW solar cells fabricated with the Ni catalytic film annealed at 950°C. In particular, annealing the Ni catalytic film for 2 min while growing the submicron wire structure produced a solar cell with an efficiency as high as 2.06%.

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Solar cells based on arrays of vertical Si submicron or nano-sized wires are promising candidates for lowering production-related material costs while still obtaining efficiencies competitive with those of planar multicrystalline Si cells. Their structures can increase the absorption efficiency of incident light, which is also beneficial for improving the external quantum efficiency of solar cells. Moreover, when the solar cell p-n junction is fabricated along the radial direction of the wire structure, the diffusion length of the optically produced minority carriers can be shortened, thereby enhancing the collection efficiency of these carriers.[1] Using the cylindrical geometry of Si nano-sized wires as opposed to a planar geometry allows lower-purity silicon to be used in the Si-based solar cells with minimal efficiency loss, thereby reducing the production costs.[2] A further significant reduction in the production costs is achieved by using thin-film techniques, such as roll-to-roll processing as well as chemical vapor deposition (CVD) to prepare the active layer described above.

So far, much progress has been reported in the research of Si-nanowire (SiNW)-based solar cells where the CVD technique was used to fabricate the SiNW structures. Tsakalakos et al. fabricated a SiNW-based radial-p-n-junction solar cell on a stainless steel substrate, attaining a conversion efficiency of 0.1%.[3] A similar efficiency has also been achieved from a SiNW-based axial-p-n-junction solar cell fabricated with n-type nanowires prepared on a p-type Si substrate.[4] The beneficial effect of using nanowires in a solar cell is mostly attributed to improved light-trapping characteristics.[1,5] However, a higher surface recombination effect should also be induced due to the larger effective area introduced by the nanowires. Gunawan and Guha coated the SiNW-based radial-p-n-junction solar cell with an Al_2O_3 surface passivation layer and improved the solar conversion efficiency to 1.8%.[6] A planarization step of a SiNW array was used to form a high-quality front electrical contact, improving the efficiency of the fabricated axial-p-n-junction solar cell to 1.9% for an illumination intensity of 100 mW/cm^2.[7] For all the catalytic growth of the SiNWs mentioned above, gold (Au) was used as the catalyst, and monocrystalline Si substrate was used to obtain the vertically oriented wire array.[4,6,7] However, research indicates that Au is incorporated in the bulk of the Si nanowires,[8] which would possibly induce a deep-level trap, causing a reduction in the efficiency of the solar cells prepared in this manner.[9] Kendrick et al. have recently fabricated a radial-p-n-junction solar cell with a 2.3% efficiency by using Si wire arrays, catalytically grown on patterned Si substrates by Au.[10] In that work, a Si wire array was first treated with repeated thermal oxidation and oxide etching to remove any residual Au from the wire tips, and then a radial p-n junction was formed through $POCl_3$ thermal diffusion.

In this work, we report the catalytic growth of Si submicron wires on upgraded metallurgical grade Si (UMG-Si) substrates with nickel (Ni) as the catalyst. In particular, we analyze and compare the characteristics of Si-submicron-wire-based (Si-SMW-based) solar cells fabricated with catalytic film annealed under various conditions. To the best of our knowledge, our study is the first to examine the feasibility of analogous cell structures on UMG-Si substrates. We devised the material structure as a means of achieving an energy-conversion efficiency approaching that of wafer-based crystalline Si solar cells yet with costs competitive to those of producing solar cells with thin-film technologies.

Experimental

The starting material was boron-doped UMG-Si substrates, each with an area of 4×4 cm^2, a thickness of 200–180 μm, a resistivity of 0.2 Ω-cm, and a hole concentration of 2.5×10^{17} cm^{-3}. Before the Si submicron wires were fabricated, the UMG-Si substrate was cleaned by the RCA clean procedure.[11] After the substrates were washed ultrasonically in sequence using trichloroethylene, acetone, and deionized water, the saw damage was removed with 20% KOH alkaline etching solution at a temperature of 75°C for an etching time of 5 min. Next, the oxidized surface of UMG-Si was removed using a buffered HF aqueous solution ([HF]:[H_2O] = 1:10), forming a hydrogen-terminated substrate.

For the catalytic growth of the Si submicron wires, a 10-nm-thick Ni layer with a purity of six 9's was first deposited on the substrate by an e-gun evaporator, used to deposit the catalyst for the nucleation of the polysilicon nuclides. The Ni layer was then annealed in a halide CVD chamber at temperatures which varied from 900 to 975°C and for time durations which varied from 2 to 12 min. Si submicron wires were then produced through the vapor-liquid-solid (VLS) growth mechanism after introducing dichlorosilane (SiH_2Cl_2) with a flow rate of 15 cc/min and a flow time of 5 min using H_2 as the carrier gas. After the Si submicron wires were grown, the specimens were dipped in a 5% buffered HF aqueous solution to etch away the Ni metal on top, which would hinder the formation of a p-n junction in the following step. Finally, the n^+-p junction of the Si-SMW-solar-cell material structure

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was fabricated in a diffusion chamber with a diffusion temperature which varied from 780 to 830°C and a fixed diffusion time duration of 20 min. The n^+ region formed on the surfaces of the Si submicron wires was completed by the diffusion of phosphorous atoms into the substrate using phosphorous oxychloride ($POCl_3$) as the source of the phosphorus atoms. A back electrode was formed by covering the bottom surface of UMG-Si substrate with aluminium paste (AG PRO TECHNOLOGY CORPORATION) using screen-printing technology and sintering the contact in an infrared rapid thermal annealing (RTA) furnace to produce the back surface field. The Ti/Pd/Ag metal system was deposited on the top surface of the specimen by an e-gun evaporator, and RTA annealing followed to form the front electrode with a finger contact pattern that was defined using a metal mask. The thin layer of titanium (500 nm thick) is used as the bottom layer because it adheres well to silicon and the silver (1 μm thick) is used as the top layer due to its low resistance and solderability. A layer of palladium (70 nm thick) sandwiched between the two layers mentioned above prevents any undesirable reaction between the Ti and Ag layers in the presence of moisture. After deposition, the contacts were sintered at 450°C in H_2 ambient to ensure a good adherence and a low contact resistance. The 4×4 cm^2 specimen was then scribed to form solar cells with a cell size of 1×1 cm^2.

The crystalline quality of the Si submicron wires was examined by means of x-ray diffraction (XRD) analysis. The surface morphology of the specimens was characterized using a scanning electron microscope (JEOL-6700F). Optical reflectance spectra were measured with a Shimadzu UV-VIS-NIR spectrophotometer. The current voltage (I-V) characteristics of the Si-SMW solar cells fabricated were measured using a solar simulator (Wacom, WXS-155s-10) under AM1.5 illumination conditions. We then analyzed and compared the cell parameters corresponding to each solar cell, namely, the open-circuit voltage (V_{oc}), short-circuit current (I_{sc}), fill factor (FF), and energy conversion efficiency (E_{ff}).

Results and Discussion

The growth of Si submicron wire structures was realized by performing Ni catalysis at different temperatures, ranging from 900 to 975°C, with a constant annealing time duration of 6 min. However, only those fabricated at 950°C could demonstrate clear Si(111) and Si(220) XRD peaks as shown in Fig. 1. From the binary Ni-Si phase diagrams as calculated, in the Ni-rich region the lowest eutectic point at Ni-Si liquidus is around 964°C.[12] However, it is suggested that the formation of Ni-Si droplets at lower temperatures is possible in this study due to that the thin Ni film shrinks into small islands during the annealing treatment, the melting points of them are lower than that of the corresponding bulk solid. This result simultaneously accompanied by the interdiffusion of Si atoms from the substrate during the annealing process had made it possible to form Ni-Si droplets at a

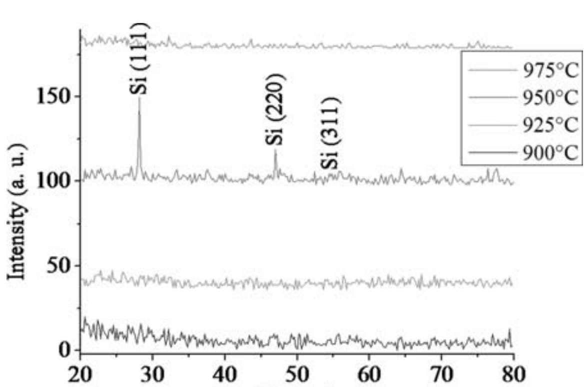

Figure 1. XRD analysis results of Si submicron wire structures produced at different temperatures.

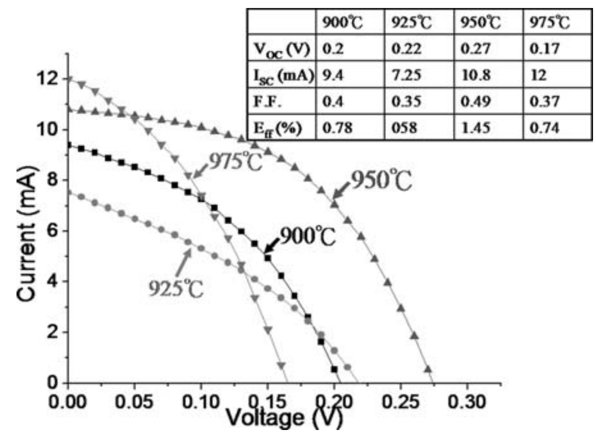

Figure 2. I-V characteristics of Si-SMW solar cells under AM 1.5 illumination with Si submicron wires produced at various temperatures.

temperature as low as 900°C. Next, the surface of the Ni-Si eutectic droplets has a large accommodation coefficient for gas source and is therefore a preferred site for gas deposition. Therefore, the introduction of dichlorosilane source into Ni-Si droplets would afford enough supersaturation for the nucleation of Si wires. It is noticeable that although our Si wires can be grown at the temperatures: 900–975°C, only those obtained at 950°C demonstrate the XRD peaks mentioned above, manifesting a crystalline structure with preferred orientations. Comparatively, those fabricated at other temperatures became disordered (polycrystals with random orientations). The I-V characteristics of the Si-SMW solar cells with submicron wire structures prepared at temperatures ranging from 900 to 975°C are shown in Fig. 2 along with an inset that summarizes the parameters extracted from these curves. As can be seen, only the device based on the wire structures produced at 950°C shows a conversion efficiency greater than 1%. Therefore, our results indicate that a superior quality of submicron wire structure is best achieved with annealing at 950°C compared to other temperatures in the range studied. The fabrication conditions of the Si submicron wires were studied further by maintaining the annealing temperature at 950°C but varying the annealing time duration for the Ni catalyst. Figs. 3a–3e show the scanning electron microscopy (SEM) planar and cross-sectional views of the Si-SMW structures prepared with the Ni films annealed for 2, 4, 8, 10, and 12 min, respectively. From the planar SEM images, it seems that the grown Si wires can be roughly categorized into two groups: the thinner ones with the diameters ≤0.3 μm and the thicker ones with the diameters ≥0.5 μm. As demonstrated in the cross-sectional SEM images, Si wires grown through the VLS mechanism on poly-Si substrate are difficult to maintain their correspondence in both the direction and diameter, the wires curve in different orientations within a thickness range of 4–6 μm. Overall, the proportion of the thicker ones increases with the duration of the annealing time. This phenomenon might be explained using the information presented in Figs. 4a and 4b, depicting the SEM surface images of Ni films after the films were annealed at 950°C for 2 and 12 min, respectively. An increase in the annealing time duration should enhance the agglomeration of the Ni melt, causing a decrease in the number of Ni droplets. After SiH_2Cl_2 molecules have been supplied, the sticking coefficient of the resultant Si species is higher in the Ni liquid than on the solid UMG-Si surface, resulting in crystal growth only where liquid Ni droplets are present. Then when the eutectic Ni-Si alloy becomes supersaturated with Si, silicon atoms precipitate out of the supersaturated Ni-Si droplet and nucleate at the interface between the liquid alloy and the solid UMG-Si, and Si submicron wires grow to lift the droplets. In the nucleation stage, the number and size of the liquid Ni catalyst droplets delivered on the silicon substrate are important parameters. Although a definite relationship between the size of a Ni droplet and the annealing conditions has not yet been established, decreasing the number of Ni droplets

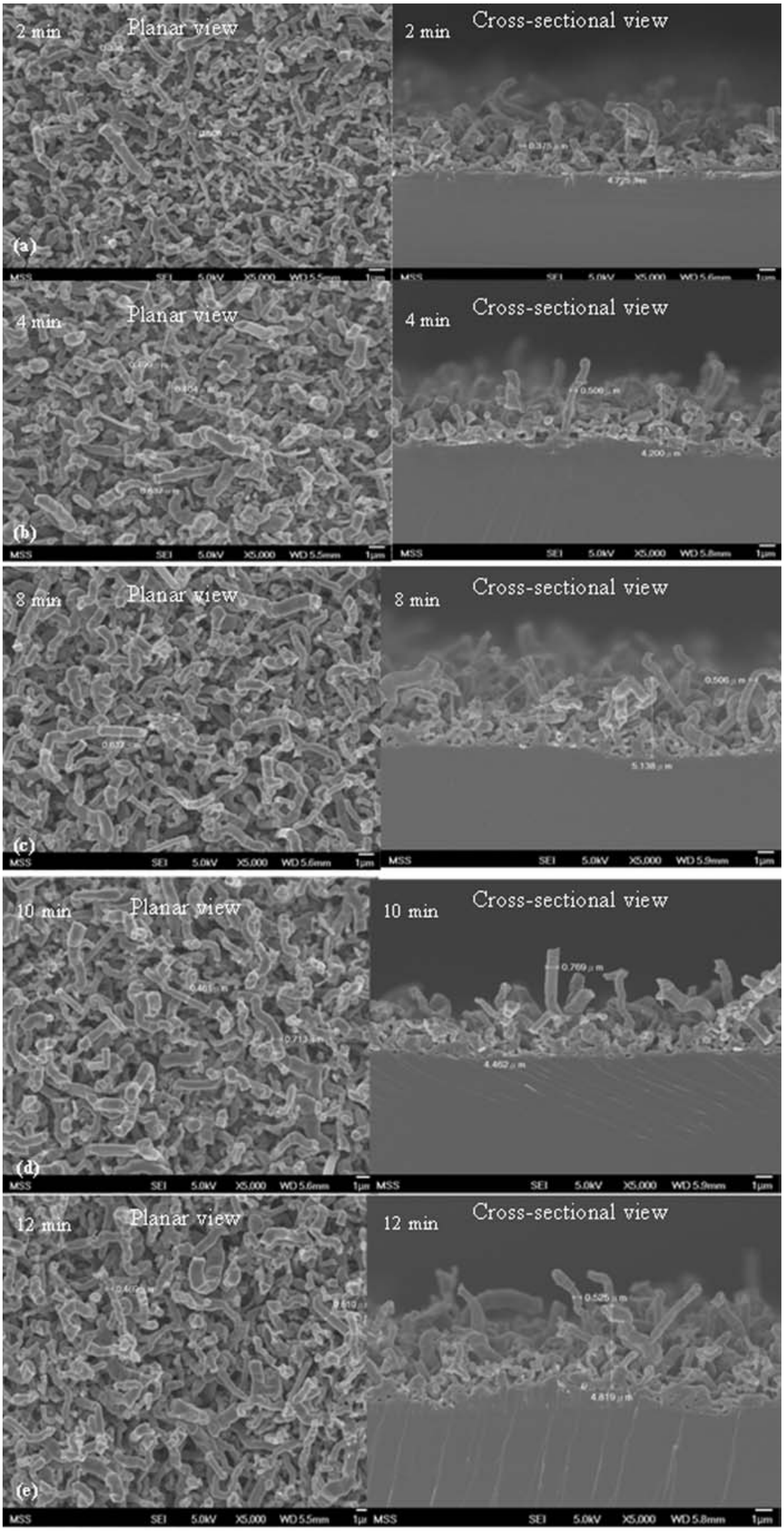

Figure 3. Planar and cross-sectional SEM images of Si submicron wire structures prepared with Ni catalytic film annealed at 950°C for (a) 2, (b) 4, (c) 8, (d) 10, and (e) 12 min.

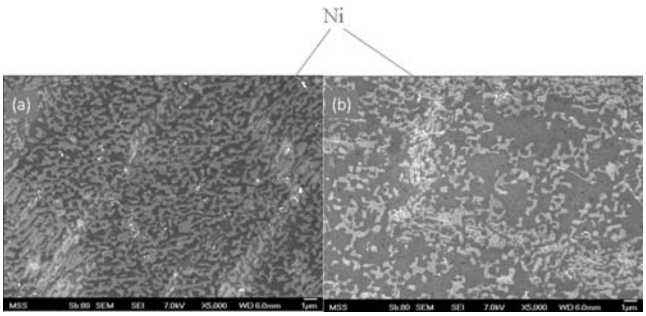

Figure 4. SEM surface images of Ni film annealed at 950°C for (a) 2 min and (b) 12 min.

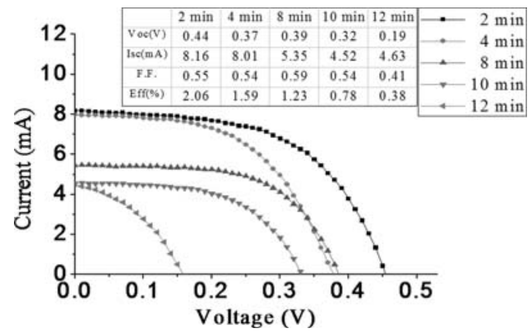

Figure 6. I-V characteristics of Si-SMW solar cells under AM 1.5 illumination with Ni catalytic film annealed for 2–12 min.

is generally thought to introduce a higher supersaturation for each Ni droplet in the nucleation stage. This is because the origins of the supersaturation should not only be from vapor precursors impinging directly on the droplets but also from the surface diffusion of source atoms occurred on the substrate surface. A sparse distribution of large droplets might attain quite a amount of supersaturation through the surface diffusion of source atoms. This reasoning would favor an increase in the number of thicker and longer Si wires due to a higher growth rate; such wires were observed in the specimens with the Ni catalytic film which was annealed for more than 8 min. Meanwhile, we have examined the elemental composition of Ni droplets by energy dispersive X-ray (EDX) analysis and one of the results is shown in Fig. 5a. For reference, the EDX spectrum obtained from the region free of Ni is displayed in Fig. 5b. As can be seen, except Si and a small amount of O elements no other impurity from the UMG-Si substrate is observable.

All the submicron wire structures fabricated with the Ni catalytic film annealed for various time durations demonstrated an average reflectance of about 0.1% compared to 0.4% for the polished UMG-Si wafer over the range of 300–1400 nm. It can be said that the antireflection characteristics, namely, the light trapping effects of the submicron wire structures produced on UMG-Si substrate, are similar. The following text examines the carrier collection effects of the devices prepared using these structures. It should also be noted that as demonstrated in the cross-sectional SEM images, each UMG-Si substrate surface is fully covered with Si-SMWs regardless of how thick the layer deposited. Our Si-SMWs curve in different orientations and interconnect one another, almost forming a mesoporous structure within a range of 2 μm from the substrate surface. Consequently, the contribution from the p-n junction at the UMG-Si surface can be neglected.

Fig. 6 shows the I-V characteristics of the Si-SMW solar cells fabricated using the Si wire structures shown in Fig. 3, and the inset summarizes the parameters obtained. As can be seen, annealing the Ni catalyst for a time duration shorter than 4 min would present a conversion efficiency of greater than 1.5% for the Si-SMW solar cell. In particular, the specimen prepared with Ni catalyst annealed for a short duration of 2 min exhibited a superior efficiency of 2.06%; the same specimen also showed the highest V_{oc} and I_{sc} of 0.44 V and 8.16 mA, respectively. Noticeably, both V_{oc} and I_{sc} decrease with increasing annealing time duration, and the conversion efficiency decreases to less than 1% when the Ni catalyst was annealed for more than 10 min. The cell qualities were further compared by examining their shunt

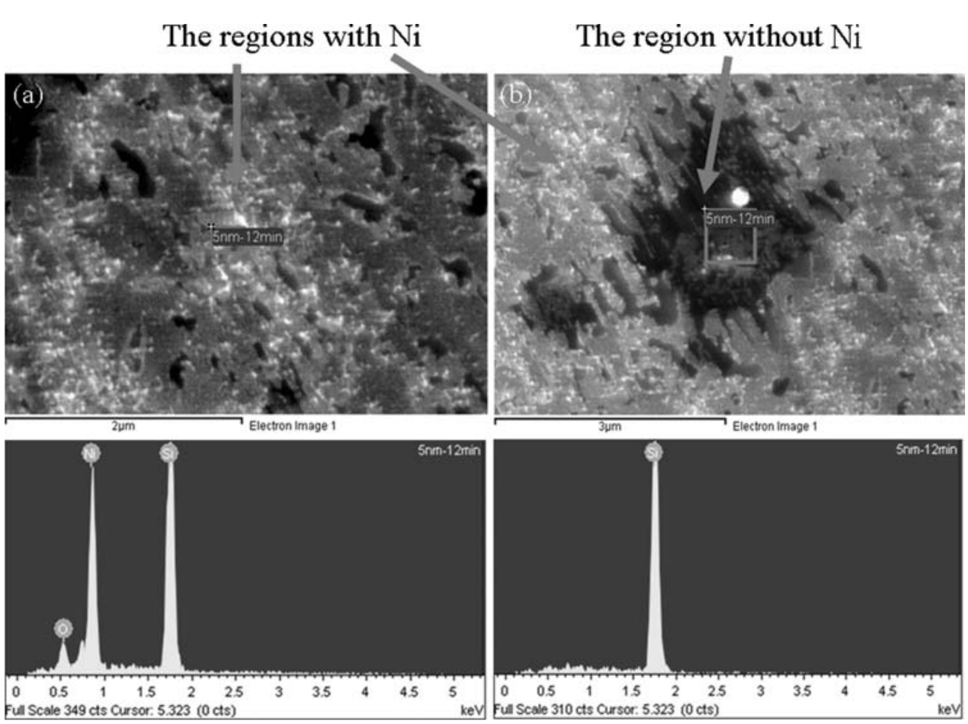

Figure 5. EDX analysis results of Ni catalyst after being annealed to form droplets: (a) the region with Ni-Si alloy and (b) the region without the coverage of Ni metal.

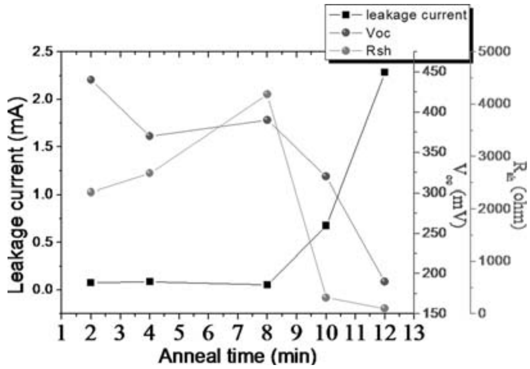

Figure 7. Variations of the leakage current, R_{sh}, and V_{oc} for Si-SMW solar cells plotted as a function of Ni annealing time duration.

resistance (R_{sh}) and series resistance (R_s). The leakage current and R_{sh} of the solar cells were derived from the reverse-bias I-V characteristics in the dark, with the former measured at -0.2 V, while the latter was derived from the linearly approximated region of the I-V curve. Fig. 7 displays the variations of the leakage current, V_{oc}, and R_{sh} as a function of the annealing time duration of Ni catalytic film. As shown, the leakage current for the specimens with the Ni film annealed for 8 min or less show several tens of nA in magnitude, while those for the specimens with the Ni film annealed for more than 8 min exhibit magnitudes on the order of mA. The R_{sh}'s were found to be higher than 2.3 kΩ and lower than 500 Ω for the specimens with the Ni film annealed for shorter than and longer than 8 min, respectively. These results imply that both the wire filling ratio and the wire diameter influence the R_{sh}. We suggest that shortening the annealing time duration for Ni film to about 8 min would induce the growth of homogeneously-distributed Si wires, which is beneficial for increasing R_{sh} and therefore the V_{oc} of the devices fabricated. Moreover, a further reduction of the annealing time duration for Ni film to 2 min enhanced the involvement ratio of thin submicron wires as demonstrated in the previous SEM images. It is noteworthy that for an annealing time duration of 2 min, both V_{oc} and I_{sc} increase compared to the condition with an annealing time duration of 8 min, regardless of a slight decrease of R_{sh} from 4.2 kΩ to 2.3 kΩ, probably due to the enhancement of surface recombination effects. Indeed, a submicron-wire radial-p-n-junction-geometry structure has been devised to minimize bulk recombination. A homogeneously dense distribution of such wires on a solar cell surface was expected to offer efficient carrier separation effects. However, unlike the Si wire array fabricated on monocrystalline Si substrates, the Si wire array fabricated on the UMG-Si substrates could not exhibit unified wire orientations, making it difficult to analyze the detailed mechanisms for the device improvements mentioned above. Up to now, solid-state solar cells using VLS-grown SiNW arrays have faced many challenges and yielded a low V_{oc} (mostly $<$300 mV) and a limited cell efficiency ($<$2%). Nevertheless, we have demonstrated that Si-SMW solar cells with a V_{oc} of greater than 400 mV and an efficiency of greater than 2% can be produced on UMG-Si substrate. Certainly, the quality of the devices fabricated must still be improved for practical applications, and many issues must still be clarified or addressed: For example, high values ranging from 9 to 13 Ω have been estimated for the R_s's of all the Si-SMW solar cells produced, which are inferior to the R_s values of conventional Si solar cells (about 0.5 Ω) and might be one of the causes for a low J_{sc} ($<$10 mA/cm^2). Besides the high R_s, there are also serious surface and/or interfacial recombination effects that occur in the present device structure. For this reason, to address the cost issue of Si solar cells using wire geometry, further studies on surface passivation and contact optimization are critical for improving device performance in the future.

Conclusions

Submicron-sized Si wires with 0.2 – 0.8 μm diameters were synthesized on UMG-Si substrates by CVD using Ni catalyst annealed under various conditions and the output characteristics of the Si-SMW solar cells fabricated on them were examined. We found that an annealing treatment of Ni catalytic film at 950°C for a time duration equal to or less than 8 min was favorable for the carrier extraction of Si-SMW solar cells, yielding a conversion efficiency of greater than 1.2%. In particular, the number of thinner ($\leq$0.3 μm) wires increased when annealing the Ni catalytic film for a short duration of 2 min, resulting in an efficiency as high as 2.06% for the device produced. Our results demonstrate the possibility of developing VLS-grown Si-submicron or nanowire-based solar cells on UMG-Si substrates.

Acknowledgments

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References

1. L. Tsakalakos, J. Balch, J. Fronheiser, M. Y. Shih, S. F. LeBoeuf, M. Pietrzykowski, P. J. Codella, B. A. Korevaar, O. Sulima, J. Rand, A. Davuluru, and U. Rapol, *Journal of Nanophotonics*, **1**, 013552 (2007).
2. B. M. Kayes, H. A. Atwater, and N. S. Lewis, *J. Appl. Phys.*, **97**, 114302 (2005).
3. L. Tsakalakos, J. Balch, J. Fronheiser, B. A. Korevaar, O. Sulima, and J. Rand, *Appl. Phys. Lett.*, **91**, 233117 (2007).
4. T. Stelzner, M Pietsch, G Andrä, F Falk, E Ose, and S Christiansen, *Nanotechnology*, **19**, 295203 (2008).
5. L. Hu and G. Chen, *Nano Letters*, **7**, 3249–3252 (2007).
6. O. Gunawan and S. Guha, *Solar Energy Materials & Solar Cells*, **93**, 1388 (2009).
7. S. Perraud, S. Poncet, S. Noël, M. Levis, P. Faucherand, E. Rouvière, P. Thony, C. Jaussaud, and R. Delsol, *Solar Energy Materials & Solar Cells*, **93**, 1568 (2009).
8. G. S. Doerk, N. Feralis, C. Carraro, and R. Maboudian, *J. Mater. Chem.* **18**, 5376 (2008).
9. M. G. Mauk, *J. Mier. Met. Mater. Soc.*, **55**, 38 (2003).
10. C. E. Kendrick, H. P. Yoon, Y. A. Yuwen, G. D. Barber, H. Shen, T. E. Mallouk, E. C. Dickey, T. S. Mayer, and J. M. Redwing, *Appl. Phys. Lett.*, **97**, 143108 (2010).
11. W. Kern, Ed., *Handbook of Semiconductor Cleaning Technology*, Ch 1, Noyes Publishing: Park Ridge, NJ (1993).
12. T. B. Massalski, *Binary alloy phase diagrams*, Materials Park, Ohio: ASM International (1990).