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Growing High-Performance Tunneling Oxide by CF_4 Plasma Pretreatment

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Thin tunneling oxides grown on a CF_4 pretreated silicon substrate were prepared and investigated for the first time. The tunneling current of the CF_4-treated oxide is about three orders of magnitude higher than that of thermal oxide; furthermore, the stress-induced anomalous current and low electric field leakage current were greatly suppressed. The improvement was attributed to the incorporation of fluorine in the oxide region. Both control and CF_4-treated devices exhibited comparable channel mobility. However, pretreatment with CF_4 markedly improved the reliability of the insulator. This oxide is highly promising for fabricating low-voltage electrically erasable and programmable read-only memories (EEPROMs) without increasing the complexity of the process.
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Electrically erasable and programmable read-only memories (EEPROMs) with low operating voltages are necessary to lower the power consumption of portable electric products. A feasible method of reducing the power consumption is to reduce the thickness of the gate oxide. Equivalent electric fields and tunneling currents can be maintained when devices operate at low voltage. However, the thickness of the oxide is limited to around 6.0 nm due to the stress-induced-leakage-current, or SILC effect.[1,2] Reducing the barrier height of silicon dioxide is another approach to lowering the operating voltage. The operating voltage can be done by increasing the silicon surface roughness,[3] changing the doping concentration of polysilicon gates,[4,5] implanting fluorine into silicon before gate oxidation, and gate oxidation in NO or similar gases.[6] Thin fluorinated oxides have been investigated and found to have lower barrier height than silicon dioxide.[7] Fluorinated oxides have also been widely studied for their high resistance against ionized radiation and hot electrons.[2,8-10] Additionally, the nitrided oxide grown on F-implanted silicon was found to be able to suppress anomalous leakage currents.[11] Consequently, metal-oxide semiconductor field effect transistors (MOSFETs) fabricated with fluorinated oxides exhibit a decreased interface trap density. Moreover, fluorinated oxide interfaces are more resistant to hot carrier damage than thermal oxides. Several methods were proposed for fabricating oxide;[8-11] however, few methods are compatible with modern integrated circuit (IC) processes.

Plasma-containing fluorine has been extensively used in ultralarge-scale integrated (ULSI) technology. Fluorinated oxides exhibit high resistance against ionized radiation and hot carriers.[10,12] Recently, the authors reported a simple fabrication process to grow fluorinated oxides with a high tunneling current and low leakage current.[13] This study investigates the electrical and physical characteristics of MOSFETs with this fluorinated oxide, pretreated with CF_4 plasma.

Experimental

Metal oxide semiconductor (MOS) capacitors and n-channel MOSFETs with fabricated oxides were constructed. First, p-type (100) wafers with sheet resistance of 15-20 Ω-cm underwent RCA cleaning and were then treated with CF_4 plasma in a plasma-enhanced chemical vapor deposition (PECVD) chamber at 300°C and a pressure of 600 mTorr. The plasma treatment times were 1, 2, 3, and 5 min. The radio frequency (rf) power was set to 10 W. In contrast, the control sample was cleaned without CF_4 plasma treatment. Following the standard RCA cleaning, a thin oxide, with a thickness of 5.0 nm, was then grown on those wafers at 900°C in

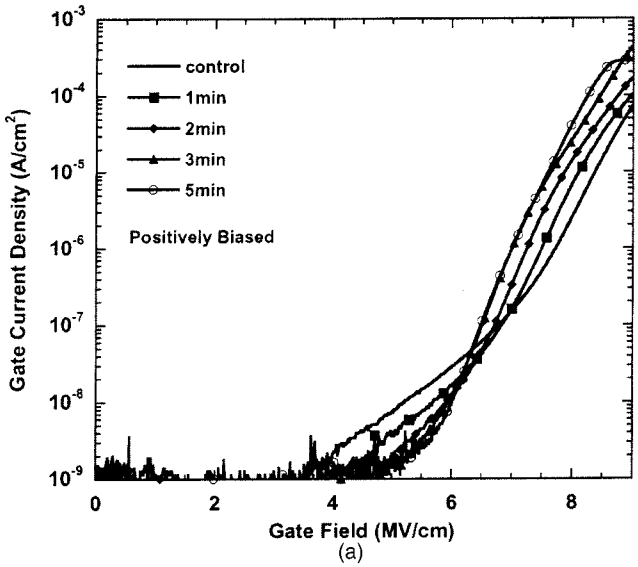

Figure 1. (a) Positive and (b) negative J-E characteristics of the five samples: samples were CF_4 plasma treated for 1, 2, 3, and 5 min, respectively.

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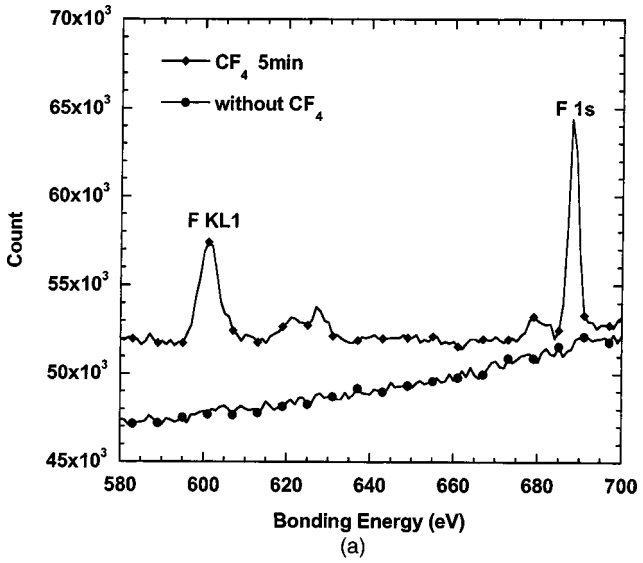


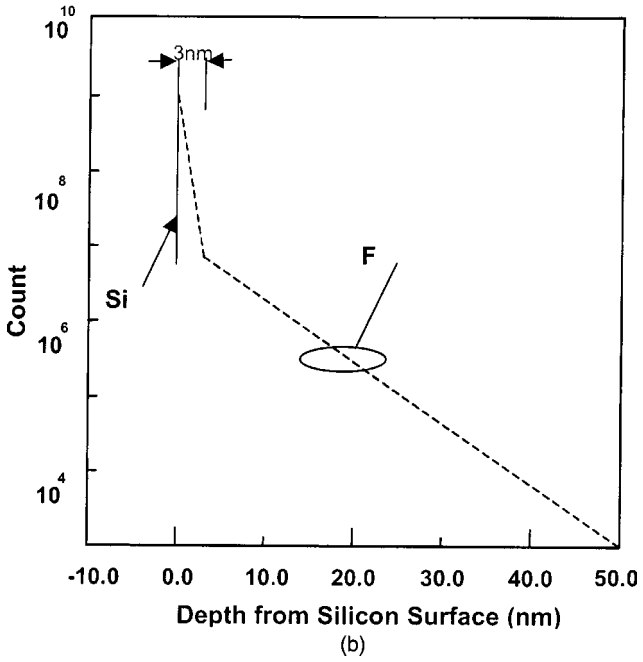


Figure 2. (a) XPS profiles of the control sample and CF_4-plasma-treated wafer. The treatment was at a power of 10 W for 5 min. (b) SIMS analysis of the silicon substrate treated by CF_4 plasma at 10 W for 5 min.

diluted O_2 ambient and annealed in N_2O at 900°C for 5 min. A 300 nm polysilicon film was then deposited. After the gate electrode was defined, gate, source, and drain were doped by phosphorous ion implantation. The substrate contact was doped by boron ion implantation. A rapid thermal anneal (RTA) process, lasting 30 s performed at 1000°C, was used for activation. Finally, contact holes were etched by reactive ion etching (RIE) and Al pads were also defined.

The electrical thickness of the oxide was determined by capacitance-voltage (C-V) measurement, and the physical thickness was characterized by using transmission electron microscopy (TEM). The current-voltage (I-V), leakage current, and reliability characteristics were measured using an HP 4156B. Fluorine incorporation was determined by secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS) analysis.

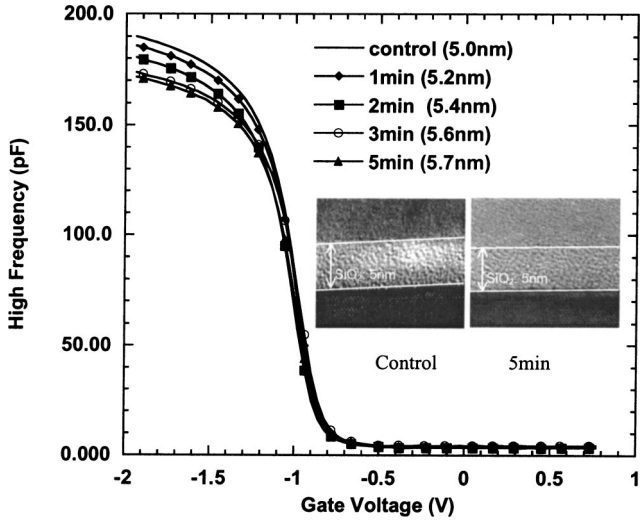
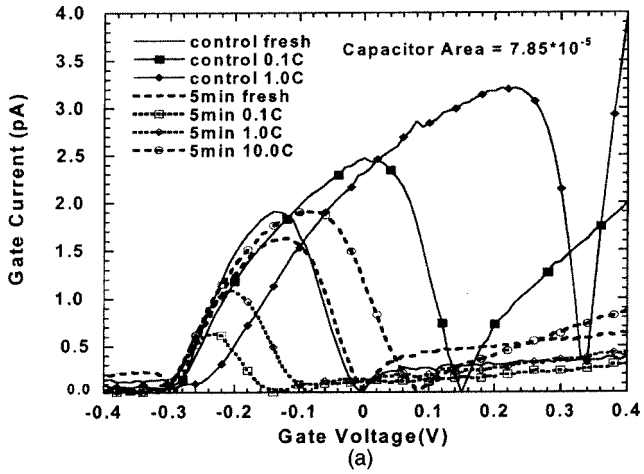


Figure 3. High-frequency C-V characteristics of the five samples: samples were CF_4 plasma treated for 1, 2, 3, and 5 min, respectively.



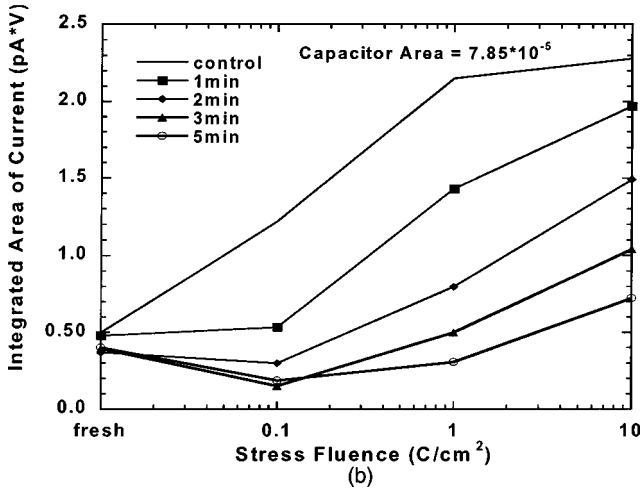
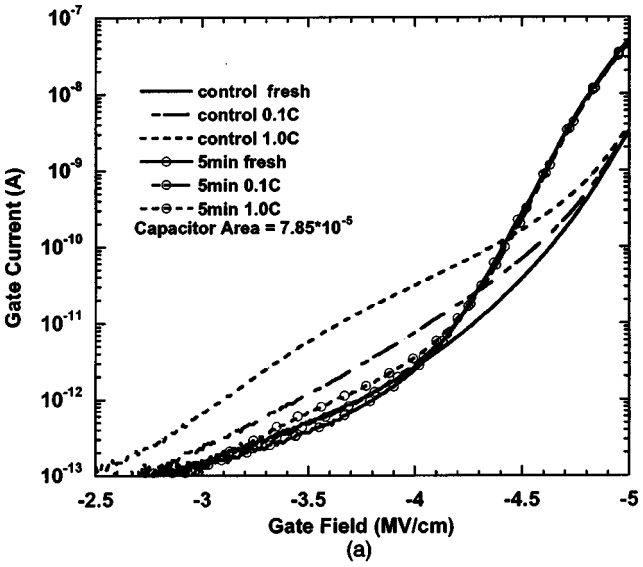


Figure 4. (a) Characteristics of anomalous leakage current of the control sample and the 5 min samples, and (b) the integral of the area from $V_g = -0.5$ to 0.5 V: $\Sigma(\Delta V I_g)$ under the curve of the anomalous current of the five samples. Samples 0.1, 1.0, and 10.0 C were stressed at 0.1, 1.0, and 10.0 C/cm^2, respectively.



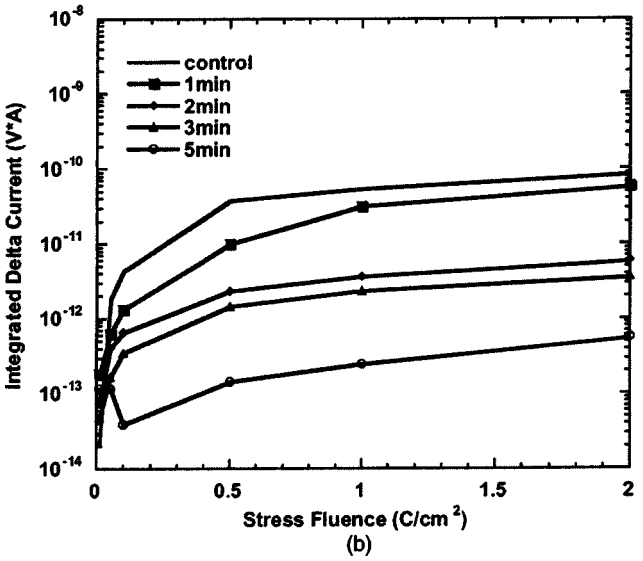


Figure 5. (a) SILC characteristics of the control and 5 min samples and (b) the integral of the area of the ΔI_g from V_g = 1-3 V; that is: $\Sigma(\Delta V(I_g\text{-}I_{go})$, where the I_g is the measured oxide leakage current and I_{go} is the leakage current of the fresh samples.

Results and Discussion

Figure 1 shows the *J*-*E* characteristics of the samples with different process times under (a) positive and (b) negative gate voltages. The symbols indicate samples treated with CF_4 plasma treatment for 1, 2, 3, and 5 min. The tunneling current of the oxide increases with the treatment time. The tunneling current was especially high for the 5 min sample with the negative gate bias. The tunneling current of the 5 min sample was found to be about three orders of magnitude higher than that of the control sample, due to the lower barrier height of the gate oxide after CF_4 pretreatment.[14] Under positive gate bias, the leakage current in the low-electric-field (4-6 MV/cm) region decreases as the plasma treatment time increases. The improvement was attributed to the fluorine incorporation at the SiO_2/Si interface, resulting in Si-F bond formation. Thus, the leakage current in the low-electric-field regime was suppressed because the Si-F bonds could passivate the defects and the dangling

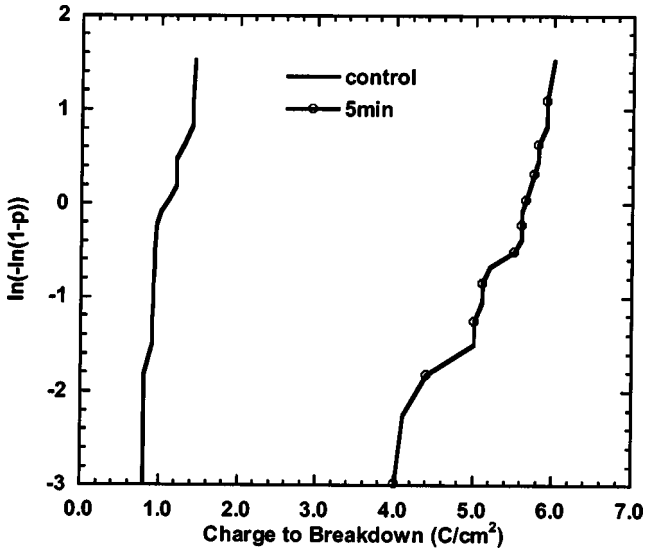


Figure 6. Weibull distribution plots of the Q_{bd} of the control and 5 min samples.

bonds in the oxides.[11,12,15] In the high-electric-field region, the higher tunneling current is also the result of a lower barrier height of the SiOF layer.

Both the control and the samples that were CF_4 plasma-treated for 5 min were analyzed by XPS, as shown in Fig. 2a, to elucidate the effect of the CF_4 plasma treatment. Strong signals associated with fluorine bonds were detected. However, no fluorine signals were observed in the control sample. Therefore, fluorine is indeed incorporated into the silicon substrate during CF_4 plasma treatment. The location of the fluorine incorporated during plasma treatment was discerned by SIMS. Figure 2b shows the SIMS depth profile of the silicon substrate treated by CF_4 plasma. The SIMS profile shows that fluorine atoms are located in a thin layer (about 3.0 nm) on the surface of the silicon wafer. That is, fluorine is confined in the SiO_2/Si interface region during oxidation. The SIMS analyses show that much density of fluorine was incorporated only at the interface, instead of in the substrate. This method is superior to the fluorine-implant method, which causes a high concentration of fluorine to be found in the channel region.

Figure 3 plots the high-frequency C-V curves of these five samples pretreated under different CF_4 treatment conditions. The symbols that represented different CF_4 plasma conditions are the same as those used previously. The samples pretreated with CF_4 plasma exhibited an increase in electrical thickness (that is, they have a lower capacitance). The 5 min sample had a 10% greater thickness than the control. Although fluorine has been reported to enhance the rate of oxidation by replacing Si-O bonds with Si-F bonds,[15,16] this did not occur in the samples considered here. In fact, the physical thickness of both the control and the treated samples observed by transmission electron microscope (TEM) are almost the same, as shown in the insert in Fig. 3. For a particular physical thickness, increase in the electrical thickness should reduce the dielectric constant, due to fluorine incorporation, as for the low-*k* material SiOF.

Figure 4a presents the characteristics of anomalous leakage current of the control sample and the 5 min pretreated sample. An additional CF_4 process was found to suppress the anomalous leakage current. Figure 4b shows the integral of the area from V_g = − 0.5 to 0.5 V: Σ (ΔVI_g) under the curve of the anomalous currents for the five samples. Samples were stressed at 0.1, 1.0, and 10.0 C/cm^2, respectively. The leakage current of 5 min CF_4 plasma-treated sample was lower than that of the control. After constant current stress, the leakage current of the control sample increased

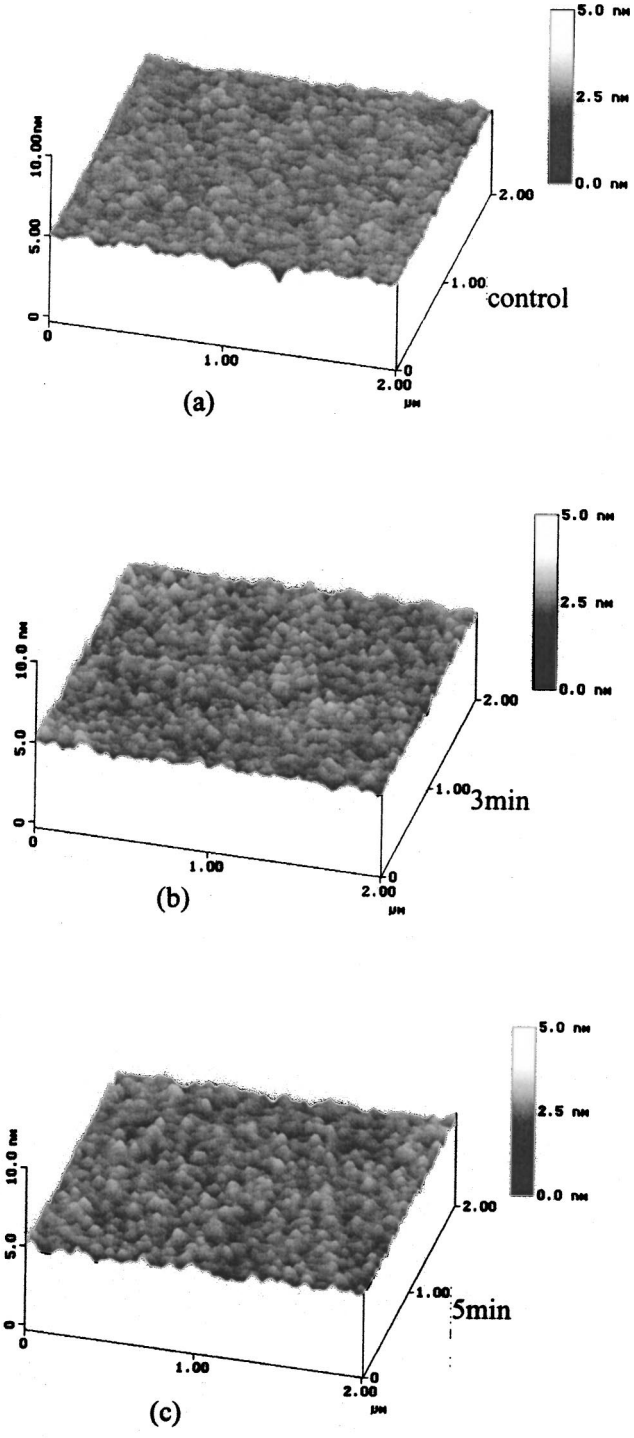


Figure 7. AFM images of the silicon substrate surface of the (a) nontreated sample, (b) sample treated with CF_4 for 3 min, and (c) sample treated with CF_4 for 5 min.

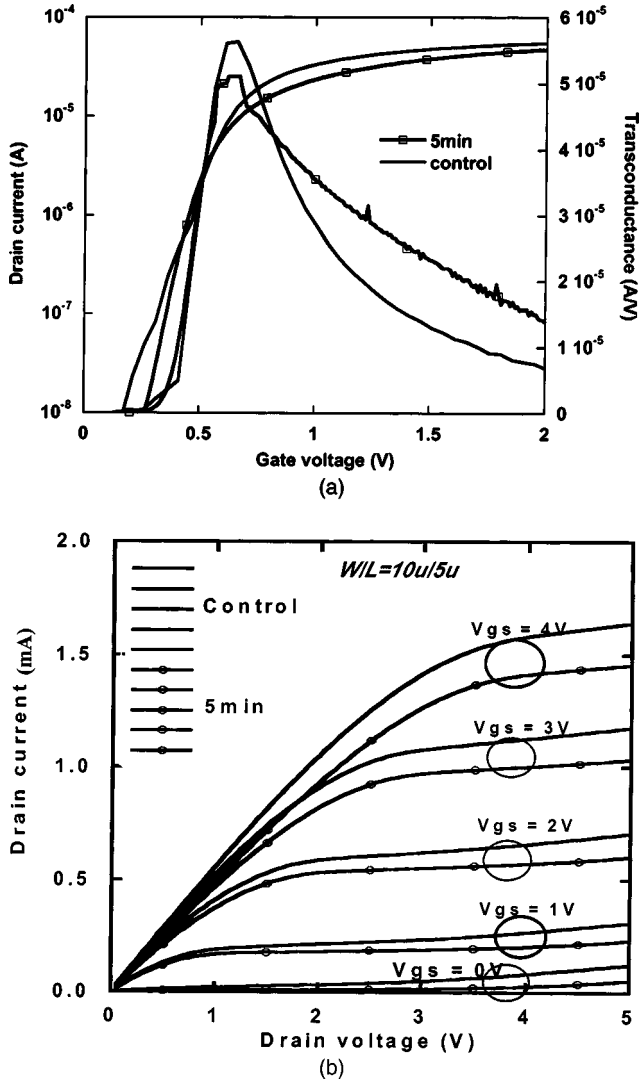


Figure 8. (a) Drain current *vs.* gate voltage curves and transconductance *vs.* gate voltage curves and (b) drain current *vs.* drain voltage curves of the control and the 5 min samples.

rapidly. However, the leakage current of the 5 min sample decreased in the first stage of stress and then increased slowly, not only in the case of the 5 min sample but also for all the pretreated samples. Briefly, the anomalous leakage current decreased as the CF_4 plasma treatment time increased. Incorporating fluorine into the oxide region significantly suppressed the anomalous current.

Figure 5a plots SILC characteristics for the control and 5 min samples. The 5 min sample has a higher resistance against stress-induced leakage current at a low electric field (3-6 MV/cm) than the control. Additionally, Fig. 5b shows the integral of the area under the curve of ΔI_g from V_g = 1-3 V, $\Sigma\,[\Delta V(I_g - I_{go})]$, where I_g is the measured oxide leakage current and I_{go} is the leakage current of the fresh samples. Clearly, oxides grown by CF_4 pretreatment are more resistant to constant current stress. This method can greatly improve the reliability of the EEPROMs. The improvement can be further enhanced with more fluorine incorporation. In fact, when measuring wafers at a constant current stress, a higher tunneling current of the oxide is another important factor affecting reliability.

Figure 6 shows the Weibull distribution plots of charge-to-breakdown (Q_{bd}) for the control and 5 min samples. Q_{bd} is a useful index of the quality of the oxides in EEPROM applications, since a high-density current tunnels through the oxides during programming and erasing. In this figure, the 5 min sample exhibits a higher Q_{bd} than the control. Stronger Si-F bonds are suggested perhaps to be able to effectively replace Si-H or Si-OH bonds and enhance the charge-to-breakdown performance. Consequently, the oxides grown on a CF_4-pretreated wafer are very promising as tunneling oxides in EEPROMs.

CF_4 plasma is commonly used for Si-etching applications. A rough surface degrades device performance. Atomic force micros-

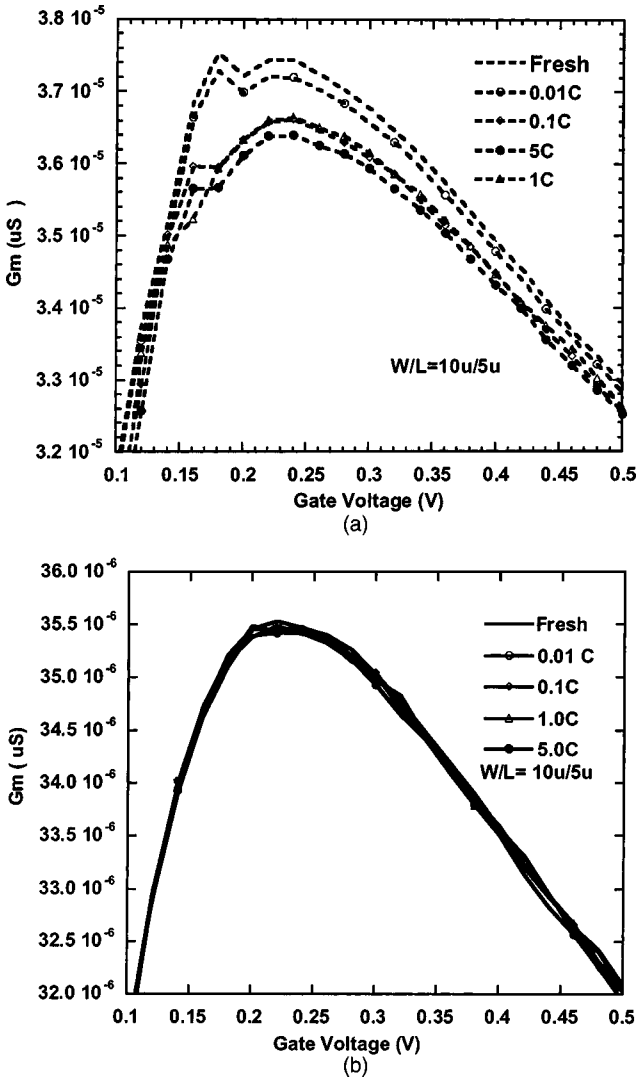


Figure 9. Degradation of the transconductance under constant current stress for (a) the control sample and (b) the 5 min sample.

copy (AFM) was used to obtain a surface image to investigate surface morphology. Figure 7 presents AFM images of the silicon substrate surface of the (a) nontreated sample, (b) the sample treated with CF_4 for 3 min, and (c) the sample treated with CF_4 for 5 min. The root-mean-square (rms) value of surface morphology for each sample was about 3-4 Å. Surface roughness does not significantly differ among these samples; therefore, surface roughening caused by the plasma treatment does not influence the differences among electrical characteristics.

Figure 8a plots the drain current and transconductance *vs.* the gate voltage of the control and the 5 min samples. A 10% decrease was found in the drain current and transconductance of the CF_4-pretreated sample. The C-V data showed that the capacitance decrement was also approximately 10%. That is, the degradation of the on current is proportional to the decrease of capacitance. According to the TEM images, only the *k* value differs, perhaps further indicating that the plasma pretreatment only slightly affects the channel mobility of the MOSFETs. Furthermore, our fabricated oxide (annealed in N_2O ambient) shows degraded maximum transconductance but improved high-field mobility.[17] These characteristics are similar to those of the reoxidized-nitrided oxide.[18] The reduction of the maximum transconductance was due to electron trapping. However, incorporating nitrogen can reduce acceptor-like interface states and improve the high-field mobility. The drain current *vs.* drain voltage curves of the control sample and the 5 min sample, shown in Fig. 8b, both exhibit the reduction of channel mobility, as mentioned previously.

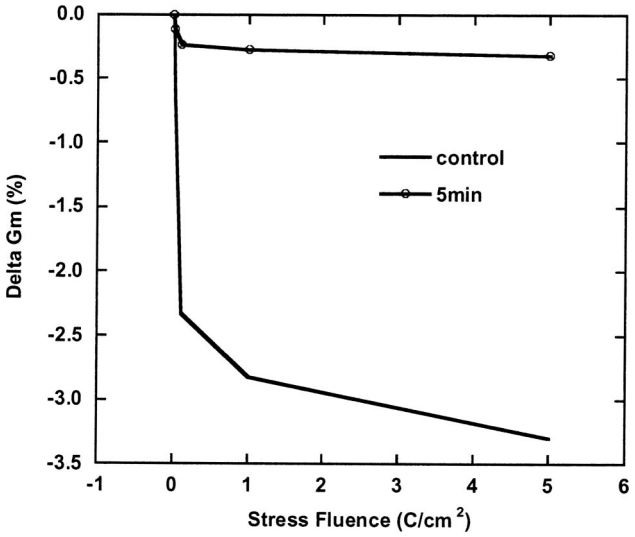


Figure 10. Delta transconductance *vs.* injected charge fluence curves of the control and 5 min samples.

Figure 9 exhibits the degradation of transconductance under different stress charges for (a) the control sample and (b) the 5 min sample. Hot-carrier stress conditions are measured by applying +10 mA from the gate, while the other electrodes are grounded. The control sample exhibits Gm degradation after hot carrier stress; however the Gm of the CF_4-pretreated sample shows little variation. Clearly, the CF_4-pretreated sample was better able to resist hot carrier stress than the control, perhaps because more fluorine was incorporated into the former.[2,14] Figure 10 compares the transconductance degradation in more detail. This figure shows the degradation of maximum transconductance. The transconductance degradation of the control sample was around 3%. That of the 5 min sample was only around 0.3%.

Conclusions

A thin tunneling oxide with superior electrical properties was proposed and fabricated using CF_4 plasma pretreatment. This method increases the fluorination of simply fabricated oxides, increases tunneling current, reduces leakage current, and increases resistance against both stress-induced anomalous leakage and low electric field (3-6 MV/cm) leakage currents. Furthermore, comparing the MOSFETs demonstrated that CF_4 plasma pretreatment could sustain similar channel mobility and yield much higher resistance against hot carrier stress. These excellent properties are very promising in fabricating low-voltage EEPROMs.

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