AIP | Applied Physics Letters

Solid phase epitaxy of amorphous Ge on Si in N 2 atmosphere

R. R. Lieten, S. Degroote, M. Leys, N. E. Posthuma, and G. Borghs

Citation: Applied Physics Letters **94**, 112113 (2009); doi: 10.1063/1.3098075
View online: http://dx.doi.org/10.1063/1.3098075
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/94/11?ver=pdfcov
Published by the AIP Publishing

APPLIED PHYSICS LETTERS **94**, 112113 (2009)

Solid phase epitaxy of amorphous Ge on Si in N_2 atmosphere

R. R. Lieten,[a] S. Degroote, M. Leys, N. E. Posthuma, and G. Borghs
IMEC, Kapeldreef 75, 3001 Leuven, Belgium

(Received 4 December 2008; accepted 20 February 2009; published online 20 March 2009)

We demonstrate a straightforward and economical way to obtain smooth germanium layers of high quality on silicon. Thin amorphous germanium layers deposited by plasma enhanced chemical vapor deposition on Si(111) substrates are transformed into single crystalline and smooth layers by solid phase epitaxy in N_2 atmosphere. The crystal orientation of the substrate has a clear influence on the crystal quality. This is most likely due to a different growth mode, namely, layer-by-layer for Si(111) and three-dimensional growth for Si(001). The amorphous germanium layer can roughen during annealing due to mobile atoms on the surface. This can be effectively suppressed by annealing in N_2 ambient. Electrical measurements show high charge mobility. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3098075]

Epitaxial Ge on Si is useful for extending conventional Si complementary metal-oxide-semiconductor (CMOS) circuits. Indeed it can be used to integrate fast Ge photodetectors and modulators on Si CMOS for optical interconnections.[1] Furthermore Ge shows only a small lattice mismatch with GaAs and can therefore be utilized as a virtual substrate for the integration of III-V devices on Si.[2] Ge(111) layers can also be used for epitaxial growth of III-nitrides.[3] Besides extending conventional Si electronics, epitaxial Ge on Si can enable the replacement of Si CMOS by Ge electronics for high performance applications. Ge transistors can be faster because of the higher charge mobility. Using bulk Ge substrates for CMOS is not feasible, as there is insufficient material available to cover the market needs.[4] However, by employing only a thin layer of Ge deposited on a suitable substrate, this problem can be avoided. An important advantage of using epitaxial growth of Ge on Si substrates is the scalability. Ge layers of larger diameter can be obtained by simply using larger Si substrates.

Epitaxial growth is mostly utilized to obtain a crystalline layer on top of another crystalline material. However, heteroepitaxial growth of Ge on Si is rather complicated because of the large mismatch of 4% between the two lattices.[5] This difference in lattice dimensions leads to island growth, causing high surface roughness and high density of threading dislocations in the Ge layer. For the growth of 200 nm Ge on standard Si(001) wafers by chemical vapor deposition (CVD) at 400 °C, a root mean square (RMS) surface roughness of ~ 25 nm for a $10 \times 10\ \mu m^2$ atomic force microscopy scan has been reported.[6] Additional annealing[6,7] or chemical-mechanical-polishing steps are often required to reduce the surface roughness. Obtaining high quality and smooth crystalline Ge, directly on Si, is therefore challenging.

Regarding the difficulties of Ge heteroepitaxy on Si substrates, we have looked into the possibilities of solid phase crystallization. This method is mainly used to obtain large polycrystalline layers on amorphous substrates[8] for low cost applications, such as thin film transistors.[9] In the case of solid phase epitaxy (SPE), a crystalline substrate is used to impose its structure onto an amorphous layer. In this way it is possible to obtain a single crystalline layer. Crystallization within the amorphous layer must be avoided during thermal annealing. Therefore it is important to deposit a highly disordered layer onto the crystalline substrate. However the deposition of such an amorphous layer is much more difficult on a crystalline substrate than on an amorphous one. SPE is extensively used to create epitaxial silicides on crystalline Si layers.[10] SPE of pure Ge on Si(111) substrates has been reported for layers of a few nanometers thick deposited in ultrahigh vacuum.[11] However this resulted in a non-planar surface.[11] The growth process of SPE of Ge on Si therefore seems similar to all other epitaxial growth techniques. Both epitaxy as SPE seem to be dominated by the problem of large lattice mismatch and show island growth leading to high surface roughness and high density of threading dislocations in the Ge layer.[11] Surfactants, deposited on the amorphous Ge, have been used to suppress island formation during SPE on Si.[12–14] Capping the amorphous Ge with a Si layer also suppresses island formation.[15] These measures reduce the surface diffusion of the Ge atoms, consequently suppressing roughening. We will show that SPE of Ge on Si can lead to smooth layers of high crystal quality without using surfactants or a capping layer.

A chemical deposition method was used for Ge deposition on Si substrates: plasma enhanced chemical vapor deposition (PECVD). The Si substrates were chemically cleaned to remove metal contamination, particles, and native oxide.[16] Immediately hereafter the samples were loaded into the deposition system. No additional annealing step was executed before deposition. Ge deposition by PECVD is done by cracking germane (GeH_4) molecules in a plasma source at a pressure of a few torr. As a consequence atomic hydrogen is present during deposition and will be incorporated into the Ge layer. In our experiments a mixture of 10% GeH_4 in H_2 is used. Amorphous Ge was deposited at temperatures between 150 and 270 °C, at a rate of 1.0 μm/h. After deposition the Ge layers were transferred to a different system and crystallized by thermal annealing at 600 °C for a few minutes. X-ray reflectivity (XRR) was used to measure the surface and Si-Ge interface roughness and the thickness of the deposited layer. The structural quality of the Ge layer was investigated by x-ray diffraction (XRD). Hall measurements were used to determine the electrical quality.

---

[a] Electronic mail: ruben.lieten@imec.be.

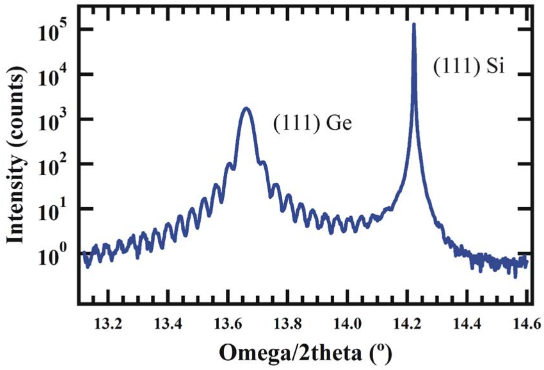

FIG. 1. (Color online) XRD $\omega/2\theta$ scan of 100 nm crystallized amorphous Ge on Si(111). An intense and narrow Ge (111) diffraction peak is observed, indicating high crystal quality. The presence of fringes indicates a smooth Ge surface and interface between Ge and Si.

In a first series of experiments Ge layers were deposited on Si(111) substrates and were thermally annealed at 600 °C in ultraclean N_2 atmosphere at atmospheric pressure. The resulted Ge layers are crystalline with the {111} crystal planes parallel to the {111} Si surface, as observed from $\omega/2\theta$ XRD scans, see Fig. 1. The Ge crystal quality is high. A XRD rocking curve scan of the Ge (111) diffraction peak showed a full width at half maximum (FWHM) of only 146 arc sec for 100 nm Ge. Fringes are visible in the $\omega/2\theta$ XRD scan of Fig. 1 indicating a smooth Ge surface and interface between Ge and Si. However when using a similar cleaning, deposition and annealing procedure for Si(001) substrates, a much broader and less intense XRD (004) peak was observed, see Fig. 2. From this experiment it is clear the crystal orientation of the Si surface has an important influence on the crystallization process. A difference in seed nucleation or seed growth related to the crystal orientation could be the reason for the difference in crystal quality. A difference in grain growth of amorphous Ge can be expected on Si(111) and Si(001) substrates as crystallization of amorphous Si is reported to be faster on Si(001) surfaces than on Si(111).[17] For this reason one could expect that crystallization of Ge on Si(111) proceeds layer-by-layer, whereas on Si(001) crystalline seeds will grow in an island growth mode. Layer-by-layer growth will lead to superior quality in respect with island growth, explaining the difference in crystal quality.

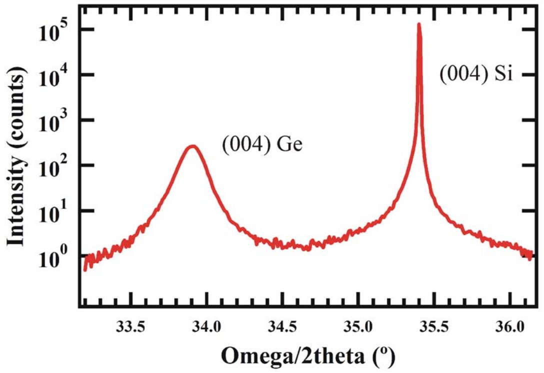

FIG. 2. (Color online) XRD $\omega/2\theta$ scan of 100 nm crystallized amorphous Ge on Si(001). A Ge (004) diffraction peak is observed, which is less intense and broader than the Ge (111) peak on Si(111). This indicates that crystallization on Si(001) leads to less good crystal quality than on Si(111).

We have investigated the crystallization of amorphous Ge layers deposited by PECVD with mass spectrometry and reflection high energy electron diffraction in ultrahigh vacuum. The release of hydrogen could be observed during the beginning of the crystallization process around 400 °C. This hydrogen originates from the breaking of Ge–H bonds inside the amorphous Ge layer during crystallization. The layers that were thermally annealed in vacuum at 600 °C however showed a rough surface, which is in agreement with other reports.[11,14] Our layers showed a RMS roughness larger than 2.5 nm, as measured with XRR. Much smoother layers were obtained for annealing in N_2 atmosphere at 600 °C. A RMS surface roughness of 0.7 nm was measured for 100 nm crystallized Ge on Si(111) by XRR. Therefore annealing in N_2 seems effective in keeping the surface atoms immobile during annealing and obtaining smooth layers. In this way the surface roughness after crystallization is comparable to the roughness of the as deposited layers. A possible explanation could be the formation of a few monolayers of Ge nitride during annealing, which protects the Ge layer from roughening. Such a layer is formed when exposing Ge to nitrogen plasma.[18] However no Ge nitride layer was observed by x-ray photoemission spectroscopy measurements for annealing in N_2 atmosphere at 600 °C. Therefore it seems that the Ge atoms are immobilized by collisions with N_2 molecules. The crystalline Ge layers that were annealed in N_2 atmosphere and in vacuum showed in both cases complete relaxation. This indicates that the surface roughening is not related to the relaxation of the Ge layer which exceeds the critical layer thickness, but to the Ge surface mobility. During annealing, when the Ge layer is not yet fully crystallized, Ge atoms at the surface can become mobile and cluster. This surface mobility should be limited during crystallization to keep the surface smooth.

Structural characterization of various samples has been carried out using high resolution XRD. The influence of the Ge thickness was investigated by preparing layers of 100, 50, 10, and 5 nm. For all these thicknesses the crystalline Ge layer was fully relaxed, as observed by XRD. This indicates that the lattice mismatch between Si and Ge is compensated by the introduction of dislocations in the first 5 nm. There does not seem to be an upper or lower limit in layer thickness for crystallization. The crystallization must start at the Si–Ge interface and then propagate to the Ge surface. Crystallization in the bulk, before the crystalline front has reached the surface must be avoided. This would lead to polycrystalline layers. Therefore, there is a limit on the speed of the temperature ramp and possibly on the total thickness of the Ge layer. The high crystal quality of our Ge layers indicates PECVD is well suited for depositing highly disordered layers. The limited roughness after crystallization in N_2 atmosphere indicates a layer-by-layer growth mode for SPE of Ge on Si(111).

Structural investigation by XRD shows the presence of Ge twins. This was observed by XRD phi scans of skew-symmetric reflections, a typical result is shown in Fig. 3. The (202) reflection was measured for different phi angles, corresponding with a rotation of the sample in the plane of growth. Two types of Ge diffraction peaks are observed: at the same phi angle as the Si diffraction peaks and in between the Si diffraction peaks. The latter Ge diffraction peaks originate from Ge that is 180° rotated in plane. Avoiding the formation of these twins would improve the crystal quality

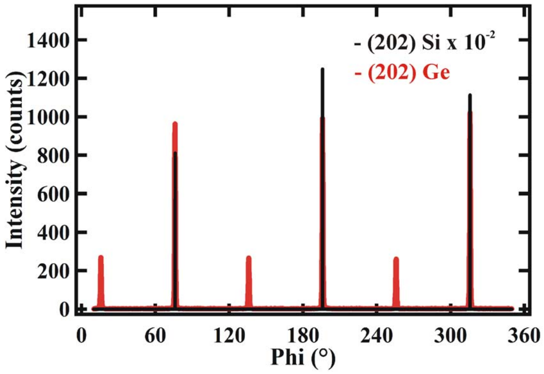

FIG. 3. (Color online) XRD phi scans of skew-symmetric reflections of Ge (202) and Si (202) from 100 nm Ge on Si(111). The Ge and Si scans are overlaid. The Si diffraction peaks are repeated every 120°, whereas the Ge diffraction peaks are repeated every 60°. The Ge diffraction peaks in between the Si diffraction peaks indicate the presence of Ge twins.

further. It has been reported that Ga atoms can induce the nucleation of twinned islands during epitaxial growth of Ge on Si(111).[19] Limiting the presence of impurities during Ge deposition therefore could help to reduce the number of twins in SPE of Ge on Si. Notwithstanding the presence of twinned Ge, excellent crystal quality was obtained as observed by XRD measurements.

The electrical quality of our layers has been investigated with Hall mobility measurements. During deposition of hydrogenated amorphous Ge by PECVD, dopants were introduced into the layer. Phosphine (PH_3) was used to incorporate phosphor for *n*-type doping and diborane (B_2H_6) to incorporate boron for *p*-type doping. In view of the good results of Ge crystallization on Si(111) substrates, 90 nm doped Ge layers were deposited on insulating Si(111). After crystallization at 600 °C in N_2 ambient, Hall measurements were performed. Unfortunately, mobilities of high carrier concentration are not available for Ge(111). Therefore we compare our data to reported values for Ge(001)[20] and Si(001)[21]. Our first results look promising. The electron and hole mobilities obtained are higher than for bulk Si(001) and lower than bulk Ge(001), see Table I. It can be expected that a thin Ge layer on a foreign substrate will show lower charge mobility with respect to bulk Ge, because of the presence of crystal defects and scattering at the interface. A reduction in defect density and twin formation will most likely improve the electrical quality further.

In summary, we have demonstrated a straightforward and economical way to obtain smooth Ge layers on Si, with excellent crystal and electrical properties. Amorphous Ge layers deposited by PECVD on Si(111) substrates are transformed into single crystalline and smooth layers by SPE in N_2 atmosphere. This high quality can be obtained for thin layers (≤ 100 nm). We showed that the crystallization conditions have a large influence on the surface quality. Above the critical thickness the amorphous Ge layer can roughen during annealing. This surface roughening is not related to the relaxation of the Ge layer but to the Ge surface mobility. N_2 ambient effectively suppresses surface roughening related to mobile Ge atoms during crystallization. Both *p*- and *n*-type doping can be achieved by introducing suitable doping gasses during deposition. The crystal orientation of the Si substrate has an important influence on the final result. Si surfaces of {111} orientation result in crystalline Ge of high quality. On Si(001) the results are less good. The high crystal quality and smooth Ge surface indicates a layer-by-layer growth mode for SPE of Ge on Si(111). The low deposition temperature and crystallization under N_2 atmosphere effectively keep the Si–Ge interface and Ge surface smooth. This is an important advantage of SPE of Ge in respect with heteroepitaxy. Hall measurements showed very good electrical properties: an electron mobility of 271 $cm^2/V\ s$ for 2.6×10^{18} e/cm^3 and a hole mobility of 149 $cm^2/V\ s$ for 5.4×10^{18} $holes/cm^3$.

TABLE I. Comparison of charge mobility for 90 nm crystallized Ge on Si(111) and bulk Ge(001) (Ref. 20) and Si(001) (Ref. 21) for electron and hole concentrations of, respectively, 2.6×10^{18} and 5.4×10^{18} cm^{-3}.

	Mobility ($cm^2/V\ s$)	
Layer	2.6×10^{18} (e/cm^3)	5.4×10^{18} (h/cm^3)
90 nm Ge on Si(111)	271	149
Bulk Ge(100)	550	350
Bulk Si(100)	150	80

[1] M. Oehme, J. Werner, E. Kasper, S. Klinger, and M. Berroth, Appl. Phys. Lett. **91**, 051108 (2007).

[2] R. P. Gale, J. C. C. Fan, B. Y. Tsaur, G. W. Turner, and F. M. Davis, IEEE Electron Device Lett. **2**, 169 (1981).

[3] R. R. Lieten, S. Degroote, K. Cheng, M. Leys, M. Kuijk, and G. Borghs, Appl. Phys. Lett. **89**, 252118 (2006).

[4] C. Claeys and E. Simoen, *Germanium-Based Technologies: From Materials to Devices*, 1st ed. (Elsevier, New York, 2007).

[5] J. Tersoff, Phys. Rev. B **43**, 9377 (1991).

[6] A. Nayfeh, C. O. Chui, K. C. Saraswat, and T. Yonehara, Appl. Phys. Lett. **85**, 2815 (2004).

[7] D. Choi, Y. S. Ge, J. S. Harris, J. Cagnon, and S. Stemmer, J. Cryst. Growth **310**, 4273 (2008).

[8] G. Harbeke, L. Krausbauer, E. F. Steigmeier, A. E. Widmer, H. F. Kappert, and G. Neugebauer, Appl. Phys. Lett. **42**, 249 (1983).

[9] T. P. Brody, IEEE Trans. Electron Devices **31**, 1614 (1984).

[10] K. E. Sundström, S. Petersson, and P. A. Tove, Phys. Status Solidi A **20**, 653 (1973).

[11] I. Suzumura, M. Okada, A. Muto, Y. Torige, H. Ikeda, A. Sakai, S. Zaima, and Y. Yasuda, Thin Solid Films **369**, 116 (2000).

[12] H. J. Osten, J. Klatt, G. Lippert, B. Dietrich, and E. Bugiel, Phys. Rev. Lett. **69**, 450 (1992).

[13] N. Aizawa, Y. Homma, and M. Tomita, Jpn. J. Appl. Phys., Part 1 **37**, 2460 (1998).

[14] T. Yamamoto, M. Ikeda, K. Ezoe, K. Ishii, and S. Matsumoto, Jpn. J. Appl. Phys., Part 1 **39**, 4545 (2000).

[15] P. M. J. Maree, K. Nakagawa, F. M. Mulders, J. F. Vanderveen, and K. L. Kavanagh, Surf. Sci. **191**, 305 (1987).

[16] M. Meuris, P. W. Mertens, A. Opdebeeck, H. F. Schmidt, M. Depas, G. Vereecke, M. M. Heyns, and A. Philipossian, Solid State Technol. **38**, 109 (1995).

[17] C. Spinella, S. Lombardo, and F. Priolo, J. Appl. Phys. **84**, 5383 (1998).

[18] R. R. Lieten, S. Degroote, M. Kuijk, and G. Borghs, Appl. Phys. Lett. **91**, 222110 (2007).

[19] J. Falta, M. Copel, F. K. Legoues, and R. M. Tromp, Appl. Phys. Lett. **62**, 2962 (1993).

[20] V. I. Fistul, M. I. Iglitsyn, and E. M. Omelyanovskii, Sov. Phys. Solid State **4**, 784 (1962); O. A. Golikova, B. Y. Moizhez, and L. S. Stilbans, *ibid.* **3**, 2259 (1962).

[21] C. Jacoboni, C. Canali, G. Ottaviani, and A. A. Quaranta, Solid-State Electron. **20**, 77 (1977).