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Simultaneous Switching Noise Minimization Technique Using Dual Layer Power Line Mutual Inductors*

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A novel technique for minimization of simultaneous switching noise is presented. Dual Layer Power Line (DLPL) structure is newly proposed for a possible silicon realization of a mutual inductor, with which an instant large current in the power line is half-divided flowing through two different, but closely coupled, layers in opposite directions. This mutual inductance between two power layers enables us to significantly minimize the switching noise. SPICE simulations show that with a mutual coupling coefficient higher than 0.8, the switching noise reduces by 63% compared to the previously reported solutions. This DLPL technique can also be applied to PCB artworks.

Keywords: Simultaneous switching noise; SSN; VLSI; Noise minimization; Output buffer; Dual Layer Power Line

1. INTRODUCTION

In today's CMOS VLSI, more and more high-density and high-speed I/O buffers are required to switch large number of drivers at the same time. As a result, simultaneous switching noise (SSN) or 'supply bouncing', which comes from a parasitic inductance of power lines, is also becoming significant [1–7]. The output pad buffers are the main contributors of the SSN because of large switching currents that change very fast flow through the parasitic inductance at the bonding wire and packages [1–2].

A typical output stage of a pad driver is shown in Figure 1. There are the parasitic inductor, resistor and capacitor along the power line, pad, bonding wire and pin package path. Generally, the parasitic resistor is neglected because it's comparably small [1]. In the worst scenario, if the peak magnitude of SSN exceeds the threshold voltage of the transistors, then it causes malfunction of the circuit. Therefore, it is necessary to estimate SSN

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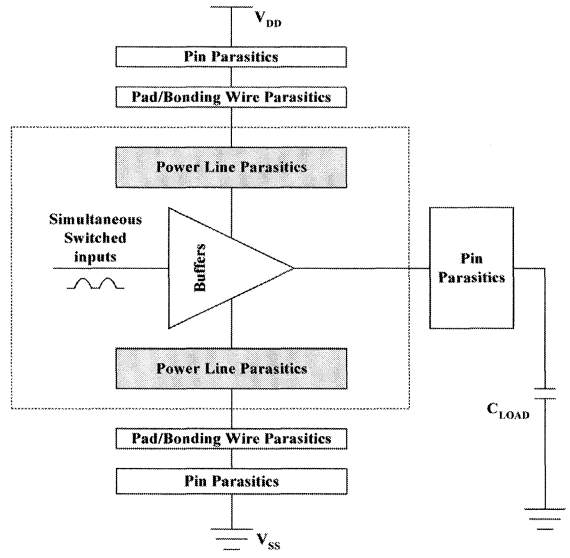

FIGURE 1 Typical output drivers and parastics.

more accurately and, more importantly, to minimize SSN in the output drivers [1, 2].

There have been a number of formulae proposed for modeling and minimizing the SSN [1–4]. Yang [1] and Jou [3] presented optimized output buffer circuit in constraint of SSN magnitude or transition time. Song [2] presented a new modeling for the SSN. Spurlin [4] proposed a serpentine transistor layout technique to reduce current variation with respect to time at cost of silicon area for extra switching circuits.

In this paper, we propose a new solution for the SSN, Dual Layer Power Line (DLPL) technique that can be implemented by adopting a simple power line strategy without causing any extra cost either in layer number or in silicon area. In Section 2, a brief description of the SSN is given and an analytical expression of the DLPL dynamics is derived. In Section 3, DLPL mutual inductor implementation technique on silicon is illustrated. Finally, conclusions along with future works are given in Section 4.

2. SSN MINIMIZATION THEORY

Figure 2 depicts two power line parasitic inductors of the typical CMOS output drivers. Suppose inputs V_{in} switch simultaneously, then a sudden current change will be induced in the power line generating the SSN.

The switching noise (V_n) at node A is defined as [1]

$$V_n = nL_{VSS}\frac{dI}{dt} \tag{1}$$

where n is the number of simultaneously switching drivers and I is the current flowing through one buffer. Here we only consider the V_{SS} power line case and the SSN of the V_{DD} can be explained in the same way.

Figure 3 shows the SPICE simulation of the SSN in Eq. (1). As can be seen the SSN peaks at t = 1 ns with the highest of 2 volts with n = 100 case. Note here the SSN level is considerably high enough to disrupt the chip function.

Basically, the proposed technique Dual Layer Power Line (DLPL) adopts well-known mutual inductor dynamics into power lines on silicon. Figure 4 shows the schematic of the DLPL with mutual inductors, here functionally same as transformers. L_{VSS} and L'_{VSS} represent primary and secondary inductors, respectively.

Figure 5 shows this mutual inductor model in the ground line. Power line (V_{DD}) can also be modeled in the same way and not dealt in this work. Here I represents a time-varying current in Eq. (1), which is same as i_S.

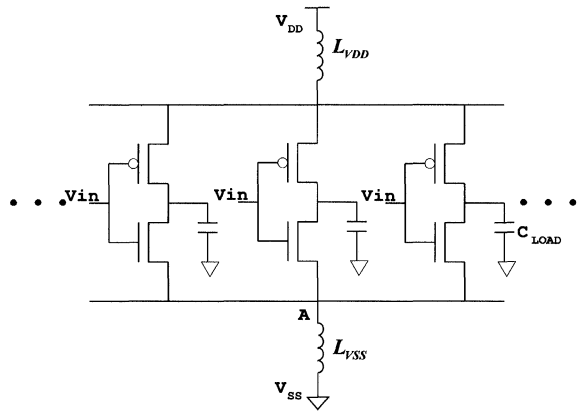

FIGURE 2 CMOS representation of the output drivers.

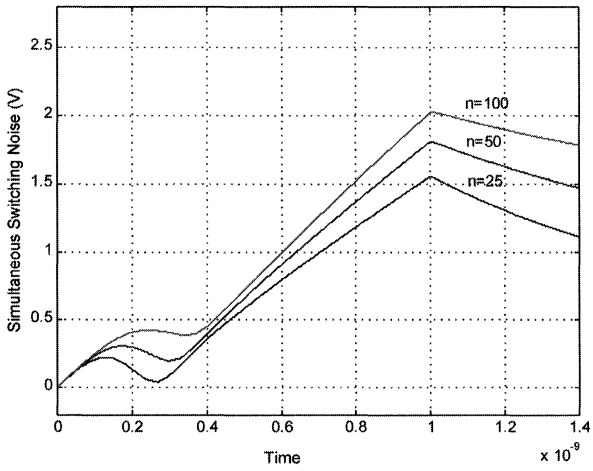

FIGURE 3 SSN simulation results with various driver numbers(n). ($V_{DD}=3.3$ V, 0.5 μm N-well CMOS, Pull-down NMOS: 325/1 μm).

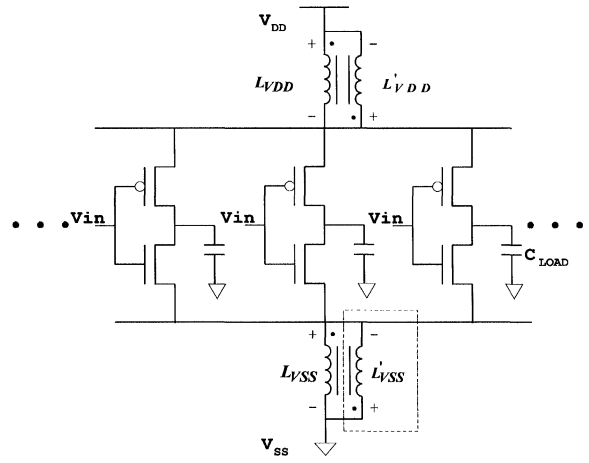

FIGURE 4 The proposed SSN minimization drivers with mutual inductors.

Two inductors, L_{VSS} and L'_{VSS}, are electromagnetically coupled being separated by a very thin insulator such as silicon-nitride or silicon-dioxide. In this scheme, we know that

$$V_n = L_{VSS}\frac{di_S}{dt} + M\frac{di_I}{dt} \tag{2}$$

$$V'_n = L'_{VSS}\frac{di_I}{dt} + M\frac{di_S}{dt} \tag{3}$$

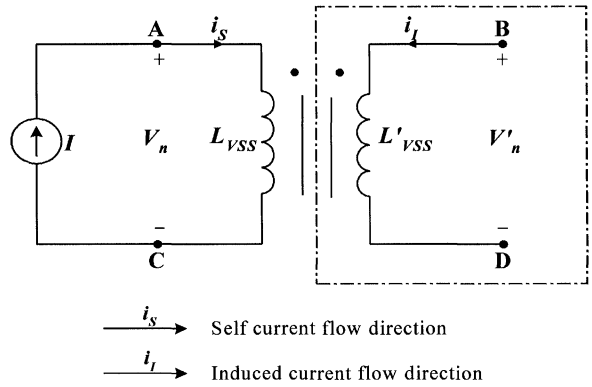

FIGURE 5 Mutual inductor model in the ground(V_{SS}) line.

The coupling coefficient, k, indicates the degree of coupling between two inductors, which is defined as,

$$k = \frac{M}{\sqrt{L_{VSS}L'_{VSS}}} \tag{4}$$

where M is mutual inductance [6]. If ideally, L_{VSS} and L'_{VSS} are perfectly coupled and same size, k equals 1. That means that Eq. (4) becomes

$$M \cong L_{VSS} = L'_{VSS}. \tag{5}$$

In Figure 5, if node A and node C connects with D and B, respectively, then we have $V_n = -V'_n$. Combining Eqs. (2) and (3) now yields,

$$V_n + V'_n = \left(L_{VSS}\frac{di_S}{dt} + M\frac{di_I}{dt}\right) + \left(L'_{VSS}\frac{di_I}{dt} + M\frac{di_S}{dt}\right) = 0 \tag{6}$$

Putting Eq. (5) into Eq. (6), we have

$$\frac{di_S}{dt} + \frac{di_I}{dt} = 0. \tag{7}$$

Therefore, i_I is to be $-i_S$, resulting, Eqs. (2) and (3) be as follows,

$$V_n = V'_n = 0 \tag{8}$$

So, when $k=1$, the SSN can theoretically be eliminated as an ideal case. In reality, however, k cannot be 'one', but we know this will minimize the SSN, V_n and V'_n.

In order to prove DLPL technique, SPICE simulations are used with a 150pF C_{LOAD}, 2nH inductance, and with 1ns rise time input. Figure 6 shows the SPICE simulation result, which is compared with [2] (noted as 'SONG') and 'SPICE' with a conventional power line scheme. As seen, about 63% SSN reduction was obtained.

Table I summarizes results comparing TI's solution [4] and DLPL (mutual inductor) method.

Figure 7 shows the cases of the values of k with 0.8, 0.9 and 0.999 for 36 drivers. 'SSN' in the figure presents the switching noise of conventional power scheme.

These mutual inductors, or transformers, in power lines are very easily realized by dual layer power line (DLPL) technique, that will be explained in the following Section 3.

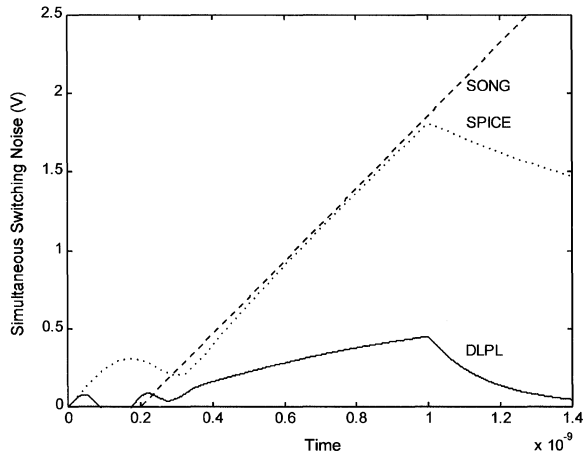

FIGURE 6 Comparison of natural SSN and DLPL SSN with 50 drivers. (VDD = 3.3 V, k = 0.9, 0.5 μm CMOS, Driver size: 325/1 μm).

TABLE I Comparison of TI's solution [4] and DLPL

	No. of Drivers		Vn, max(V)
TI's solution (C_{LOAD} = 50pF)	36		0.9
DLPL (C_{LOAD} = 150pF)	36	$k=0.999$	0.018
		$k=0.8$	0.796

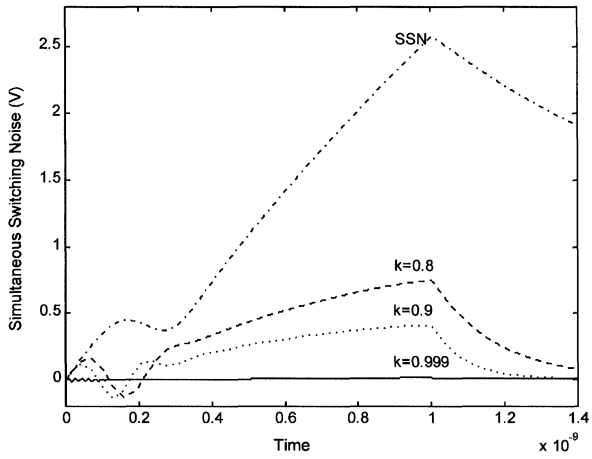

FIGURE 7 Minimized SSN simulation results according to coefficient k.

3. DUAL LAYER POWER LINE MUTUAL INDUCTOR

Figure 8(a) shows geometrical power line structure for the DLPL mutual inductor, and Figure 8(b) depicts lateral view of the DLPL.

It consists of two stacked power lines. Insulator such as silicon-dioxide, silicon-nitride or others (larger dielectric material is preferable for a larger k) fills the space between DLPL. It was reported in [7] that with a reasonably feasible thin insulator thickness in current CMOS technology, the coupling coefficient, k can be increased more than 0.88.

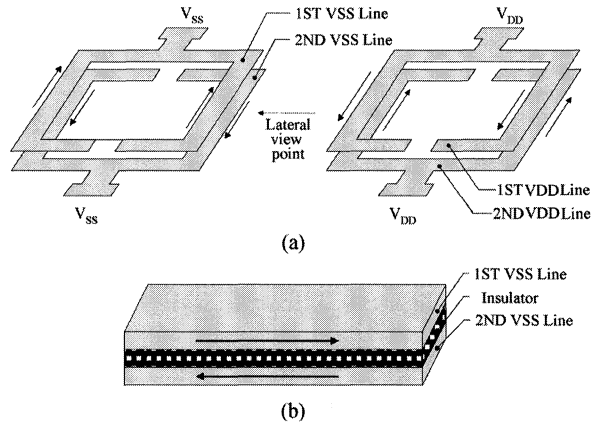

FIGURE 8 (a) Dual layer power line(DLPL) mutual inductor for V_{SS} and V_{DD} and (b) lateral view of the DLPL.

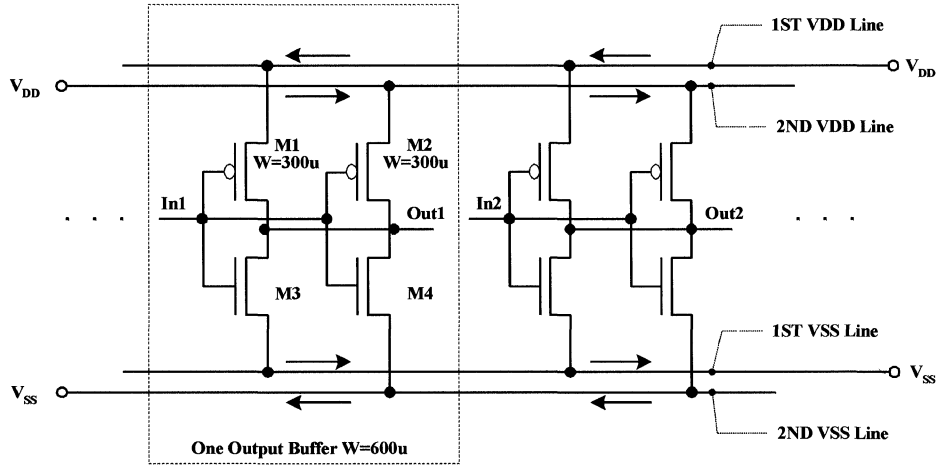

FIGURE 9 The proposed output driver structure with DLPL for mutual inductors.

For DLPL structure, there is no need to use special fabrication process. This DLPL is realized by a standard CMOS double metal process. Using a double metal process it should not be too difficult to make dual layer mutual inductors.

In order to realize this mutual inductor composed by DLPL, we need to apply a new power line strategy as shown in Figure 9. Drivers are divided, thus without any size overload, in two same half-sized buffers. Such as, dotted box in the Figure 9 corresponds to one buffer with channel width $W = 600\,\mu m$ that is composed of two same-sized $W = 300\,\mu m$ buffers. Here, one power line is connected at "1ST Line" and the other is connected at "2ND Line" of the DLPL.

Now, the buffer composed of two half-sized small buffers handles two opposite-direction instant currents of same amount at the same time. Here we assume probability density functions of switchings, at individual buffers of the dual power lines, are same, which is reasonably acceptable with a large number of I/O drivers in current high-speed digital logic. This is because SSN only occurs when many output buffers are simultaneously switching. Therefore, with our assumption, we can apply that two currents in DLPL are almost same with only opposite direction, satisfying Eq. (7).

One driver layout using the proposed DLPL is shown in Figure 10. Notice here that this structure occupies the same size as the typical conventional driver.

In Figure 10, sources of transistor M1 and M2 (or M3 and M4) are connected to metal 1 and

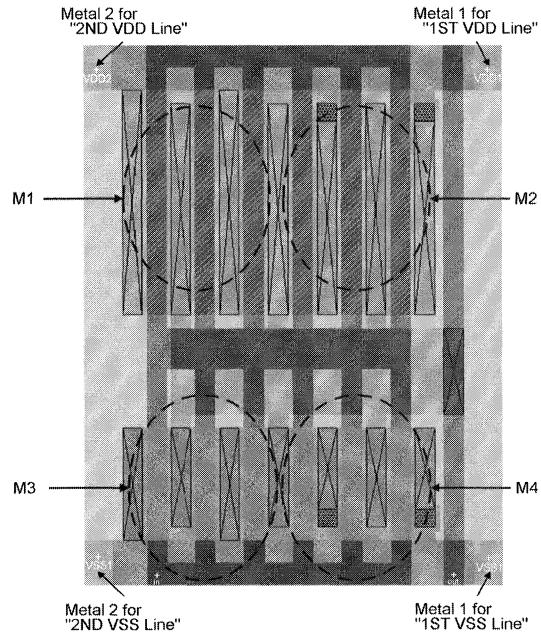

FIGURE 10 Driver layout with proposed DLPL technique.

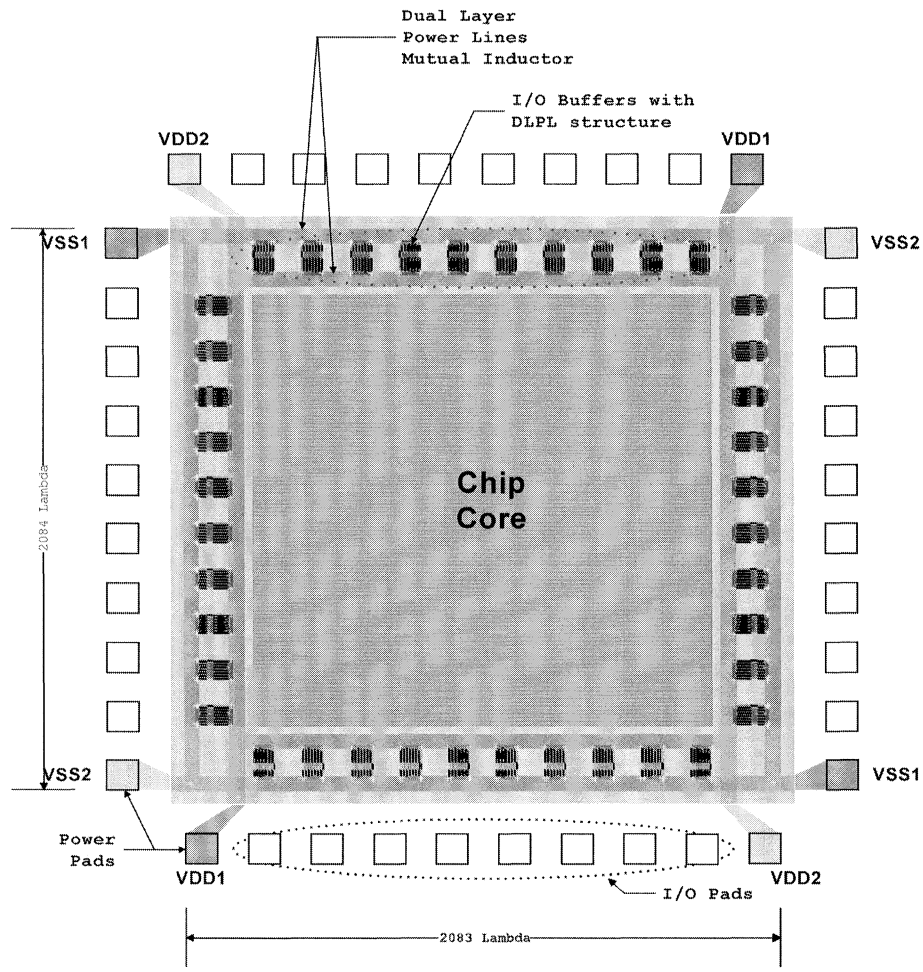

FIGURE 11 Overall view DLPL structure for the two metal processes.

metal 2, respectively. All gates and drains of M1, M2, M3 and M4 are connected.

One simple example for pad frame configuration is shown in Figure 11. Power pads are located at the corner of die. Each corner has one VDD and VSS pads that are separated using different metal lines.

4. CONCLUSIONS

A novel technique for minimization of simultaneous switching noise is presented. Dual Layer Power Line (DLPL) technique is newly proposed for a possible silicon realization of a mutual inductor, with which an instant large current in the power line is half-divided flowing through two different, but closely coupled, layers in opposite directions. Although we still need to take into account of the stray effect of the pad, bonding wire and the pin in the package, this technique gives us a new perspective of minimizing the SSN from an IC designer's point of view. This mutual inductance between two power layers enables us to significantly minimize the switching noise without overload of silicon estate. SPICE simulations show that with a mutual coupling coefficient higher than 0.8, the switching noise reduces more than 63%

compared to the previously reported solutions. Notice that this technique can also be adopted for the PCB power line art-works. Layout for the DLPL technique and test from silicon are under way. Research works are currently on going and more works will be included in the final paper.

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Authors' Biographies

Yongha Lee received the B.S. and M.S. degrees from Hallym University of Chunchon, Korea, in 1998 and 2000, respectively. He is currently a Ph.D. candidate at the same university. From 1997 to 1999 he worked at SETRI Microsystems, Seoul, Korea, on ASIC design for 220 Mbps Viterbi decoder in 155 Mbps Satellite Modem. His research interests include VLSI design of high-speed modem, RF integrated circuits, minimization technique of simultaneous switching noise, and security system.

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Gyu Moon received the B.S. degree from the Seoul National University, Korea in 1982. He then received M.S. and D.Sc. in electrical engineering degree from the George Washington University, Washington, DC, in 1990 and 1993, respectively. From 1982 to 1988 he worked for the Electronics and Telecommunications Research Institute, Korea, as a member of technical staff in the fields of VLSI Design/CAD. Since 1993, he has been with Hallym University, Korea where he is currently an Associate Professor in the Division of Information and Telecommunications Engineering. He is also serving, from 1998 to present, as Director of Information and Electronics Engineering Research Center at Hallym University. He has held visiting appointments in Ohio State University, USA, and Western Australia University, Australia. In 1998, he also worked for Micrys Inc., Ohio, USA as a General Manager, in developing various mixed mode ASIC chips.

Jeomkeun Kim received the B.S., M.S. and Ph.D. degrees in electrical engineering from Seoul National University, Korea, in 1982, 1986 and 1992, respectively. From 1992 to 1994 he worked for Samsung Electronics Co., Korea, as a senior research manager in the fields of Hard Disk Drive. Since 1994, he has been with Hallym University, Korea, where he is currently an Associate Professor in the Division of Information and Telecommunications Engineering. His current research interests are mechatronics, control application to industries and analog/digital VLSI design.