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Single-electron effects in side-gated point contacts fabricated in low-temperature deposited nanocrystalline silicon films

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Single-electron effects have been observed up to 60 K in a side-gated point contact device fabricated in nanocrystalline silicon films. The films were phosphorus-doped and deposited at 300 °C by plasma enhanced chemical vapor deposition. Using transmission electron microscopy and Raman spectroscopy, the grain size, crystalline volume fraction, and grain boundary thickness are determined. The single-electron effects are associated with islands formed by crystalline silicon grains ~4 nm in size, isolated by amorphous silicon regions ~0.5 nm in thickness. The structural characteristics of the *nc*-Si film are correlated to the electrical behavior. The electrical transport mechanism at high temperatures is attributed to percolation conduction across a distribution of tunnel barriers with a maximum height of 40 meV. © *2001 American Institute of Physics.*
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Nanocrystalline silicon (*nc*-Si) is a chemically-tailored material where crystalline silicon grains <10 nm in size are embedded in an oxide or amorphous silicon matrix. These nanoscale grains can form isolated charging islands which show single-electron effects, raising the possibility of room temperature single-electron devices fabricated in silicon. Several large-area *nc*-Si devices have been demonstrated, such as the nanodot memory structure of Tiwari and co-workers[1] and the tunneling diode of He and co-workers.[2] An atomic force microscope has been used to characterize individual *nc*-Si grains embedded in SiO_2 by Fukuda and co-workers[3] and Otobe and co-workers.[4] Resonant tunneling and single-electron effects have been observed at room temperature in these systems.

Nc-Si can be prepared using a low-temperature plasma-enhanced chemical vapor deposition (PECVD)[5] process. Typically, a plasma of SiH_4 or SiF_4 at temperatures $\leqslant$300 °C is used. The *nc*-Si can be deposited on glass or silicon-on-insulator substrates for faster device operation and better electrical isolation. The low process temperature reduces fabrication costs and makes large-area fabrication easier. This raises the possibility of device applications such as quantum devices fabricated on flexible plastic sheets.

In this letter, we report the observation of single-electron effects up to a temperature of 60 K in an in-plane, side-gated, point contact device fabricated in phosphorous-doped *nc*-Si. Our *nc*-Si film is deposited by PECVD at 300 °C. We structurally characterize the *nc*-Si film and correlate this to the electrical characteristics. We attribute electron transport in our device to a thermally-assisted single-electron tunneling process in the low-temperature range and percolation conduction through a distribution of barriers heights in the high-temperature range.

We prepared 30 nm thick *nc*-Si films using very high frequency (VHF) PECVD from a SiF_4:H_2:SiH_4 gas mixture. The films were deposited on a 150 nm thick silicon oxide layer thermally grown on top of *n*-type crystalline silicon. The flow rates of the SiF_4, H_2, and SiH_4 were 30, 40 and 0.25 sccm. The films were doped *in situ* with PH_3 (1% diluted with H_2) where the concentration of PH_3 in SiH_4 was 2%. The VHF frequency was 100 MHz, the VHF power was 40 W and the reactor pressure was 200 mTorr. The carrier concentration and electron mobility, measured at room temperature by Hall measurements, were $3\times10^{20}\,cm^3$ and 1.8 cm^2/Vs, respectively.

Our silicon point contact structures were defined using electron-beam lithography in polymethyl methacrylate resist and reactive-ion etching in a mixture of $SiCl_4$ and CF_4 gases (20 sccm each) at 13.56 MHz, 300 W, and 20 mTorr. The point contact has a width of 20 nm. Ohmic contacts were formed to the structure by first wet etching the surface oxide on the *nc*-Si film in SILOX (Laporte proprietary chemical) and then depositing aluminum contact pads. Figure 1 shows

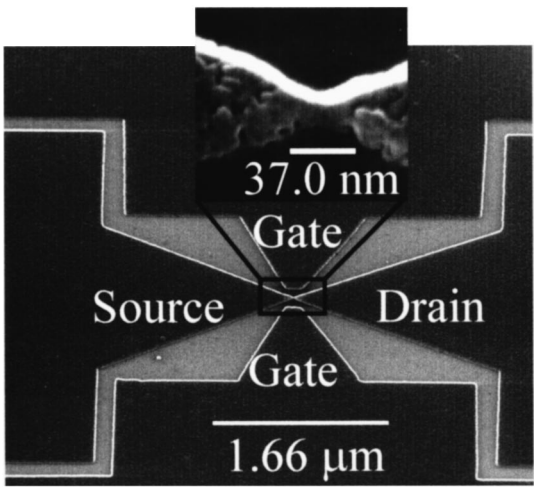

FIG. 1. Scanning electron micrograph of the side-gated point contact device. The inset shows an enlarged view of the source–drain point contact.

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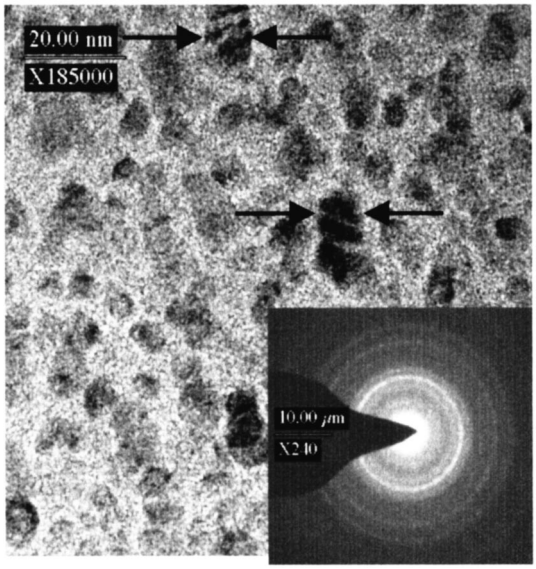

FIG. 2. TEM planar image of *nc*-Si. The arrows indicate examples of twinning in the grain structure.

a scanning electron micrograph of the structure.

We have characterized the structure of the *nc*-Si films using transmission electron microscopy (TEM). We used a Philips CM 300 FEG with an accelerating voltage of 300 kV. Figure 2 shows a TEM image of uniformly distributed *nc*-Si grains embedded in an amorphous silicon matrix. The grain sizes range from 4–8 nm. The diffraction rings shown in the inset demonstrate that the film contains crystalline silicon and not entirely amorphous. Additional high-resolution TEM analysis using Fresnel contrast indicated that the grain boundaries were decorated with fine layers of amorphous silicon less than 1 nm thick.

We have also characterized the structure of the *nc*-Si films with Raman spectroscopy, using an argon–ion beam with an excitation wavelength of 514.5 nm. The film structure was analyzed[6–8] by fitting the Raman spectra with a combination of the correlation length model for the crystalline silicon peak at $\sim 521\ \mathrm{cm}^{-1}$ and a Gaussian function for the amorphous silicon peak at $\sim 480\ \mathrm{cm}^{-1}$. The results demonstrated that the average grain size in the *nc*-Si film is 4 nm and the crystalline volume fraction is 70%. Assuming spherical *nc*-Si grains with a radius of 2 nm, uniformly encapsulated by an amorphous silicon layer of thickness D, we estimate $D=0.25\,\mathrm{nm}$ from the crystalline volume fraction of 70%. Therefore, the average thickness of the grain boundary region is $d=2D=0.5\,\mathrm{nm}$.

We have electrically characterized the point contact devices at temperatures ranging from 4.2 to 300 K. Figure 3(a) shows the drain–source current–voltage ($I_{ds}-V_{ds}$) characteristics of the device at 8 K as the gate voltage V_{gs} is varied from -2 to 2 V in 50 mV steps. A Coulomb gap V_C, strongly modulated by V_{gs}, is observed at low V_{ds}. The maximum width of V_C is $\sim$40 mV. Periodic peaks separated by $\sim$20 mV are observed in the differential conductance characteristic (not shown). A nonlinearity in the $I_{ds}-V_{ds}$ characteristics corresponding to the Coulomb gap is observed up to a temperature 70 K.

Figure 3(b) shows oscillations in I_{ds} as V_{gs} is swept from -1 to 1 V and V_{ds} is varied from -44 to -4 mV and from

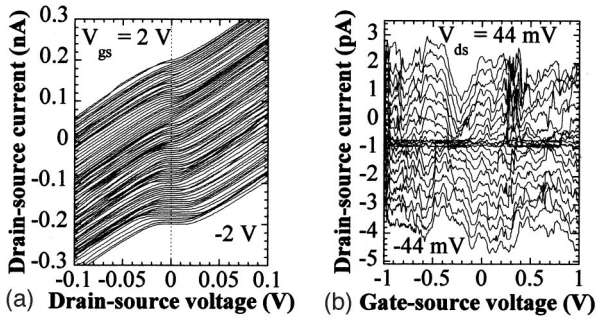

FIG. 3. (a) $I_{ds}-V_{ds}$ characteristics at 8 K. V_{gs} is varied from -2 to 2 V in steps of 50 mV. Each $I-V$ curve is displaced by 20 pA for clarity. (b) $I_{ds}-V_{gs}$ characteristic at 4.2 K. V_{ds} is varied from -44 to 44 mV in steps of 4 mV.

4 to 44 mV in 4 mV steps. A dominant oscillation with smaller superimposed peaks is seen in the characteristics. A Fast Fourier Transform of the characteristics indicates a period ΔV_g of 500 mV for the dominant oscillation and periods of 100 and 60 mV for the superimposed minor oscillations. This behavior can be attributed to single-electron conductance oscillations in a multiple tunnel junction (MTJs).[9] Each oscillation is associated with a charging island in the MTJ and a corresponding island—gate capacitance $C_g=e/\Delta V_g$ (Ref. 10) can be extracted. The island—gate capacitances corresponding to the three oscillation periods are 0.3 aF, 1.6 aF, and 2.7 aF, respectively. There exist switching effects at $V_{gs}\sim 200-400\,\mathrm{mV}$ which may be associated with defect states near the charging islands. We have observed the conductance oscillations at temperatures up to 60 K. The minor oscillations disappear at lower temperatures then the dominant oscillation, which persists up to 60 K.

We can estimate the minimum size of the charging islands from the oscillations periods. Assuming equal tunneling capacitances $C_1=C_2=C$ along the conducting path across each island,[10] the total capacitance of the island $C_\Sigma=2C+C_g$. The temperature at which an oscillation disappears may be used to estimate the total charging energy of each associated charging island using $E_C=e^2/(2C_\Sigma)\approx 3k_BT$ (Ref. 11) and larger oscillation periods imply a smaller island–gate capacitance. The dominant oscillation of 500 mV disappears at 60 K and can be associated with an island with $E_C\sim 15\,\mathrm{meV}$, $C_\Sigma\sim 5.3\,\mathrm{aF}$, and $C=(C_\Sigma-C_g)/2=2.5\,\mathrm{aF}$. Assuming that C is a simple parallel plate capacitor where the plate separation is equal to the amorphous silicon tunnel barrier width $d\sim 0.5\,\mathrm{nm}$ (estimated earlier from the volume fraction) and ignoring any depletion regions on either side of the amorphous silicon region, the island size is $\sim$4 nm. This is in good agreement with the grain size obtained from TEM analysis and Raman spectroscopy. Similarly, we can obtain island sizes for the minor oscillations periods. The 100 mV oscillations disappear at $\sim$20 K and the 60 mV oscillations disappear at $\sim$6 K. For these oscillations, $C_\Sigma\approx 15\,\mathrm{aF}$ and 52 aF and the island size is $\sim$6.4 nm and 12 nm, respectively. The TEM analysis indicated some twinning of grains and this is likely to form larger coupled islands.

Figure 4 shows an Arrhenius plot of the conductance of the device as a function of inverse temperature. The device conductivity σ is measured at a bias of $V_{ds}=50\,\mathrm{mV}$ (circles) and at zero bias (triangles). For the measurement at V_{ds}

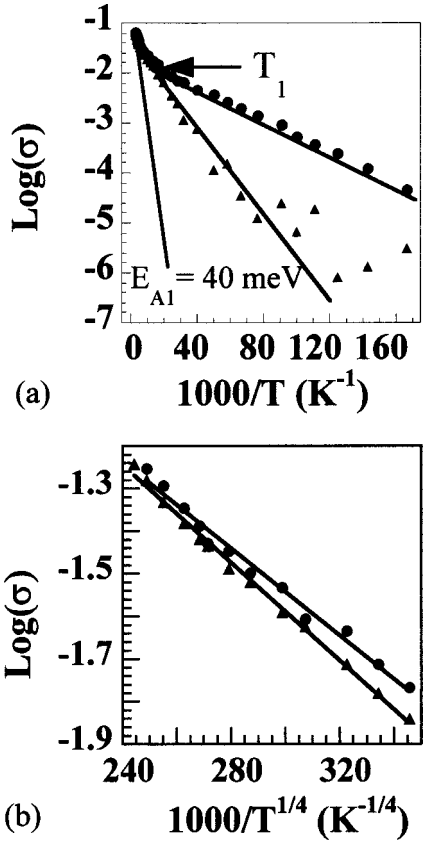

FIG. 4. (a) Arrhenius plot of V_{ds} biased at 50 mV (circles) and at zero biased (triangles). T_1 indicates the transition temperature, ~60 K, and E_{A1} is the maximum gradient obtained from the region for 60 K<temperature <300 K, as indicated by the first solid line. The second and third solid line shows the T^{-1} dependence. (b) For 60 K<temperature<300 K, the results follow a $T^{-1/4}$ dependence as shown by the solid lines.

$=50\,\mathrm{mV}$, the device operates outside the Coulomb gap. From 6 K to a transition temperature $T_1 \sim 60\,\mathrm{K}$, $\log(\sigma)$ follows a T^{-1} dependence and above T_1, $\log(\sigma)$ follows a $T^{-1/4}$ dependence. In the region of the $T^{-1/4}$ dependence, the conduction mechanism is likely to be dominated by percolation conduction through a distribution of potential barrier heights with various activation energies.[12] The maximum gradient obtained from the region of $T^{-1/4}$ dependence corresponds to an activation energy $E_{A1} \sim 40\,\mathrm{meV}$, which can be associated with the maximum height of the amorphous silicon tunnel barrier in the *nc*-Si. The region of T^{-1} dependence corresponds to a smaller activation energy $E_{A2} \sim 3\,\mathrm{meV}$. This value is too low for electronic confinement and we speculate that it corresponds to the difference between the Fermi level and conduction band edge in the *nc*-Si grains. Electron transport in this temperature range is controlled by a thermally-assisted tunneling process.[2]

For σ measured at zero V_{ds}, the device operates within the Coulomb gap. At temperatures above T_1, the behavior is similar to that measured at $V_{ds}=50\,\mathrm{mV}$. This is because the Coulomb gap in the device disappears at $\sim T_1$ and the zero bias conductivity is similar to the conductivity at $V_{ds}=50\,\mathrm{mV}$. Below T_1, there again exists a T^{-1} dependence. However, the activation energy $E_{A3} \sim 10\,\mathrm{meV}$ is larger. This energy is close to the Coulomb charging energy ~15 meV obtained for the dominant island from the gate oscillations of Fig. 3(b).

The variation in the amorphous silicon tunnel barrier height may be explained by considering the dopant distribution in the *nc*-Si film. A *nc*-Si grain of 4 nm diameter contains on average thirty phosphorous atoms while a 0.5 nm thick amorphous silicon grain boundary contains on average only six phosphorous atoms. This implies that the grain boundaries would be strongly influenced by any fluctuation in the doping concentration, leading to a variation in the energy difference between the conduction band edge and the Fermi level in the amorphous silicon, and a variation in the depletion width at the crystalline silicon/amorphous silicon interface. We note that if the tunnel barrier on average is 40 meV high and 0.5 nm wide, the tunnel resistance is ~10 kΩ, which is less than the quantum resistance $R_K=25.8\,\mathrm{k\Omega}$ and Coulomb blockade effects are not possible.[11] However, in our measurements there must be a wider than average grain boundary because of statistical fluctuations in the grain boundary width together with additional depletion regions on either side. This would create a wider tunnel barrier with a higher tunnel resistance, for example if the barrier is 40 meV high and 2 nm wide, the tunnel resistance is $\sim 10R_K$ and Coulomb blockade effects would occur.

We have also fabricated up to 60 nm wide devices which exhibit a maximum tunnel barrier height from 16–22 meV. In these devices a larger number of percolation paths may exist for electron transport and a lower tunnel barrier height is more likely observed. Even in the point contact device of Fig. 4, the maximum barrier height of 40 meV is relatively low for electronic confinement at higher temperatures closer to room temperature. At temperatures $>T_1$, single-electron effects disappear and there is a transition to percolation conduction.

In conclusion, we have observed single-electron effects in *nc*-Si point contacts up to a temperature of 60 K. We have shown that the charging islands are *nc*-Si grains as small as ~4 nm, isolated by amorphous silicon regions ~0.5 nm thick. Electron transport is attributed to a thermally assisted single-electron tunneling process at low temperature and percolation conduction at high temperature. Our work is funded by the Japan Science and Technology Agency CREST program.

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