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Controlled formation of individually seeded, electrically addressable silicon nanowire arrays for device integration

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The formation of large-scale arrays of individually seeded, electrically addressable Si nanowires with controlled dimension, placement, and orientation is demonstrated. Electron beam evaporated gold nanoparticles were used for nanowire synthesis. By controlling the lithography and metal deposition conditions, nanowire arrays with narrow size distributions have been achieved. Low-energy postgrowth ion beam treatment has been utilized to control the orientation of Si nanowires. This process also leads to the attachment of nanowires on the substrate. Fabrication of planar devices with robust metal contact formation becomes feasible. The method enables efficient and economical integration of nanowires into device architectures for various applications. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2398900]

Semiconductor nanowires and nanotubes represent an important class of nanostructured materials with potential to impact applications from nanoscale electronics to biotechnology. Field effect transistors based on silicon nanowires (SiNWs) and carbon nanotubes have been demonstrated as good candidates for ultrasensitive, miniaturized molecule sensors.[1–3] Because of the high surface-to-volume ratio of the nanostructures, their electronic characteristics may be sensitive enough to a very small amount of charge transfer such that single molecule detection becomes possible.[1]

The vapor-liquid-solid (VLS) growth mechanism[4] is an ideal synthetic technique in the gas phase to produce nanowires with high crystalline quality required for sensing applications. Superior performance based on individual SiNW devices has been demonstrated.[1] However, devices have been constructed around single or several dispersed SiNWs. For practical applications, efficient and precise manipulation and placement of nanowires at desired locations need to be established to allow the integration with microfluidics and complementary-metal-oxide semiconductor (CMOS) circuits.

Most of the existing fabrication methods for nanowire devices utilize nanometer-scale colloidal catalyst particles. It is important, yet challenging, to control the placement of these particles with the precision required to form large-scale arrays. As a result, postgrowth flow-directed and electric-field assisted assembly techniques have been proposed and demonstrated.[5,6] However, such approaches may not be suitable for nanowires with small diameters. Alternatively, controlled growth of SiNWs in predetermined configurations has been demonstrated using Si (111) as substrate.[7,8] Patterned depositions of the gold seeds led to confinement of the vertical nanowire growth to selected regions. However, formation of metal contact remains challenging for such device configuration.

In this letter, a pathway to fabricating large scale, high-density nanowire arrays using standard semiconductor processes is described. SiNWs with controlled dimensions and specific placement were produced by the conventional chemical vapor deposition via the VLS process. Postgrowth ion-beam alignment process was employed to control the orientation of nanowires. This process provides a simple yet reliable method for enhanced control over the placement and handling of one-dimensional nanostructures. As a result, integration of nanowires with various device architectures can be realized.

The fabrication process begins with a doped Si wafer with 160 nm thermal oxide. Electron-beam lithography (EBL) and electron-beam evaporation were utilized to define the location of catalyst. An array of Au nanodisks with diameter of ~40 nm and thickness of ~10 nm is shown in Fig. 1. Such Au nanodisks were used as catalyst for mediating growth of silicon nanowire. The sizes of metal catalyst controlling the diameters of SiNWs can be tailored by the electron-beam lithography and metal deposition steps. It has been noticed that the edge of some of the Au naoparticles is rough and ill defined. This is likely related to imperfection in lithography/metal deposition/lift-off processes. The shape of Au nanoparticles could be improved by using e-beam lithography with better resolution and metallization with better directionality.

The growth of SiNWs was carried out at temperatures between 450 and 550 °C using 2% disilane (Si_2H_6) in H_2 as a precursor and hydrogen as a carrier gas. Although the edge of the particles was not well defined, it did not appear to

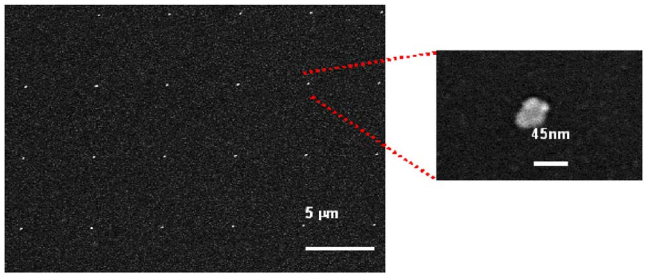

FIG. 1. (Color online) SEM images of an array of Au nanoparticles on SiO_2 surface prepared by e-beam lithography followed by e-beam evaporation of gold and lift-off.

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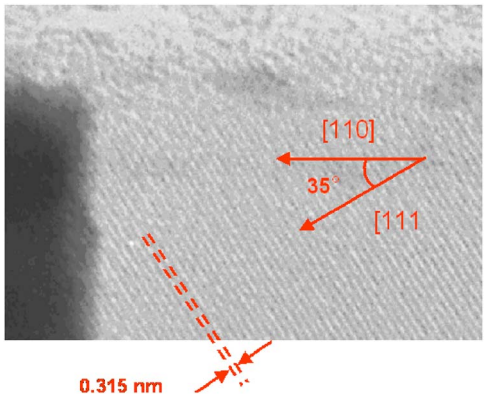

FIG. 2. (Color online) High-resolution TEM image of a Si nanowire showing [111] lattice fringes and ⟨111⟩ growth direction.

affect the growth of the nanowires under optimal process conditions. SiNWs with diameters ranged from 20 to 50 nm have been obtained by changing the parameters of metal deposition and e-beam lithography. With growth rate of about 0.2 μm/min, the length of SiNWs in the range of 1–5 μm can be tailored by controlling growth time. Extensive transmission electron microscopy characterization indicates that these wires are single crystalline in nature, as shown in Fig. 2.

It has been reported previously that SiNWs grown via VLS process using thin gold films deposited on plain substrates did not provide good diameters control of the resulting wires due to the randomness of the film breakup at growth temperatures.[9,10] Our results indicate that with optimized process and growth conditions, a single SiNW can be grown from each lithographically defined catalyst site, as shown in Fig. 3. Fabrication of large-scale arrays of SiNWs then becomes feasible. The diameter, position, and density of SiNWs can be controlled to create desired arrays through lithographic means. Nanowires can be grown with narrow size distributions approaching those of the seed particles, as determined by scanning electron microscopy (SEM). As an example, the diameter of SiNWs grown from Au nanodisks with ~40 nm is in the range of 40–50 nm (45±5 nm). Results indicated that most SiNWs grew straight, as shown in Fig. 3(c). Some SiNWs exhibited kinking. Kinking of SiNWs has been reported in the literature,[10,11] and is most likely related to the instability of liquid-solid interface between molten Au–Si alloy and a SiNW during the growth.

Unlike Si nanowires grown epitaxially on Si (111) substrate, due to lack of crystalline characteristics of the SiO_2 surface, the nanowires grown on SiO_2 surface are randomly oriented after growth, as shown in Fig. 3. For many applications, having the wires parallel to each other and possibly parallel to the substrate surface would aid fabrication. Accordingly, an ion beam irradiation process was employed to align the SiNWs in a desired manner.[12] At the present case, typical argon ion energy within the range of about 1–4 keV with a flux density of $\sim 6\times 10^{15}$ ions/cm^2 was applied. The treatment was performed at some angle to the substrate surface, typically within the range of about 10°–45°. It was found that effective alignments of nanowires with diameters ranging from 20 to 50 nm can be readily achieved with less than 30 s treatment. The attachment of nanowires to substrate surface after ion beam irradiation and the subsequent device fabrication process is verified by atomic force microscope (AFM) measurement. When similar conditions were used for sputter etching of thermally grown SiO_2, the thickness of SiO_2 sputter etched during a similar exposure to the ion beam was less than ~2 nm. Therefore, the alignment process using an ion beam should not significantly change the properties of the nanowires.

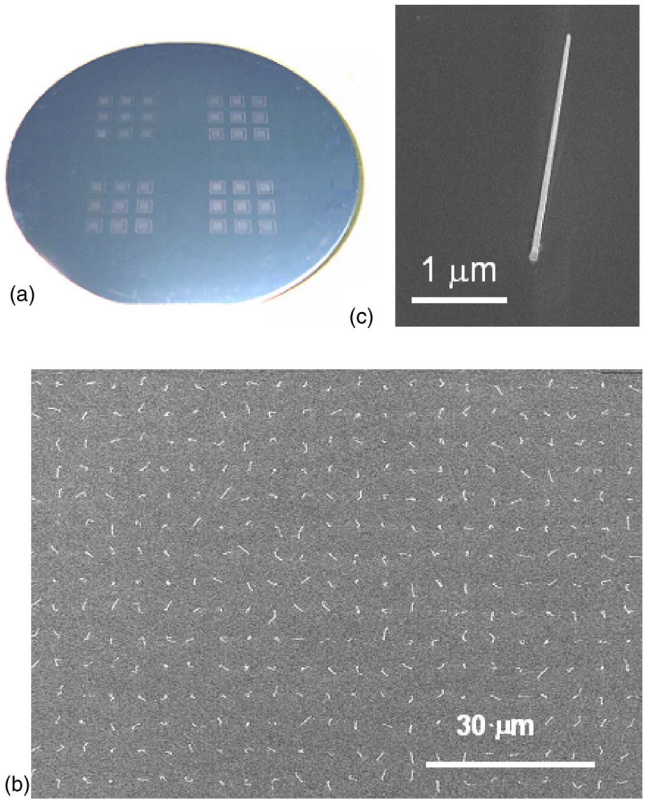

FIG. 3. (Color online) (a) Large-scale arrays of Si nanowires grown on a 3 in. e-beam patterned substrate. (b) Plan-view SEM image of an array of SiNWs grown over large area. (c) SEM image of a typical, single SiNW grown from a lithographically defined catalyst site.

Lastly, electrical contacts to the ends of SiNWs were made by defining pairs of electrodes using EBL and subsequent evaporation of contact metal and lift-off. Arrays of high density SiNWs with controlled orientation have been obtained. The SEM and AFM images of a connected SiNW between two metal contacts are shown in Fig. 4. Compared with a prior approach employing formation of vertically aligned Si nanowires relative to substrates, this method provides a route for the fabrication of planar devices with robust metal contact formation. A typical *I-V* characteristic of an electrically connected SiNW is shown in Fig. 5. The *I-V* characterization from devices without a connected wire indicate that the leakage current is negligible (less than picoamperes) after the growth and processing steps. The *I-V* characterization from devices with connected wires with diameter of 35–40 nm exhibits linear characteristics with resistivity of approximately 100 Ω cm, which is fairly consistent with the value for the nonintentionally doped Si. These experimental observations indicate that the deteriorate effects of postgrowth process, including ion-beam alignment and metal contact formation on the crystalline quality of nanowire, are negligible. We have also found the presence of thin amorphous layer on substrate surface when the growth was carried out in nonoptimized conditions. This amorphous layer can lead to an increase in leakage current. Therefore,

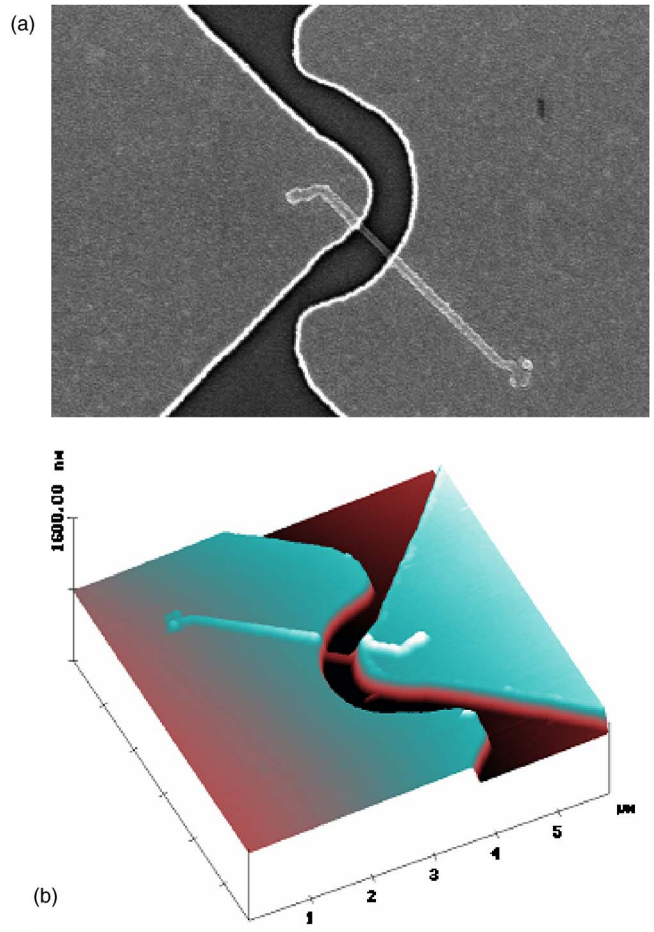

FIG. 4. (Color online) (a) SEM picture and (b) AFM picture of a connected SiNWs between two metal contacts.

growth parameters should be optimized to minimize noncatalytic deposition on SiO_2 surface.

In summary, a method of fabricating arrays of SiNWs with control over NW location, density, diameter, and orientation has been demonstrated. The method described herein, utilizing standard semiconductor fabrication processes, may serve as the basis for forming high density nanoscale sensors that can be integrated with microfluidics and CMOS driver circuits. Specifically, the implementation of postgrowth ion-beam alignment makes this process ideal for fabricating array of planar devices with robust metal contact formation.

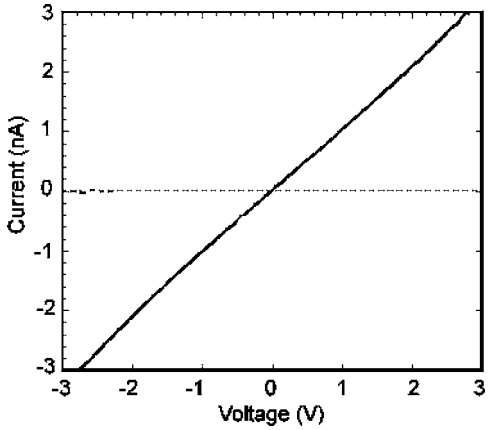

FIG. 5. *I-V* measurement of an electrically connected Si nanowire. Solid line: with a nanowire, and dotted line: without a nanowire.

Density of ion flux and impact energy of ionic species can be precisely controlled, which leads to a reproducible process, and can potentially offer high throughput for the fabrication of devices in large scale.

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