Journal of The Electrochemical Society, **148** (12) F207-F211 (2001)
0013-4651/2001/148(12)/F207/5/$7.00 © The Electrochemical Society, Inc.

Minimizing the Effects of Hardware Marginality on Charging Damage during Plasma-Enhanced Chemical Vapor Dielectric Deposition

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In this paper, Kelvin-probe measurements, antenna transistors, and electrically programmable read-only memory cells are used to minimize the influence of hardware marginality on charging damage during plasma-enhanced chemical vapor deposition of dielectric films. It is shown that charging during tetraethosiloxane (TEOS) deposition can be reduced by increasing the deposition pressure and optimizing the plasma ramp-down after deposition. It is also demonstrated that differences in the charging performance between tools from different vendors during the deposition of silicon-rich oxides can be smoothed out if a double radio frequency process replaces the traditional single radio frequency deposition.
 [DOI: 10.1149/1.1414289]

Manuscript received March 15, 2001. Available electronically November 2, 2001.

Plasma processes are widely used in microelectronic manufacturing for anisotropic etching, surface cleaning, and low-temperature plasma-enhanced chemical vapor deposition (PECVD) of thin films.[1] During plasma processing, wafers are subjected to the direct bombardment of ions, electrons, and photons. In uniform plasma the ion and electron conduction locally balance each other over the rf cycle.[2] In this case, the surface potential stays close to that of the substrate. In nonuniform plasma, however, the situation differs significantly. Ion and electron currents do not balance locally during the rf cycle, although there is a net balance over the electrode as a whole. In this case, charges (positive or negative depending on specific ratio between positive and negative currents) start to accumulate on the wafer regions covered by insulating films. The charge buildup continues until the electric field across gate oxides reaches values high enough to allow Fowler-Nordheim (FN) tunneling of charges. This causes what is usually called plasma charging damage, *i.e.*, trap formation, wear out, and premature breakdown of thin gate oxides. Moreover, it increases the probability of charge trapping in the oxide. As a consequence, shifts of the threshold voltage, leakage, degraded circuit speed, and deterioration of transistor matching may occur. As device dimensions and gate oxide thicknesses are scaled down, charging becomes an increasing reliability[3] or yield[4] concern. To limit charging damage, tight control of plasma uniformity and knowledge of the interaction among plasma, hardware, and process settings are mandatory.[5] In this paper, these issues are addressed by using fast-feedback noncontact Kelvin-probe measurements,[6] antenna transistors, and electrically programmable read-only memory cells (EPROM)[7] to measure charging during plasma-enhanced chemical vapor deposition of two materials widely used in microelectronic manufacturing for interlayer and intermetal insulation, tetraethosiloxane (or TEOS)[8] and the silicon-rich oxide (or SILOX).[9] In particular, the relation between plasma ramp-down, reactor architecture (single-wafer or batch), and charging is investigated. Possible ways to optimize the deposition process in order to minimize the influence of process-hardware marginality on charging are also discussed.

Experimental

Dielectric deposition.—TEOS deposition.—SiO_2 layers (500 nm thick) were deposited on 200 mm wafers using plasma-enhanced chemical vapor deposition (PECVD) by decomposition of tetraethosiloxane, $Si(OC_2H_5)_4$, better known as TEOS,[8] $Si(OC_2H_5)_4 + O_2 \rightarrow SiO_2 + CO + OH$. The deposition was carried out for 45 s at 400°C using an rf power of 675 W and a deposition pressure of 8 Torr. During deposition, the TEOS and O_2 flows were 1200 and 1000 sccm, respectively. Helium (1200 sccm) was used as a carrying gas. After deposition, a ramp-down step was performed using a $He + O_2$ plasma (5 s at 200 W, 8 Torr, 1200 sccm He, 1000 sccm O_2). Variants to the standard process were obtained varying the deposition pressure in the range from 5 to 15 Torr, the oxygen flow in the range 500 to 2000 sccm, the deposition temperature, and the TEOS flow. For all the variants, the thickness of the TEOS layer was 500 nm, *i.e.*, the same of the standard process.

SILOX deposition.—300 nm PECVD silicon-rich oxide films were deposited on 200 mm wafers. Prior to SILOX deposition, EPROM cells were fabricated on the same wafers using a 0.35 μm complementary metal oxide semiconductor (CMOS) technology. Deposition was carried out at a temperature of 400°C, a pressure of 2.5 Torr, an rf power of 250 W and using a $SiH_4 + N_2O$ gas chemistry. The deposition time was *ca.* 15 s. Unlike for TEOS films, after deposition the plasma was switched off without a $He + O_2$ plasma ramp-down. SILOX layers were deposited using either batch or single-wafer PECVD reactors. In the case of the batch reactor, the chamber allowed the deposition of six wafers at the same time. The SiH_4 flow was 130 and 300 sccm for the single-wafer and batch reactor, respectively. The N_2O flow was 800 sccm (single-wafer reactor) or 9500 sccm (batch reactor). In some cases, in addition to the 13.5 MHz rf power used to decompose the $SiH_4 + N_2O$ gas mixture and ignite the plasma, a low-frequency (10 kHz) rf power was applied to the wafer susceptor to enhance the ion bombardment on the as-deposited film. Double rf recipes are used in microelectronic manufacturing because the ion bombardment improves the quality (stability and density) of the insulating layers.[10]

Charging measurements.—Kelvin probe.—During PECVD deposition of insulating layers, charges may accumulate in the bulk as well as on the surface of the wafer if the plasma in unstable. These charges change the surface potential of the wafer. Therefore, a measurement of the wafer surface potential can be used to detect charging. In this work, the surface potential after PECVD TEOS deposition was measured using the Kelvin probe technique. The probe consists of a noncontact sensor that detects the ac signal induced by an oscillating shutter positioned between the electrode and the wafer surface. Measurements were carried out applying different dc biases across the sensing electrode and a grounded electrode until the ac voltage is reduced to zero. The bias at which the ac voltage is zero is equivalent to the wafer surface potential. A more detailed description of probe functioning can be found in Ref. 11. Kelvin probe measurements were performed using the plasma damage monitor system manufactured by Semiconductor Diagnostics, Inc. The distribution of the surface potential on the wafer was evaluated by measuring 6000 points per wafer.

Threshold voltage shift.—Surface potential measurements have been compared with threshold voltage measurements of n- and p-channel

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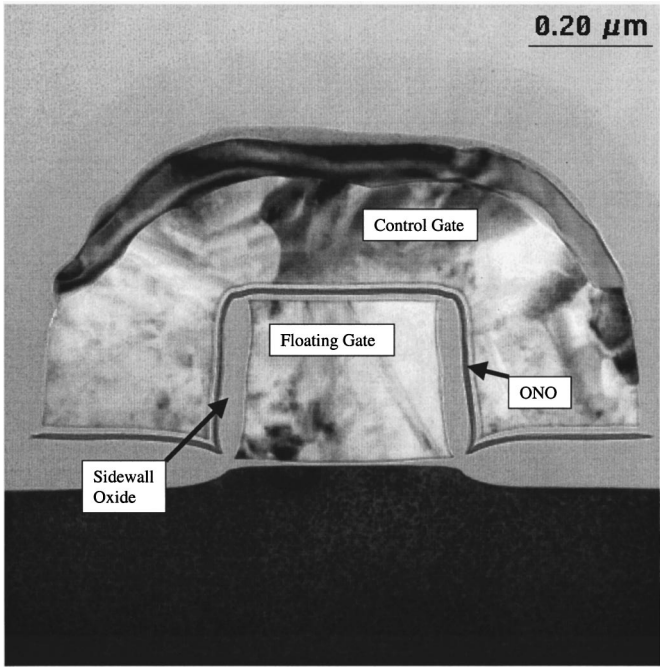

Figure 1. XTEM of the EPROM cell used in this work.

transistors connected to large metal or poly-Si antenna plates. The antenna improves charge collection during plasma exposure, thus increasing the FN current density in the gate oxide.[12] This amplifies the effect of charging on the transistor properties. In general, the larger the ratio is between the area of the antenna and the area of the MOS gate (the so-called antenna ratio), the higher the FN current and, consequently, the more affected the transistor is by charging.

The antenna transistors used in this work were fabricated in a standard three-metal 0.5 μm CMOS process. The antenna ratio for the transistors with antenna at poly-1, metal 1, or metal 2 was 550. The antenna ratio for the transistors with antenna at metal 3 was 1840. The severity of charging was estimated by calculating the total fraction of antenna transistors whose threshold voltage shifted (with respect to the threshold voltage of a reference transistor not connected to any antenna) more than a fixed value.

EPROM cells.—In addition to Kelvin probe and antenna transistors, charging was also studied by means of electrically programmable read-only memory (EPROM) cells processed in a 0.35 μm CMOS technology. The cells were n-channel devices with gate length, width, and oxide thickness of 0.35 μm, 0.5 μm, and 8 nm, respectively. The cross-sectional transmission electron microscopy (XTEM) of a typical cell is given in Fig. 1. The cell is formed by an insulated poly-Si layer (the floating gate, FG), completely overlapped by a second poly-Si layer (the control gate, CG). The FG is electrically insulated from the CG and the Si substrate by the 8 nm gate oxide, by the sidewall oxide, and by the oxide-nitride-oxide (ONO) stack (oxide equivalent thickness *ca.* 20 nm).

The principle of operation of the EPROM cell is similar to that of an ordinary MOS transistor. For a given potential difference between source and drain, the current flows only if the voltage applied to the CG is higher than the threshold voltage V_t. The difference with respect to an ordinary transistor is that the threshold voltage of an EPROM cell is controlled by the charges trapped in the FG.[7] This property makes the EPROM cells suitable for detect charging. In fact, if, because of charging, a voltage is applied to the control gate during, for example, deposition of SILOX or TEOS, the voltage across the gate oxide increases and electrons start tunneling from the silicon substrate into the floating gate, thus increasing the V_t of the EPROM cell. A simple measure of the threshold voltage of the

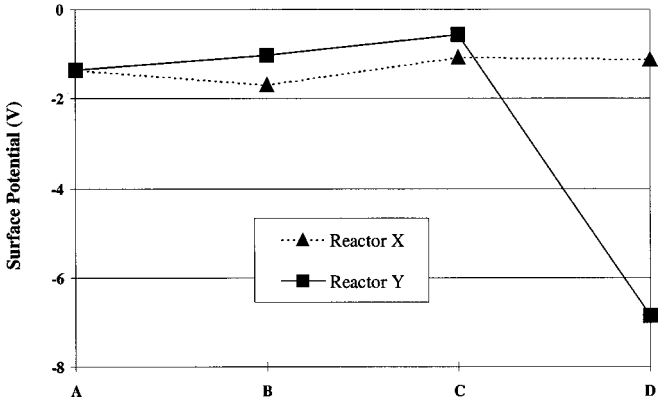

Figure 2. Average surface potential after 500 nm PECVD TEOS deposition carried out on each of the four chambers (A, B, C, D) of the two single-wafer PECVD reactors X and Y. Nine points were measured on each wafer.

EPROM cells after PECVD deposition then allows the estimation of the charging-induced voltage the cells have been exposed to. In this work the threshold voltage of the cell has been defined as the voltage that is necessary to apply to the control gate to measure at the drain a current of 1 μA when the potential difference between source and drain is $V_{ds} = 0.1$ V.

An important parameter for the capability of the EPROM cells to detect charging is the fraction of the voltage applied to the control gate that is coupled to the floating gate (the so-called coupling factor α). The higher the coupling factor, the higher the voltage across the oxide in the case of charging and, as a consequence, the more electrons can tunnel into the FG. The coupling factor for the cells considered in this work was 0.79 ± 0.4. This value is higher than that of conventional stacked-gate EPROM cells because the CG of the cell in Fig. 1 completely overlaps the FG.[13]

To study charging during PECVD deposition, the threshold voltage of the EPROM cells has been measured before and after erasure of the cells. Erasure has been achieved by illuminating the cells with UV light. During UV illumination, the energy necessary for the stored electrons to surmount the energy barriers surrounding the floating gate is provided by the UV photons.[14]

In addition to the threshold voltage of the standard cells, the V_t of a reference cell placed at a distance of 3 μm from the standard EPROM cell was also measured. In the reference cell the floating and control gates are shorted. This allowed the separation of threshold voltage shifts due to charges trapped in the floating gate from shifts due to wafer-to-wafer variations of the cell morphology (like oxide thickness or floating gate length variations).

Results and Discussion

TEOS deposition.—TEOS layers, 500 nm thick, were deposited on unpatterned Si wafers using the standard process. Deposition was performed on each of the four chambers (A, B, C, and D) of two different single-wafer PECVD reactors (X and Y). After deposition, Kelvin-probe measurements of the wafer surface potential were carried out. Results are shown in Fig. 2. The average surface potential, V_{Spave}, is $-2 \text{ V} < V_{SPave} < -1 \text{ V}$ for all the wafers of reactor X and for those processed in the chambers A, B, or C of the reactor Y. This value is close to the detection limit of the Kelvin-probe system (±1 V), indicating negligible charging during deposition. The situation is different for the wafer processed in chamber D of the reactor Y. In this case the absolute value of the surface potential is much higher (7 V), suggesting charging during deposition.

The influence on the anomalous behavior of chamber D of the plasma ramp-down step is investigated in Fig. 3. Four different ramp-down processes were carried out after the standard 500 nm TEOS deposition: (1) XX: no plasma and no He or O_2 flow; (2) NP: He and O_2 flow but no plasma; (3) He: only He plasma (1200

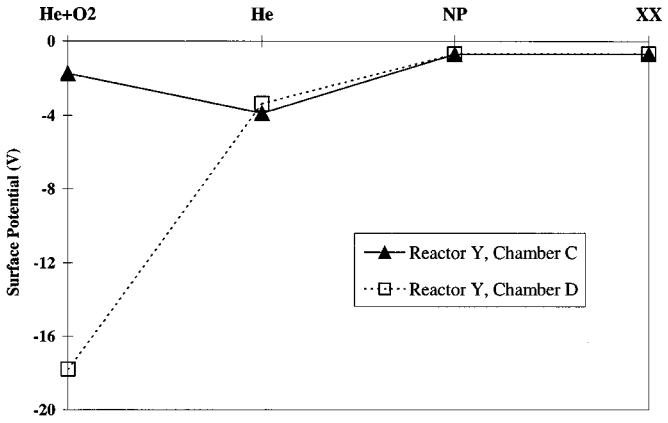

Figure 3. Average surface potential after 500 nm TEOS deposition performed in chambers C and D of the PECVD system Y for different ramp-down processes. Nine points were measured on each wafer.

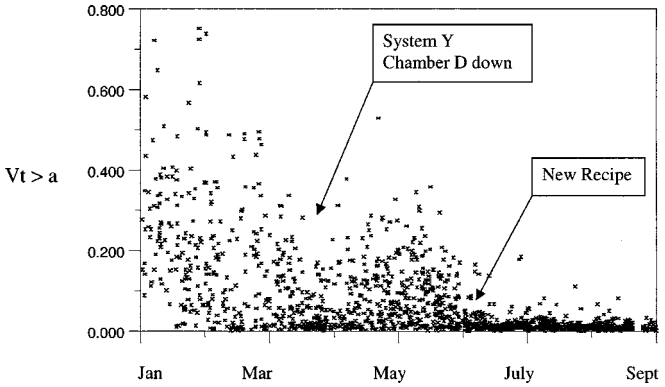

Figure 5. Five-lot average of the fraction of antenna transistors with high threshold voltage shift due to poly, metal 1, metal 2, metal 3 charging.

sccm) during ramp-down; (4) He + O_2: standard ramp-down in a He and O_2 plasma (1200 sccm He, 1000 sccm O_2). This is the same ramp-down used in the case of data in Fig. 2.

For each variant, one wafer was processed in chamber C and one wafer in chamber D of the Y system. The average surface potential for each of the eight wafers is plotted in Fig. 3. Negligible differences between C and D are observed if no plasma is ignited during ramp-down (variants 1 and 2). The same is obtained if only He plasma is used (variant 3). However, if He + O_2 plasma is used during ramp-down (variant 4), the surface potential measured for chamber D is *ca.* −18 V whereas that measured for chamber C is only *ca.* −2 V.

Results in Fig. 3 indicate that the anomalous behavior of chamber D is triggered during plasma ramp-down after deposition. They also illustrate the relevance of the hardware-process interaction for charging. In fact, they indicate that the risk of charging in the presence of hardware marginality (chamber D is behaving differently from chamber C) is enhanced by a wrong process choice (ramp-down in a He + O_2 plasma).

The issue of process optimization to reduce charging in the presence of hardware marginality is discussed in Fig. 4. TEOS layers were deposited at pressures ranging from 4 to 15 Torr and at three different oxygen flows using the defective chamber of system Y (chamber D). After deposition, the wafer surface potential was measured on nine points per wafer and V_{SPave} and ΔV_{SP} have been

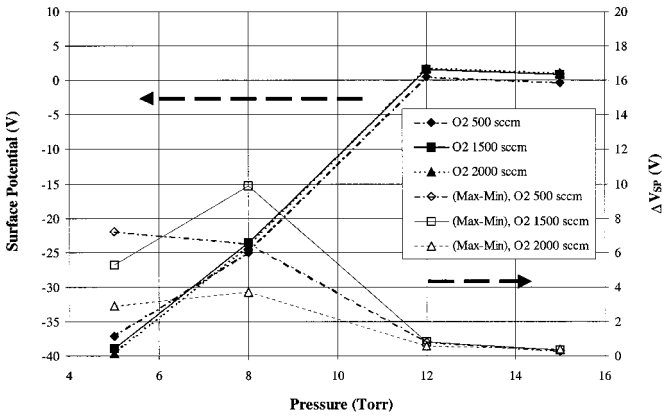

Figure 4. Average surface potential (V_{Spave}) and in-wafer spread ($\Delta V_{SP} = V_{Spmax} - V_{Spmin}$) *vs.* the deposition pressure for different oxygen flows. The TEOS layers (500 nm thick) were deposited using chamber D of system Y. Nine points were measured on each wafer.

calculated. As illustrated in the figure, V_{SPave} is 40 V at 5 Torr, it reduces to 24 V at the pressure of 8 Torr (standard deposition pressure), and it decreases almost to zero if the pressure is further increased to 12 V. A similar trend is observed for ΔV_{SP}. No effect of the oxygen flow are observed instead. These results indicate that an increased deposition pressure may reduce the effect of defective hardware on charging.

The effect of disabling the defective chamber and of the introduction of an optimized recipe with a higher deposition pressure on the threshold voltage of the antenna transistors is shown in Fig. 5. In this figure the total fraction of antenna transistors with threshold voltage higher than the upper specification limit *a* is displayed as a function of the process time. At the beginning, a large spread in the failing fraction was observed. This spread was reduced, but not completely suppressed, after the defective chamber D was put down for production. Finally, after the introduction of the optimized recipe, the failing fraction reduced practically to zero. Results in Fig. 5 confirm those obtained by Kelvin-probe measurements and indicate that when, as in the case considered here, instability occurs during the last moments of the plasma process, the Kelvin-probe technique can be used as a fast feedback technique to monitor charging.

SILOX deposition.—SILOX films, 300 nm thick, were deposited on 200 mm wafers as part of the dielectric stack that insulates the control gate of EPROM cells from the first metal layer. The deposition was carried out using a single-frequency recipe and two different reactors: a single-wafer reactor and a batch reactor. The threshold voltage of the EPROM cells was measured immediately after the deposition and patterning of the first metal layer.

Figure 6 shows the cumulative distributions of the threshold voltage before and after UV erasure. Before UV erasure, the distribution is shifted to higher values when the single-wafer tool is used. In fact, the 50% value of the distribution is 1.6 and 1.3 V for the single-wafer and the batch reactor, respectively. The spread $V_{tmax} - V_{tmin}$ of the threshold voltage in the wafer is also higher for the single wafer than for the batch reactor, 0.6 and 0.3 V, respectively. The difference between the two systems disappears after UV erasure, demonstrating that the cause was a difference in the amount of charges trapped in the floating gate. This difference can be quantified using the relation between the charge trapped in the FG, ΔQ_{FG}, and the shift, ΔV_t, of the threshold voltage after UV erasure[7]

$$\Delta V_t = -\frac{\Delta Q_{FG}}{C_G} \qquad [1]$$

where C_G, the capacitance between the control and floating gates, is equal to

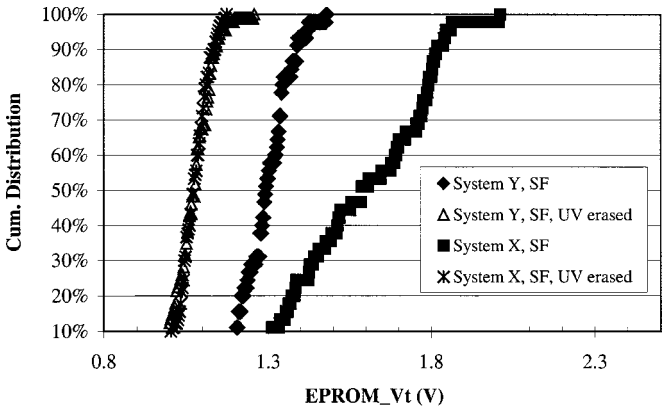

Figure 6. Cumulative distributions of the threshold voltage V_t of EPROM cells processed either in the single-wafer or in the batch reactors. Distributions before and after UV erasure are compared. The V_t measurements were performed after metal 1 deposition.

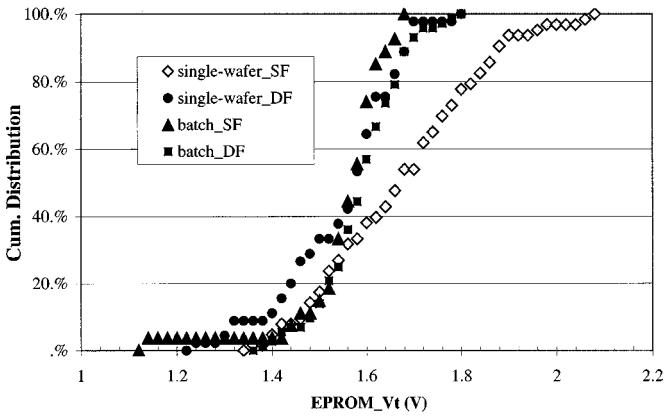

Figure 8. Cumulative distributions of the threshold voltage V_t of EPROM cells processed either in the single-wafer or in the batch reactors. The SILOX deposition was carried out either using single-frequency (SF) or double-frequency (DF) recipes.

$$C_G = \frac{KL\varepsilon_0\varepsilon_{ox}}{t_{ONOeff}} + \frac{(2K+2L)H\varepsilon_0\varepsilon_{ox}}{t_{SWeff}} \qquad [2]$$

In Eq. 2, t_{ONOeff} and t_{SWeff} are the effective thicknesses of the ONO layer and sidewall dielectric, $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m is the permittivity of the free space and $\varepsilon_{ox} = 3.9$ is the oxide dielectric constant, K, L, and H indicate the width, the length, and the height of the floating gate, respectively. For the cells used in this study it is $t_{ONOeff} \approx 20$ nm $t_{SWeff} = 33$ nm, $K = 1.4$ μm, $L = 0.35$ μm, $H = 0.2$ μm. Equation 2 then yields $C_G \approx 1.58 \times 10^{-15}$ F. Figure 6 shows that the shift of the threshold voltage after UV erasure is $\Delta V_t = 0.5$ V and $\Delta V_t = 0.2$ V for the single wafer and the batch reactor, respectively. From Eq. 1 and 2 it follows then $\Delta Q_{FG} = 0.82 \times 10^{-15}$ C and $\Delta Q_{FG} = 0.35 \times 10^{-15}$ C for the single wafer and the batch reactor, respectively.

The threshold voltage distributions of the reference transistors (*i.e.*, EPROM cells in which FG and CG are shorted) for the same variants as in Fig. 6 are shown in Fig. 7. The threshold voltage for the reference transistors is smaller than for the EPROM cells. This is expected. In fact, the potential drop across the ONO layer which lowers the potential of the FG in the EPROM cell is absent in the reference transistor, where FG and CG are shorted. More interesting, the V_t distributions are similar for all variants, confirming that the differences between the two reactors seen in Fig. 6 are not due to wafer-to-wafer variations of the cell morphology (like oxide thickness or floating gate length variations) but to charge trapped in the FG.

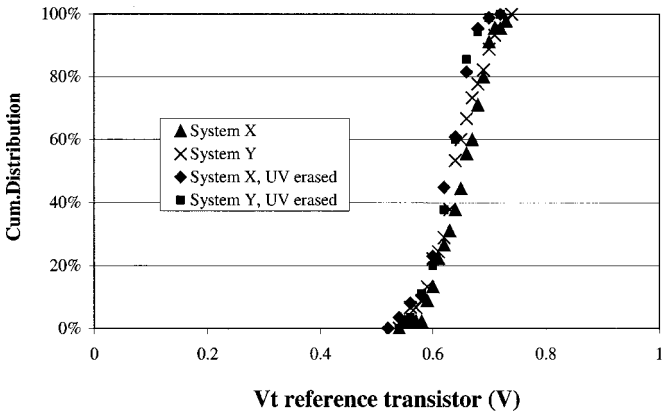

Figure 7. Cumulative distributions of the threshold voltage of reference transistor (*i.e.*, an EPROM cell in which control and floating gates are in short). The same variants as in Fig. 6 are compared.

The results in Fig. 6 and 7 illustrate that charging is higher in the single-wafer reactor than in the batch reactor. This is probably due to the fact the rf power is applied to a single wafer in the first case whereas it is divided among six wafers in the second. Data in Fig. 8 illustrate that the use of a double-frequency recipe can reduce the influence the reactor architecture has on charging. In the figure, the cumulative distributions of the threshold voltage for the two reactors (single wafer and batch) and the two deposition recipes (double and single frequency) are compared. In the case of the single-frequency deposition the difference between the two reactors is similar to that already seen in Fig. 6. However, the difference disappears if the double-frequency recipe is used. In this case, a low-frequency (10 kHz) rf power is applied to the wafer chuck in addition to the standard 13.5 MHz rf power used to ignite the plasma. The addition of the extra rf power allows the optimization of the ion plasma (ions are too heavy to react efficiently to the 13.5 MHz frequency) independently from that of the electron plasma. This results in better control of the plasma uniformity and, as consequence, in a lower charging level even in the case of the single-wafer reactor.

Sensitivity of the EPROM cell to charging.—In the presence of charging the floating gate potential rises to a value $V_{FG} = \alpha V_{CG}$ (α and V_{CG} being the coupling factor of the cell and the control gate potential, respectively). As a consequence, the following FN current flows from the substrate into the FG[15]

$$J = AE_{ox}^2 \exp\left(-\frac{B}{E_{ox}}\right) \qquad [3]$$

where $E_{ox} = \alpha V_{CG}/d_{ox}$ is the electrical field in the oxide of thickness d_{ox}.[a] In Eq. 3 A, B are constants related to the tunneling barrier height Φ and to the effective mass of the tunneling electron in the oxide m_{ox} by the equations[16]

$$B = \frac{4}{3}\frac{\sqrt{2m_{ox}}}{q\hbar}\Phi^{3/2} \qquad [4]$$

$$A = \frac{q^3}{16\pi^2\hbar\Phi} \qquad [5]$$

[a] In general it should be written $E_{ox} = (\alpha V_{CG} - V_T)/d_{ox}$ with V_T being the voltage necessary to create the inversion layer in the EPROM channel. However, at the temperature used for plasma deposition (400°C) the Si substrate becomes intrinsic (see Ref. 18) and no inversion layer has to be created to inject electrons in the FG.

where ($\hbar = 6.63 \times 10^{-34}/2\pi$ kg m^2 s^{-1} and $q = 1.6 \times 10^{-19}$ C).

For the EPROM cell of Fig. 1, the gate material is n^+-type poly-Si and the gate oxide is 8 nm thick. In this case, $\Phi \approx 3.25$ eV,[16] $m_{ox} = 0.32m_e$ (where $m_e = 9.11 \times 10^{-31}$ kg is the electron rest mass),[17] and A and B equal 4.83×10^{-7} m^2/V^2 and 7.54×10^9 V/m, respectively.

If V_{FG} (and therefore J) is assumed constant during SILOX deposition, then the charge trapped in the FG is equal to $\Delta Q_{FG} = J \times t$ (t is the deposition time). As calculated in the previous section, $\Delta Q_{FG} = 0.82 \times 10^{-15}$ C and $\Delta Q_{FG} = 0.35 \times 10^{-15}$ C for the single wafer and the batch reactor, respectively. For a deposition time of *ca.* 15 s the previous equation then yields $J = 5.5 \times 10^{-17}$ A for the single-wafer reactor and 2.3×10^{-17} A for the batch reactor. Substituting these values in Eq. 3 and solving it with respect to V_{CG}, it is found that the effective voltage applied to the control gate during deposition is $V_{CG} \approx 1.27$ V and $V_{CG} \approx 1.24$ V for the two reactors.[b] This result illustrates the capability of the EPROM cell to resolve differences as low as 30 mV in the average charging performance of different deposition systems.

Conclusions

In this work, PECVD TEOS and SILOX deposition were studied using the Kelvin probe technique, EPROM cells, and antenna transistors. It was found that

1. Charging due to a defective deposition chamber is triggered if oxygen is added to the plasma gases during plasma ramp-down after TEOS deposition. No effect of the defective chamber on charging is detected if only helium is used instead.

2. Single-wafer reactors are found to cause more charging than batch reactors during SILOX deposition. However, this sensitivity to the reactor chamber architecture is suppressed if deposition is carried out with an additional low-frequency rf power applied to the wafer susceptor.

3. Deposition pressure affects charging during TEOS deposition. Kelvin-probe measurements suggested that an increase of the deposition pressure could optimize the recipe. After the introduction of a recipe with an increased deposition pressure, the shift of the threshold voltage of antenna transistors was drastically reduced.

Results 1 and 2 demonstrate that the effect on charging of defective hardware or nonoptimal system architecture can be reduced by more careful process choices. Result 3 indicates that the Kelvin-probe technique can be successfully used as a fast feedback technique for charge monitoring and process optimization when, as in the case of TEOS deposition, charging occurs at the end of the plasma process.

[b] These values should be considered as the lower limit for the maximum voltage seen by the cell during processing. In fact, in general, the voltage is constant neither in its absolute value nor in its polarity during the deposition. As a consequence, the charge ΔQ_{FG} trapped in the floating gate at the end of the plasma deposition is the result of a balance between the negative and positive charges injected in the floating gate during the different phases of the plasma process.

Acknowledgments

Part of this work was financially supported by the MEDEA Project T501. K. Druijf, P. Schumbera, J. R. M. Luchies, and A. Scarpa (Philips Semiconductors, MOS4*YOU*, Nijmegen) are acknowledged for their help during the measurements and their useful comments and suggestions.

Philips Semiconductors assisted in meeting the publication costs of this article.

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