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Low-temperature solid phase epitaxy for integrating advanced source/drain metal-oxide-semiconductor structures

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We show that chemical vapor deposition using trisilane decomposition opens capabilities for the deposition of amorphous silicon on Si substrate at low temperature. Based on this behavior we developed a process including amorphous silicon deposition and crystallization. Transmission electron microscopy observations prove that solid phase epitaxy (SPE) occurs and produces monocrystalline layers, free of extended defects and compatible with complementary metal-oxide-semiconductor technology. We also show that during SPE films remain amorphous on oxidized areas while they transform into single crystal on Si. This process opens promising perspectives for the fabrication of advanced MOS structures. © *2010 American Institute of Physics*. [doi:10.1063/1.3298354]

The objective of this work is to realize defect free, ultrahighly doped single-crystal silicon layers using conventional chemical vapor deposition (CVD) fully compatible with complementary metal-oxide-semiconductor (CMOS) technology. For this purpose, we have developed a two-steps process including amorphous silicon (a-Si) deposition and solid phase epitaxy (SPE) at low temperature (LT). The crystallization via SPE of a-Si layers has already been shown to produce single-crystal (c-Si) layers that were doped at extremely high levels.[1–3] This process was used for the formation of source and drain (S/D) extensions where shallow and highly activated junctions are needed. In the latter work, amorphous layers were obtained by implantation of heavy species (such as Ge) which is well known to create end of range crystal defects[4] that are detrimental for junction leakage.

The main advantages of the process developed here are the low thermal budget, the full compatibility with CMOS technology and the ability to produce in a single run both monocrystalline and amorphous Si on the different surface phases of the substrate. In this approach, two main critical and challenging steps should be addressed: for a start the deposition of a fully amorphous material. Since the layer has to be totally free of any crystal grain or nanocrystal to avoid the formation of a polycrystalline layer during the subsequent SPE step. The second challenge is the formation during the SPE step of single c-Si totally free of defects and with ultrahigh concentration of fully activated dopants.

In this work, the CVD of a-Si on (001)Si and on SiO_2 is first presented. In the second part we report the LT-SPE kinetics. In the third section, the two-steps (CVD and crystallization) process is integrated in CMOS technology for the fabrication of raised S/D structures.

Thin films were grown in an industrial ASM Epsilon® reduced pressure CVD reactor, on 200 mm diameter wafers. The precursor used for Si deposition is trisilane (Si_3H_8, Silcore®). For doping (*p*-type) of the films we used diborane (B_2H_6). For all experiments, the carrier gas was purified hydrogen (H_2). It was kept constant during all the experiments to maintain a total pressure of the reactor about 60 Torr. The substrates used for experiments were (a) nominal (001)Si wafer; (b) 100 nm thick thermal SiO_2/(001)Si wafer; (c) patterned (001)Si wafer with advanced MOS structures [polycrystalline Si gate, HTO coating, Si_3N_4 spacers, and shallow trench isolation (STI)]. The film thickness was determined either by weight measurements or by spectroscopic ellipsometry. Tapping mode atomic force microscopy (AFM) images were analyzed to determine the surface roughness and the morphology of the layers (Digital Instruments DI3100 NanoScope III). The boron doping depth profiles of the layers were determined by SIMS using a CAMECA IMS 5F spectrometer. Microstructural and chemical analyses of the layers were obtained by cross-section and plane view transmission electron microscopy (TEM) observations. TEM experiments were performed on a 200 kV JEOL 2010 FEG equipped with dispersive energy spectroscopy and elastic energy loss spectrometry.

Si deposition was performed by conventional CVD using Silcore®.[5] Kinetics of growth using trisilane and silane are compared on Fig. 1 for identical incoming silicon atomic

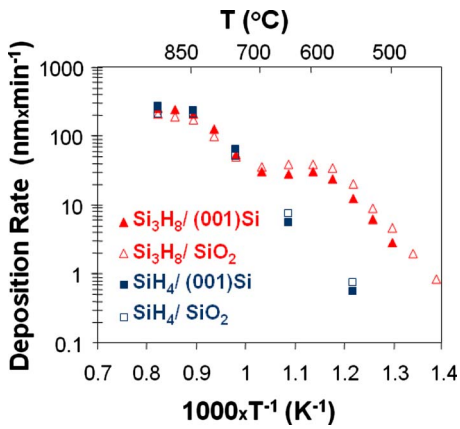

FIG. 1. (Color online) The growth rate of Si layers on (001)Si and SiO_2/(001)Si using Si_3H_8 (triangles) and SiH_4 (squares), in equivalent Si atomic flow, as a function of the growth temperature.

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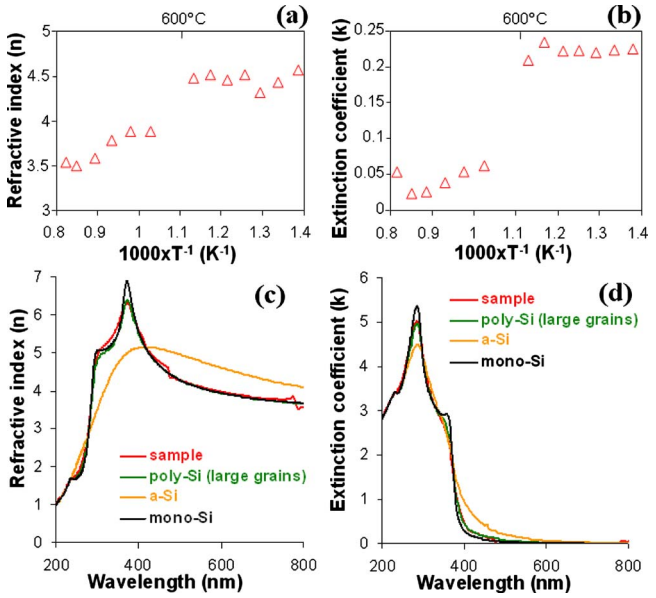

FIG. 2. (Color online) Refractive index (n) and Extinction coefficient (k) of the films deposited with 48 mTorr Si_3H_8 flow; [(a) and (b)] reproduce the evolution of (n) and (k) with the growth temperature when the films are deposited on SiO_2; [(c) and (d)] give the comparison of (n) and (k) coefficients for a film deposited at 500 °C on (001)Si (sample) and of reference samples (polycrystalline, amorphous, and monocrystalline Si). The comparison shows that in this situation, the film presents similar optical parameters than polycrystalline Si.

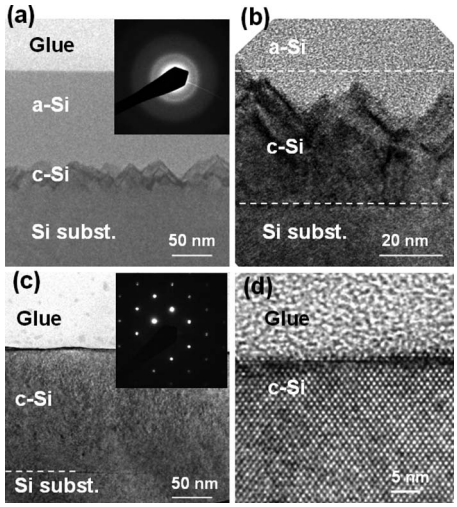

FIG. 3. TEM cross-section images of: (a) the film deposited at 400 °C on (001)Si. The inset reproduces the SAD pattern typical of the amorphous phase (diffuse ring and total absence of spots); (b) the thin c-Si layer which evidences (111) facets at the a/c interface; (c) the film after total crystallization by *in situ* SPE at 500 °C during 600 s. The inset reproduces the corresponding SAD pattern which exhibits only the [110] direction of the monocrystal; (d) of the same area at high resolution to show the atomically flat top surface.

flow (trisilane and silane partial pressures are 48 and 144 mTorr, respectively). In the LT range the growth rate is much larger with trilsilane than with silane (almost 20 times larger at 550 °C). The trisilane presents lower decomposition temperature than silane (Refs. [5,6]) and thus allows lower thermal budget deposition. From the different surface phases (SiO_2 and (001)Si), we can see that the total absence of selectivity during Si_3H_8 deposition similarly to the deposition with SiH_4.

The deposited layers on (001)Si and on SiO_2/(001)Si were then investigated by ellipsometry. Refractive index (n) and extinction coefficient (k) of the samples were extracted and compared to the n index and k coefficient of amorphous (a-Si), crystalline (c-Si) films which are, in the same experimental conditions (wavelength of 632.8 nm), $n_{a\text{-}Si}$=4.517 ($n_{c\text{-}Si}$ 3.880) and $k_{a\text{-}Si}$=0.231 ($k_{c\text{-}Si}$=0.019), respectively. The optical parameters of the films deposited on SiO_2 have been measured as a function of the substrate temperature [Figs. 2(a) and 2(b)]. The curves exhibit a dramatic change of these parameters at a temperature of ~600 °C. The comparison with reference samples shows that below 600 °C the Si film is amorphous, while above 600 °C it is polycrystalline. Concerning the deposition of Si on (001)Si (homoepitaxy), the film microstructure is well known to be single crystal. Nevertheless, a deposited monocrystalline layer totally free of any crystal grain is not able at low temperature. Crystal grains induce the formation of a polycrystalline layer. Figures 2(c) and 2(d) give the comparison of the optical parameters of the Si film deposited at 500 °C (Si_3H_8 partial pressure ~48 mTorr) on (001) Si with those of reference samples. It shows that the optical parameters of the film are very similar to the ones of polycrystalline Si.

In order to obtain an amorphous Si layer on (001)Si, we decreased again the growth temperature (to 400 °C) (Ref. 7) meanwhile the growth rate was compensated by increasing the Si_3H_8 partial pressure to ~60 mTorr (flow ratio $F_{Si_3H_8}/F_{H_2}$ of 0.1%). For application reasons the film was doped to 1.10^{21} B/cm^3 using a B_2H_6 partial pressure of 0.12 mTorr.The growth rate is approximately 22 nm min^{-1}. The thickness determined from weight measurements was ~150 nm. At this CVD temperature, the film consists of two parts: a thin c-Si rough layer at the interface (about 15 nm thick) and a second thick layer (about 140 nm thick) fully amorphous [Fig. 3(a)]. One can see that the film/substrate interface is facetted with pronounced (111) facets [Fig. 3(b)]. Such interface morphology has been predicted by molecular dynamics simulations for crystallization at high temperature.[8] The amorphous microstructure of the thick part of the film is evidenced by cross-section TEM image which reveals a "salt and pepper" phase contrast at high resolution typical of amorphous material. Moreover, the selected area diffraction (SAD) of the film evidence diffuse rings and the total absence of diffracted spots on all the areas investigated confirming the amorphous nature of the layer and the total absence of nanocrystalline grains [Fig. 3(a) inset].

Crystallization of these a-Si films on (001)Si is produced by *in situ* SPE at 500 °C with a reactor total pressure maintained at 60 Torr with H_2 flux. This annealing step considerably flattens the c/a interface and suppresses the (111) facets well visible at this interface in the sample before SPE. The c/a interface becomes essentially flat (001) with an extremely small portion of (111) edges. After total crystallization (SPE duration of 600s) the film appears single crystal, epitaxially grown on the substrate and fully free of extended defect [Fig. 3(c)]. All the SAD patterns acquired on different areas of the film only exhibited the [110] direction [Fig. 3(c) inset]. The top surface of the film is flat [Fig. 3(d)] and its surface roughness measured by AFM is below 1 Å, comparable to the residual roughness of standard bulk Si wafers. In the same experimental conditions, crystallization of a-Si film does not occur on insulating areas (SiO_2) and the film remains fully amorphous. This is attributed to the absence of

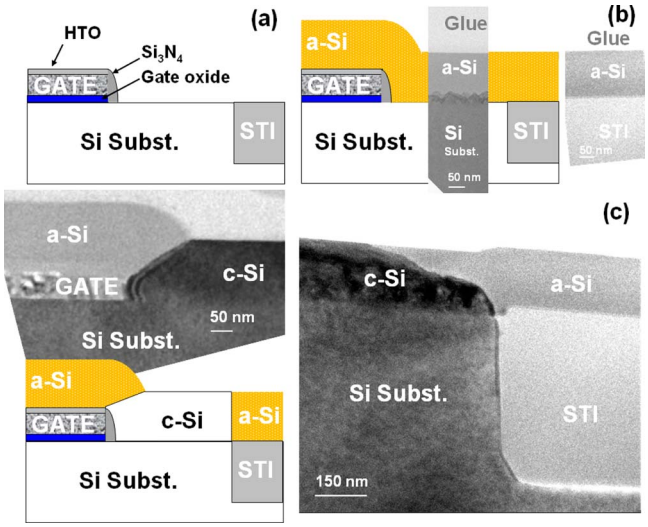

FIG. 4. (Color online) (a) Schematization of the initial MOS structure; (b) Schematization of the structure after deposition of a-Si on the initial structure. The corresponding TEM cross-section images of the experimental a-Si layer on the different areas are given; (c) Schematization of the structure resulting from the selective crystallization process. The corresponding experimental TEM cross-section images of the a-Si and c-Si on the different areas are shown.

nucleation sites and gives insights on physical properties of the a/c interface.

In the next part we used the two-steps (CVD at 400 °C and LT-SPE at 500 °C) process developed above for the fabrication of very shallow raised S/D. Such configuration has been reported to improve short channel effect (SCE) and performances of CMOS devices.[9] Raised S/D were usually formed by selective epitaxial growth (SEG) in Si–Cl–H (Refs. 9,10 and 11) or Si–H systems (Refs. 12 and 13) that require high temperature steps (>850 °C) for both the cleaning step (native oxide removal) and epitaxial growth. Such high thermal budget is known to be detrimental for device performances such as SCE.

In our study a low thermal budget approach is considered. Its process steps using MOS structure are schematized in Fig. 4. The initial MOS structure [Fig. 4(a)] is covered by a-Si using the experimental conditions determined above [Fig. 4(b)]. Then, SPE is promoted during annealing at LT (500 °C). TEM cross-section images of the structure resulting from SPE are presented in Fig. 4(c). TEM images exhibit the *a*-Si layer on top of the gate (covered by HTO coating) and the *c*-Si layer/Si substrate and *a*-Si/STI interfaces, respectively. The *a*-Si deposited on oxidized areas did not crystalline. This phenomenon is consistent with results reported above showed that below 600 °C Si phase transformation does not occur in SiO_2. Inversely, on the Si substrate, the film is perfectly monocrystalline and epitaxial. We can remark that in the region close to shallow trench insulation (STI), the crystallization of a-Si is not perfect. This phenomenon is due to the lower temperature (<500 °C) of the substrate (and of the a-Si) next to these insulating STI areas and we suggest that this interfacial zone could be suppressed by increasing the SPE annealing time to complete the crystallization. The developed SPE process gives then a unique selective crystallization of a-Si on Si substrate and not on SiO_2. Such process can be extended to various structures using either doped or intrinsic Si.

For the fabrication of a raised S/D MOS structure, a last step of a-Si removal is needed. This step could be achieved by chemical vapor etching using HCl gas at 600 °C.[14]

In conclusion, the two-steps (CVD and LT-SPE) process developed during this work provides an original way to fabricate monocrystalline Si free of defects. The characterization techniques show that the material is of good quality and compatible with CMOS technology while requesting a low thermal budget as compared to conventional processes. During the deposition step fully amorphous Si films were obtained by conventional CVD using Silcore® at 400 °C on (001)Si. The amorphous films were further transformed into monocrystalline Si, during a second step of solid phase epitaxy at 500 °C. We demonstrated, in the last part of this work, that this two-steps process creates a selective crystallization of a-Si on Si(001) and not on SiO_2 areas. Such process provides an exceptional way to fabricate in a single run monocrystalline and amorphous films and is highly promising for the fabrication of raised S/D advanced MOS structures.

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