Formation of NiSi-Silicided p$^+$n Shallow Junctions Using Implant-Through-Silicide and Low-Temperature Furnace Annealing

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NiSi-silicided p$^+$n shallow junctions are fabricated using BF$_2^+$ implantation into/through thin NiSi silicide layer (implant-through-silicide technology) followed by low-temperature furnace annealing (from 550 to 800°C). The NiSi film agglomerates following a thermal annealing at 600°C and may result in the formation of discontinuous islands at a higher temperature. The incorporation of fluorine atoms in the NiSi film can retard the formation of film agglomeration and thus improving the film's thermal stability. The forward ideality factor of about 1.02 and the reverse current density of about 1 nA/cm^2 can be attained for the NiSi (310 Å)/p$^+$n junctions fabricated by BF$_2^+$ implantation at 35 keV to a dose of 5 × 10^{15} cm^{-2} followed by a 650°C thermal annealing; the junction formed is about 60 nm measured from the NiSi/Si interface. Activation energy measurement indicates that the reverse bias junction currents are dominated by the diffusion current, indicating that most of the implanted damages can be recovered after annealing at a temperature as low as 650°C.

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Metal silicides have been extensively used in submicron devices for lowering the series and contact resistance of source/drain and polysilicon gate. Moreover, with the continuing scaling of device dimension into the deep submicrometer regime, the silicide-as-diffusion source (SADS) process has been proposed for the formation of silicide-contacted shallow junctions. In this process, silicide-contacted shallow junctions are formed by implanting dopants into the silicide layer followed by low-temperature annealing; thus, the process is also designated as implant-into/through-silicide (ITS) technology. Shallow junction formation, low-temperature processing, and low contact resistance are the major advantages of the SADS process.[1-7]

Among the metal silicides, titanium disilicide (TiSi$_2$) and cobalt disilicide (CoSi$_2$) are now widely used in salicide processes across the industry because of their good thermal stability and low electrical resistivity. However, some critical drawbacks limit their applications to future ultralarge-scale integrated (ULSI) technology. It has been reported that Ti may react with implanted dopant to form compounds such as Ti-B and Ti-As, making TiSi$_2$ a very ineffective diffusion source for boron or arsenic.[8,9] Moreover, the processing temperature window of TiSi$_2$ is relatively narrow due to the high-temperature requirement for the high-resistivity C49 to low-resistivity C54 phase transition (≧800°C) and the silicide agglomeration temperature limit (~950°C).[10] More importantly, incomplete transformation from C49 to C54 TiSi$_2$ phase occurs when the linewidth is scaled down below 2 μm because of the lack of nucleation center in the narrow lines, especially the triple-C49 grain boundaries.[11-14] In addition, the creep-up phenomenon during the formation of TiSi$_2$ silicide may form a bridge between the gate and source/drain regions in submicrometer devices, causing device failure.[15] Unlike TiSi$_2$, CoSi$_2$ has neither adverse linewidth dependence nor creep-up phenomenon. However, high Si consumption during the formation of CoSi$_2$ silicide is a major drawback for the submicrometer process. This restricts the vertical scaling for CoSi$_2$ to achieve shallow junction.[16] Moreover, junction spiking of CoSi$_2$ contacted shallow junction due to sensitivity to native oxide, and the oxygen-containing environment needs a more complex silicidation process, such as capping a passivation film during silicidation.[17-20]

Recently, nickel monosilicide (NiSi) has been recognized as a promising candidate for a contact metal for deep submicrometer device applications.[15,21-33] NiSi has a low electrical resistivity of 14-20 μm cm, which is comparable to those of TiSi$_2$ and CoSi$_2$; it

also shows neither adverse linewidth dependence nor creep-up phenomenon.[23,27] In addition, NiSi has a lower formation temperature (~400°C) than TiSi$_2$ and CoSi$_2$, making it suitable for the low-temperature process required for future device fabrication. The further advantage of NiSi relies on its smaller consumption of Si (0.82 Å Si for 1 Å NiSi) compared to CoSi$_2$ (1.04 Å Si for 1 Å CoSi$_2$),[28] which enables a shallow junction depth formation at the metal/Si contact. Besides, NiSi has the properties of low NiSi/Si contact resistance,[23,29] wide process window (400-750°C), and low film stress.[20-26] These peculiarities make NiSi suitable for usage in the low-temperature process for sub-100 nm CMOS technology.[30,31]

In this work, formation of NiSi-silicided p$^+$n shallow junction using ITS technology is investigated with respect to various implantation energies and doses. Feasibility of low-temperature processing and high-temperature stability of the NiSi/p$^+$n junction are evaluated by analyzing the electrical characteristics and material properties of the silicided junction. Effects of implantation conditions on the junction characteristics and high-temperature stability of the NiSi films are also investigated.

Experimental

The NiSi/p$^+$n junction diodes were fabricated on n-type (100)-oriented silicon wafers with 2.7-4 Ω cm nominal resistivity. After standard RCA cleaning, 5500 Å thick SiO$_2$ was thermally grown by pyrogenic oxidation at 1050°C. Active regions with areas of 1100, 580, 270, and 120 μm^2 were defined by photolithography followed by wet etching. A Ni film of 150 Å thickness was sputter deposited in a dc sputtering system with a base pressure of less than 2.5 × 10^{-8} Torr, using a Ni target in Ar ambient at a pressure of 2 × 10^{-3} Torr with a deposition rate of about 10 Å/s. After the Ni film deposition, the samples were rapid thermal annealed (RTA) at 500°C for 30 s in a N$_2$ ambient to form NiSi. The unreacted Ni film was selectively etched using a solution of H$_2$SO$_4$:H$_2$O$_2$ = 3:1 at 75-85°C. The formed NiSi film was about 310 Å thick as determined by transmission electron microscopy (TEM) analysis. The p$^+$n junction diodes were formed by BF$_2^+$ implantation into/through the NiSi silicide at an energy of 20-35 keV to a dose of 2 × 10^{15} or 5 × 10^{15} cm^{-2}, followed by thermal annealing at a temperature ranging from 550 to 800°C in a N$_2$ ambient for 30 min. Finally, a 5000 Å thick Al layer was deposited on the back side of Si substrate for all samples for a better contact in electrical measurements.

The thickness of the as-deposited Ni film and the formed NiSi film were determined with chemical delineation and TEM observation. Sheet resistance was measured by four-point probe on the unpatterned area. The p$^+$n junction depth was determined by spreading

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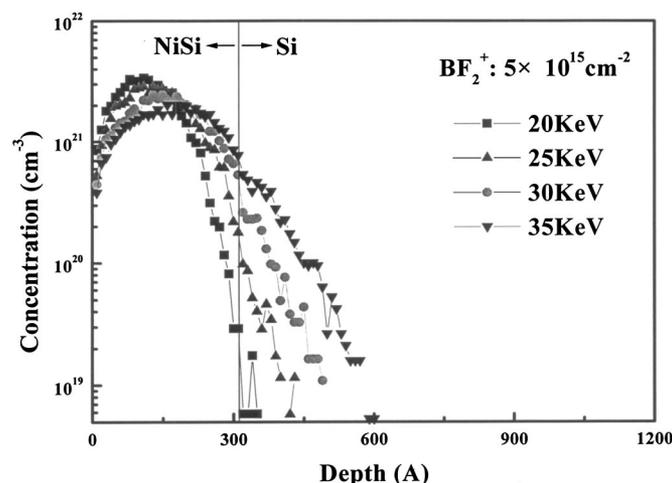
Figure 1. As-implanted boron profiles obtained by TRIM simulation for BF_2^+ implantation into a 310 Å thick NiSi film on Si substrate to a dose of 5×10^{15} cm^{-2} at various energies.

Figure 2. Sheet resistance *vs.* annealing temperature for NiSi(310 Å)/Si samples implanted with BF_2^+ at various energies to a dose of (a) 2×10^{15} and (b) 5×10^{15} cm^{-2}. The sample without ion implantation is designated as control sample.

resistance profiling (SRP) measurement. Surface morphology was observed by scanning electron microscopy (SEM). Secondary ion mass spectrometry (SIMS) was used to determine the dopant concentration profiles. The current-voltage (I-V) characteristics of the NiSi/p$^+$n junction diodes were measured by a semiconductor parameter analyzer HP-4145B. The open-circuit leakage current of the measuring system was kept below 0.5 pA. The forward bias from 0 to 1 V at a step of 0.01 V and the reverse bias from 0 to -5 V at a step of 0.05 V were used for the I-V characteristics measurement. Temperature dependence of the reverse junction current was measured from room temperature to 200°C on a thermal vacuum chunk.

Results and Discussion

Transport of ions in matter simulation.—Before making the BF_2^+ implantation, the as-implanted dopant distributions in NiSi film and Si substrate were predicted by transport of ions in matter (TRIM) simulation. For BF_2^+ ion implantation, the BF_2^+ ions are believed to be dissociated upon their first atomic scattering. Therefore, the boron energy is obtained by multiplying the BF_2^+ energy by the mass ratio of B$^+$ to BF_2^+, which is 11/49. In this work, boron ions are to be implanted into a sample which is composed of a 310 Å thick NiSi film and an underlying Si substrate. Figure 1 shows the as-implanted boron profiles obtained by TRIM simulation for BF_2^+ implantation at various energies to a dose of 5×10^{15} cm^{-2}. For the 20 keV implantation, nearly all implanted boron ions are located inside the silicide layer. In this case, the silicide film serves as a diffusion source of boron for the p$^+$n junction formation during the subsequent thermal annealing process. Boron in the silicide layer has to diffuse into the silicon substrate and become electrically active to form a good junction. Because boron can be electrically activated at a temperature as low as 550°C,[34] using NiSi as a boron diffusion source is possible at low processing temperature provided that a sufficient amount of boron atoms are diffused into the Si substrate. For the 25, 30, and 35 keV implantations to a dose of 5×10^{15} cm^{-2}, the boron concentrations at the NiSi/Si interface are all higher than 1×10^{20} cm^{-3}, while all projection ranges are kept within the silicide. These interface boron concentrations are high enough to form a good silicided p$^+$n junction provided that sufficient amount of dopants are electrically activated and most of the implantation damage can be annealed out.

Sheet resistance.—Figure 2 shows the sheet resistance (R_S) as a function of annealing temperature for the BF_2^+-implanted NiSi (310 Å)/Si samples; R_S data for the control sample without any ion im-

plantation are also included for comparison. The R_S of the control sample starts to show drastic increase after annealing at temperatures above 600°C. This increase of R_S was apparently due to the formation of islands at high temperatures, resulting in discontinuous structure of the NiSi film, as confirmed by the SEM micrographs to be shown later. The R_S of the BF_2^+-implanted samples decreased slightly with increasing temperature up to 700°C. For the sample implanted with a lower dose of 2×10^{15} cm^{-2}, annealing at 750°C resulted in NiSi film agglomeration and thus the increase of R_S, while the sample implanted with a higher dose of 5×10^{15} cm^{-2} was able to remain stable at temperatures up to 750°C. The corresponding electrical resistivity of the NiSi film is about 18 $\mu\Omega$ cm, which is in agreement with the value reported in the literature.[16] The different behavior of R_S value *vs.* annealing temperature for the sample with and without BF_2^+ implantation is attributed to the incorporation of fluorine in the NiSi film.[35-37] Moreover, a larger amount of fluorine retarded the NiSi film agglomeration to a higher temperature. Figure 3 shows the secondary ion counts of fluorine profiles in the sample of NiSi (310 Å)/Si implanted with BF_2^+ at 35 keV to a dose of 2×10^{15} as well as 5×10^{15} cm^{-2} followed by 750°C thermal annealing. The fluorine concentration in the NiSi film and at the NiSi/Si interface is much higher for the higher dose BF_2^+-implanted samples. The slightly higher value of R_S after annealing at 800°C is attributed to the formation of NiSi$_2$ phase.

SEM analysis.—Figure 4 shows the surface morphology of the NiSi (310 Å/Si) control sample annealed at various temperatures. Film agglomeration occurred at temperatures as low as 600°C, and the NiSi film was turned into isolated islands after annealing at and above 700°C, resulting in a drastic increase in the measured sheet resistance (Fig. 2). Figure 5 shows the surface morphology of the
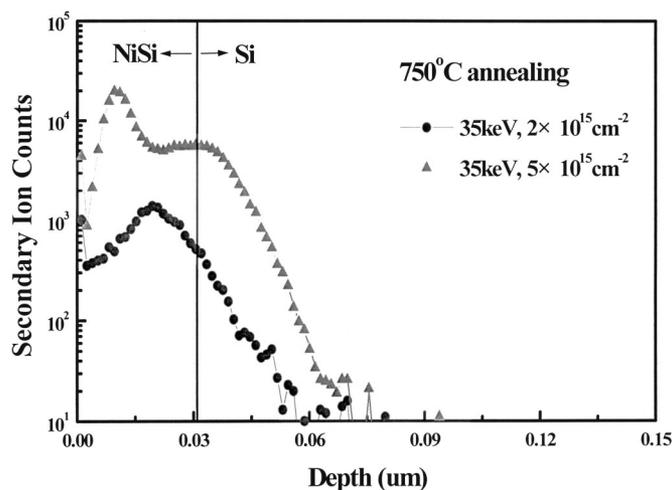
Figure 3. Secondary ion counts of fluorine ions in the sample of NiSi (310 Å)/Si implanted with BF_2^+ at 35 keV to a dose of 2×10^{15} as well as 5×10^{15} cm^{-2} followed by 750°C thermal annealing.

BF_2^+ (35 keV) implanted NiSi (310 Å)/Si samples annealed at various temperatures. For the lower dose (2×10^{15} cm^{-2}) implanted sample, the NiSi film remained smooth after annealing at 700°C, but some minor agglomeration of NiSi film was observed after annealing at 750°C, which might cause NiSi/Si interface roughness and degrade the NiSi/p$^+$n shallow junction characteristics. For the higher dose (5×10^{15} cm^{-2}) implanted samples, the NiSi film remained stable at temperatures up to 750°C. Similar results were observed for the samples implanted with BF_2^+ at lower energies of 25 and 30 keV. Apparently, incorporation of fluorine in NiSi film in a larger amount promoted the retardation of the NiSi film agglomeration. We presume that the segregation of the implanted fluorine species at the NiSi grain boundaries resulted in the change of grain boundary energy and interfacial energy, leading to retardation of the film agglomeration. After annealing at 800°C, localized sinking was observed on the silicide surface of both low- and high-dose im-
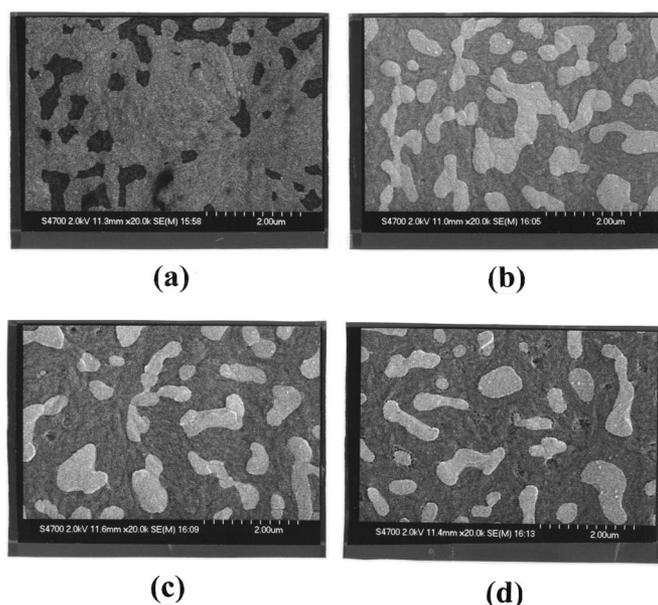
Figure 4. Top-view SEM micrographs showing the surface morphology of NiSi (310 Å)/Si control sample annealed at (a) 600, (b) 700, (c) 750, and (d) 800°C.

35keV/2x10^{15}cm^{-2} 35keV/5x10^{15}cm^{-2}
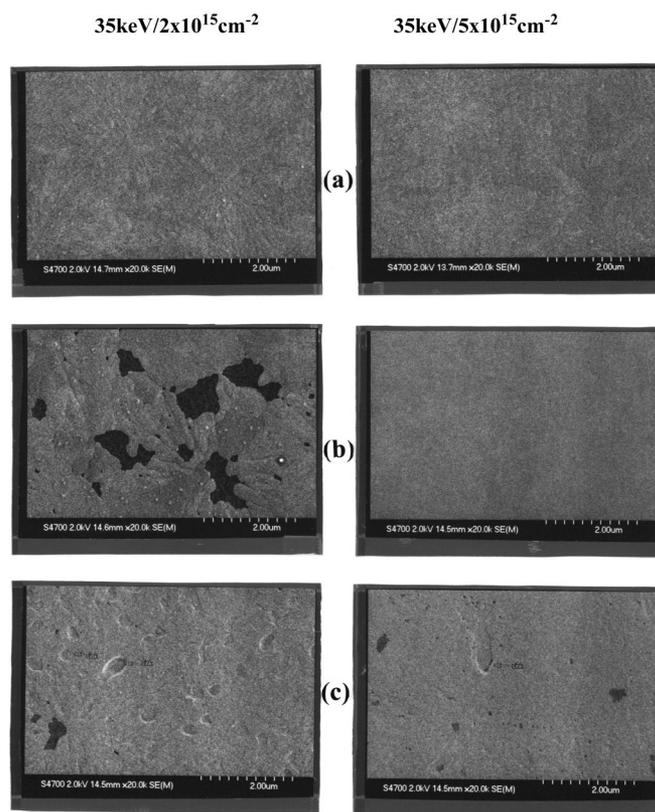
Figure 5. Top-view SEM micrographs showing the surface morphology of BF_2^+ (35 keV) implanted NiSi (310 Å)/Si samples annealed at (a) 700, (b) 750, and (c) 800°C. The micrographs of the low-dose (2×10^{15} cm^{-2}) and high-dose (5×10^{15} cm^{-2}) implanted samples are shown on the left and right columns, respectively.

planted samples, and the degree of film agglomeration was relieved to some extent. Because NiSi$_2$ phase was found to appear after annealing at 800°C [X-ray diffraction (XRD) result not shown] and it consumes more Si (Ni:Si:NiSi$_2$ = 1 Å:3.65 Å:3.63 Å) than the formation of NiSi phase (Ni:Si:NiSi = 1 Å:183 Å:2.34 Å),[28] the localized newly formed NiSi$_2$ surface would sink. Thus, we presume that the formation of NiSi$_2$ relaxed the agglomeration of silicide film and was able to maintain the continuity of the silicide film. We may conclude that the BF_2^+ implantation improves the thermal stability of NiSi film as confirmed by the film's sheet resistance behavior and the smoother surface morphology.

Junction depth measurement.—SRP measurement was used to determine junction depth in this work with an SSM-150 SRP system. All samples prepared for SRP measurements were first capped with a 3000 Å plasma-enhanced chemical vapor deposited (PECVD) oxide and then were polished to a small beveling angle of 17° for better resolution. Table I lists the junction depths measured from the silicide/silicon interface for the NiSi/p$^+$n samples studied in this work. For the sample processed with BF_2^+ implantation at 20 keV, the junction depth was determined to be about 25 nm after a 650°C/30 min thermal annealing. Since nearly all implanted boron ions are confined in the silicide film for the BF_2^+ implantation at 20 keV, the junction must be formed by the diffusion of boron from the silicide during the thermal annealing process. Although the diffusivity of boron in silicon is negligibly small at 650°C, it is presumed that the diffusivity of boron in silicon of this study could be enhanced by the presence of silicide film.[3,38] The enhancement in diffusivity is attributable to the vacancy injection from the silicide. For the implantation at higher energies (25, 30, and 35 keV), the implantation damage in silicon may also play a role for boron diffusion,

Annealing temperature	Implantation energy (keV)			
	20	25	30	35
600°C	23	24	40	56
650°C	25	36	45	60
700°C	28	40	49	65
750°C	35	45	59	70

resulting in deeper junctions. Higher implantation energy and higher annealing temperature resulted in an even deeper junction.

Electrical characteristics.—The electrical properties of the silicide contacted p⁺n shallow junction diodes fabricated by the ITS scheme are dependent on a number of factors, including the dopant activation level, implantation damage recovery, silicide/silicon interface roughness, and the distance between the silicide/silicon interface to the junction position. All of these are closely related to the energy and dosage of the dopant ion implantation as well as the dopant activation ability and the drive-in diffusion during the subsequent annealing process; this is especially important for the case of low-thermal-budget and low-energy implantation for the ITS scheme. All measurements were performed at room temperature, and each data point was obtained by averaging the data measured from six randomly chosen samples.

Forward ideality factor.—The forward ideality factor η of a junction diode can be extracted from the basic I-V relation

$$I = I_S[\exp(qV/\eta kT) - 1]$$

where I_S is the reverse saturation current, q is the electronic charge, k is the Boltzmann constant, and T is the temperature at measurement. An ideality factor of unity indicates that diffusion current predominates while a factor of two indicates that depletion recombination current is dominant. The ideality factor η can be determined from the slope of the linear segment of the I-V curve plotted on semilogarithmic coordinates. Figure 6 shows the ideality factor *vs.* annealing temperature for the NiSi/p⁺n junction diodes fabricated with BF₂⁺ implantation at various energies to a dose of 5×10^{15} cm⁻². All ideality factors are below 1.06 for the samples
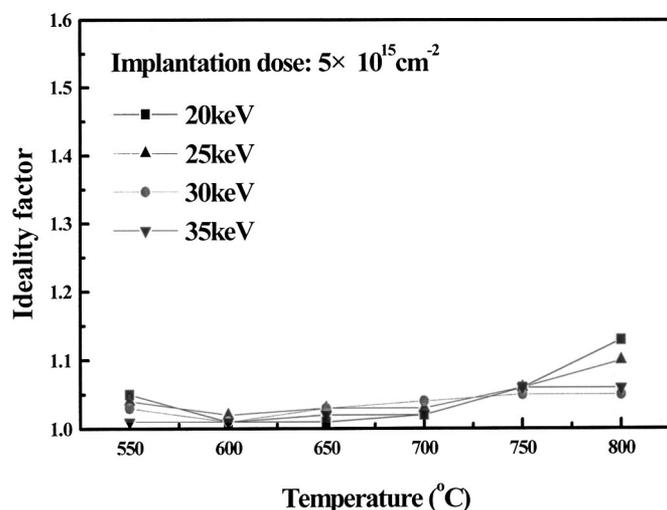
Figure 6. Forward ideality factor *vs.* annealing temperature for the NiSi/p⁺n junction diodes fabricated with BF₂⁺ implantation at various energies to a dose of 5×10^{15} cm⁻².
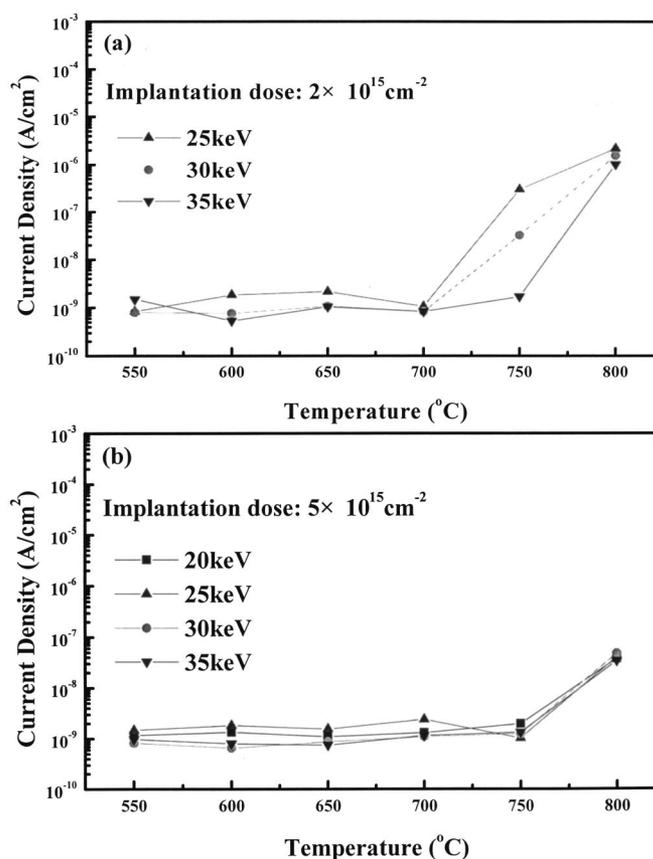
Figure 7. Reverse bias current density *vs.* annealing temperature for the NiSi/p⁺n junction diodes fabricated with BF₂⁺ implantation at various energies to a dose of (a) 2×10^{15} and (b) 5×10^{15} cm⁻².

annealed at and below a temperature of 750°C. The data in Fig. 6 indicates that a 30 min low-temperature (600-700°C) annealing is capable of incorporating sufficient amount of activated boron atoms in Si substrate as well as recovering the implantation damage to obtain a good NiSi/p⁺n shallow junction with an ideality factor below 1.04.

Reverse bias current.—Figure 7 shows the reverse bias current densities (J_R) *vs.* annealing temperature for the NiSi/p⁺n junction diodes with an area of 0.0121 cm² (1100 × 1100 μm) measured at a reverse bias of −5 V. The J_R is determined by directly dividing the measured current by the diode's area. Roughness of the silicide/Si interface in a shallow junction may lead to the formation of localized Schottky contacts or the agglomeration-induced local silicide spiking, resulting in the increase of reverse bias current. For the lower dose (2×10^{15} cm⁻²) implanted samples, J_R of less than 2 nA/cm² was easily achieved for the samples fabricated with a BF₂⁺ implantation at 25-35 keV followed by a thermal annealing at 550-700°C. For the samples annealed at 750°C, the 25 and 30 keV implanted samples exhibited drastic increase in reverse bias leakage current, while the 35 keV implanted sample revealed only a slight increase in leakage current. This increase in reverse bias leakage current is consistent with the behavior of the sample's sheet resistance (R_S), which in turn is related to the extent of agglomeration of the NiSi film. The agglomeration of the NiSi film induces roughness of the silicide/Si interface, leading to the penetration of silicide through the shallow junction and thus the degradation of the junction characteristics. The shallower the junction, the more susceptible the junction to the silicide/Si interface roughness. Thus, the J_R and the thermal stability of the p⁺n junction fabricated with BF₂⁺ implantation at 35 keV are better than those of the shallower junctions
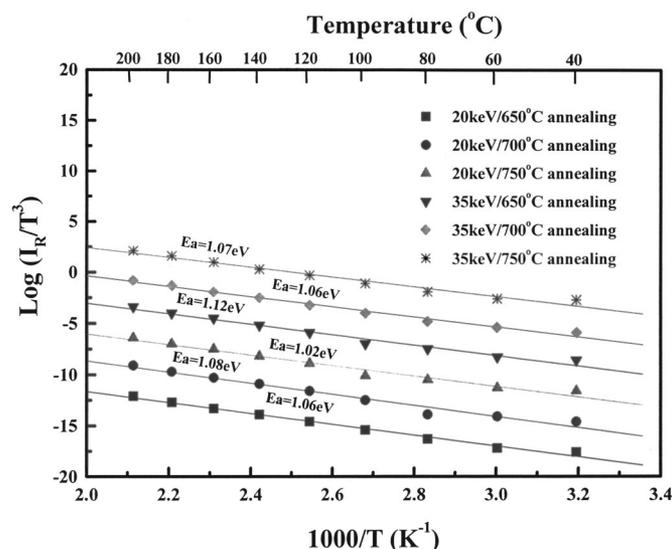
Figure 8. Arrhenius plots of the NiSi (310 Å)/p$^+$n junctions fabricated by BF$_2^+$ implantation at 20 and 35 keV to a dose of 5×10^{15} cm^{-2} followed by 650-750°C annealing for 30 min. The measurement was conducted at 1 V reverse bias.

fabricated with BF$_2^+$ implantation at 25 and 30 keV. With the annealing temperature raised to 800°C, all samples exhibited an even higher reverse bias leakage current. This is attributed to the formation of NiSi$_2$ silicide phase, the increased volume of which decreased the distance between the silicide and the junction position, leading to easier formation of localized Schottky contacts and thus the increase of reverse bias current. Moreover, since NiSi$_2$ is formed via a nucleation-controlled mechanism which induces a corrugated silicide/Si interface due to random nucleation on the original interface, large reverse bias current can be easily induced for shallow silicided junction.[35,39] As for the NiSi/p$^+$n samples fabricated with a higher dose (5×10^{15} cm^{-2}) BF$_2^+$ implantation, the J_R of less than 2 nA/cm^2 can be easily achieved with a postimplant thermal annealing at a temperature of 550-750°C. With a higher dose of BF$_2^+$ implantation, the p$^+$n junction formed becomes deeper and a larger amount of fluorine atoms is incorporated in the NiSi film, improving the thermal stability of the thin NiSi film.[36,37] With the annealing temperature raised to 800°C, formation of NiSi$_2$ phase started to occur, resulting in a drastic increase in reverse bias leakage current, similar to those observed in the samples fabricated with a lower dose (2×10^{15} cm^{-2}) of BF$_2^+$ implantation.

Activation energy measurement.—The temperature dependence of reverse bias junction current can provide insight into the junction leakage mechanism. The temperature dependence of reverse current I_R is given by

$$I_R \propto T^3 \exp(-E_a/kT)$$

where E_a is the activation energy of the junction, k is the Boltzmann constant, and T is the temperature at measurement. The value of E_a is close to the bandgap of silicon E_g when the reverse current is dominated by the diffusion current and is close to $E_g/2$ when the reverse current is dominated by the generation current. Figure 8 shows the Arrhenius plots for the NiSi (310 Å)/p$^+$n samples fabricated with various implantation and annealing conditions. The measurement was conducted at 1 V reverse bias. The activation energy was found to be close to the silicon bandgap of 1.12 eV for all samples investigated. This result clearly indicates that the reverse current was dominated by the minority carrier diffusion current at temperatures from 40 to 200°C.
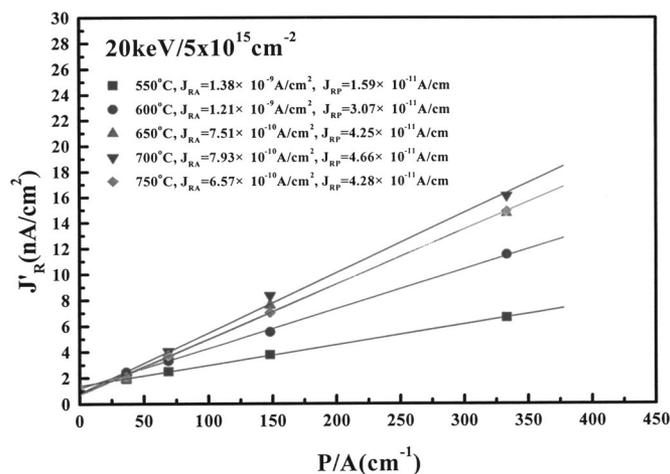
Figure 9. The J_R' *vs.* P/A plot of the NiSi/p$^+$n junctions fabricated with BF$_2^+$ implantation at 20 keV to a dose of 5×10^{15} cm^{-2} followed by annealing at 550-750°C.

Area and peripheral current.—The reverse bias leakage current (I_R) of a p$^+$n junction consists of the reverse area leakage current (I_{RA}) and the reverse peripheral leakage current (I_{RP})

$$I_R = I_{RA} + I_{RP} = A \times J_{RA} + P \times J_{RP}$$

where A is the junction area, P is the length of junction perimeter, J_{RA} is the junction area leakage current density, and J_{RP} is the junction peripheral leakage current density. A simple arrangement gives

$$J_R' = J_{RA} + J_{RP}(P/A)$$

where $J'R = I_R/A$. Thus, by measuring the I_R of junctions with different P/A ratio, the slope of J_R' *vs.* P/A plot gives the J_{RP} and the Y axis intersection gives the J_{RA}. Figure 9 shows the J_R' *vs.* P/A plot of the NiSi/p$^+$n junctions fabricated with BF$_2^+$ implantation at 20 keV to a dose of 5×10^{15} cm^{-2} followed by thermal annealing at a temperature from 550 to 750°C. It is found that the J_{RA} decreases from 1.38×10^{-9} to 6.57×10^{-10} A/cm^2 and the J_{RP} increases from 1.59×10^{-11} to 4.28×10^{-11} A/cm as the annealing temperature was increased from 550 to 750°C. For the junction diode with a size of 1100 μm^2 formed by annealing at 700°C, the J_{RA} is 0.79 nA/cm^2 and the J_{RP} is 46.6 pA/cm, and the corresponding area and peripheral current are 9.5 and 20.5 pA, respectively. This indicates that more than 68% of the total reverse current leaks through the junction's perimeter. For a smaller junction with an area of 120 μm^2, the peripheral component accounts for 95% of the total reverse current, indicating the major role of the peripheral leakage component. Presumably, most implanted defects were confined within the silicide layer; thus, very few extended defects are located beyond the silicide layer and the impact of these defects is minimal on the junction leakage. The peripheral leakage is sensitive to the interfacial behavior of Si/SiO$_2$ along the junction perimeter because the junctions formed in this study are all surrounded by field oxide. It is notable that the distance from the silicide/Si interface to the junction at the diode perimeter is much shorter than that at the diode bottom area after the postimplant thermal annealing. Moreover, the mechanical stress-induced defects along the diode perimeter is presumed to cause a higher peripheral leakage.[40] Thus, the junction characteristics are very sensitive to the silicide/Si interface property and the reverse junction current is dominated by the silicide-induced current along the periphery. Figure 10 illustrates a typical I-V characteristic for the NiSi/p$^+$n junction fabricated by BF$_2^+$ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by a 700°C thermal annealing for 30 min. It is clear that NiSi can serve as an effective
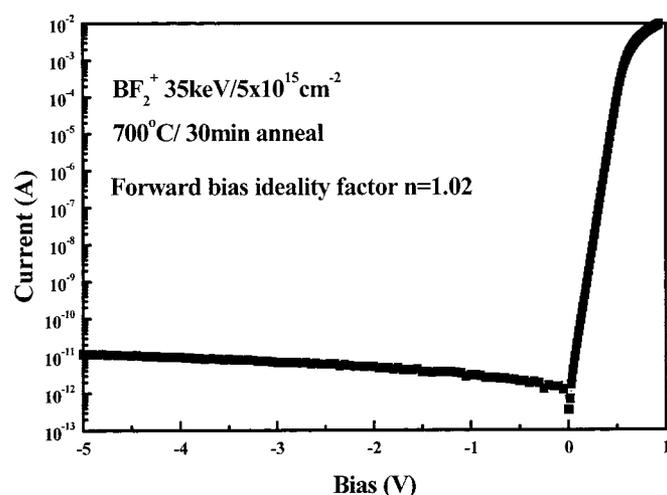
Figure 10. Typical I-V characteristic for the NiSi/p$^+$n junction fabricated with BF$_2^+$ implantation at 35 keV to a dose of 5×10^{15} cm^{-2} followed by a 30 min thermal annealing at 700°C.

diffusion source for boron diffusion during the low-temperature thermal annealing, resulting in the formation of NiSi/p$^+$n shallow junction with excellent electrical characteristics.

Conclusion

This work investigates the material properties of the NiSi film and the electrical characteristics of the NiSi contacted p$^+$n shallow junctions fabricated using BF$_2^+$ implantation into/through thin NiSi silicide layer (ITS technology) followed by low-temperature furnace annealing. The NiSi film agglomerates following a thermal annealing at 600°C and may result in the formation of discontinuous islands at a higher temperature. The incorporation of fluorine atoms in the NiSi film can retard the formation of film agglomeration and thus improve the film's thermal stability. For the sample with a BF$_2^+$ implantation dose of 5×10^{15} cm^{-2}, which is the highly doped sample studied in this work, the NiSi film is able to remain stable at temperatures up to 750°C. It is found that a larger amount of fluorine incorporation would result in a higher thermal stability temperature. Upon annealing at 800°C, however, the film agglomeration is relieved to some extent and localized sinking on the surface of Ni-silicide is observed, presumably due to the formation of NiSi$_2$ phase. The junction depth of the NiSi/p$^+$n junction diodes fabricated in this work ranges from 23 to 70 nm measured from the NiSi/Si interface. The activation energy measurements indicate that the reverse bias currents of the NiSi/p$^+$n junctions studied in this work are all dominated by the diffusion current. The reverse bias current is composed of the area current and the peripheral current components. For the diode's size of 120 μm^2 or smaller, more than 95% of the total reverse current would be contributed by the peripheral current. The reverse bias current density of 1 nA/cm^2 can be easily achieved for the NiSi/p$^+$n junctions studied in this work. To be more specific, the NiSi/p$^+$n junction fabricated with a 35 keV BF$_2^+$ implantation to a dose of 5×10^{15} cm^{-2} followed by a 30 min thermal annealing at 650°C has a forward ideality factor of 1.02, a reverse bias current density (at -5 V) of less than 1 nA/cm^2, and a junction depth of 60 nm.

Acknowledgment

References

1. V. Probst, H. Schaber, A. Mitwalsky, H. Kabza, L. Van den hove, and K. Maex, *J. Appl. Phys.*, **70**, 708 (1991).
2. B. Y. Tsui, J. Y. Tsai, and M. C. Chen, *J. Appl. Phys.*, **69**, 4352 (1991).
3. B. S. Chen and M. C. Chen, *J. Appl. Phys.*, **72**, 4619 (1992).
4. B. S. Chen and M. C. Chen, *IEEE Trans. Electron Devices*, **ED-43**, 258 (1996).
5. C. T. Lin, K. P. Ma, P. F. Chou, and H. C. Cheng, *J. Electrochem. Soc.*, **142**, 1579 (1995).
6. F. La Via and E. Rimini, *IEEE Trans. Electron Devices*, **ED-44**, 526 (1997).
7. J. S. Park, D. K. Sohn, J. U. Bae, C. H. Han, and J. W. Park, *IEEE Trans. Electron Devices*, **ED-47**, 994 (2000).
8. V. Probst, H. Schaber, P. Lippens, L. Van den Hove, and R. F. Keersmacker, *J. Appl. Phys.*, **52**, 1803 (1988).
9. K. Maex, R. F. De Keersmaecker, G. Ghosh, L. D. Delaey, and V. Probst, *J. Appl. Phys.*, **66**, 5327 (1989).
10. H. Jeon, C. A. Sukow, J. W. Honeycutt, G. A. Rozgonyi, and R. J. Nemanich, *J. Appl. Phys.*, **71**, 4269 (1992).
11. S. Motakef, J. M. E. Harper, F. M. d'Heurle, T. A. Gallo, and N. Herbots, *J. Appl. Phys.*, **70**, 2660 (1991).
12. J. B. Lasky, J. S. Nakos, O. J. Cain, and P. J. Geiss, *IEEE Trans. Electron Devices,* **ED-38**, 262 (1991).
13. Y. Matsubara, T. Horiuchi, and K. Okumura, *Appl. Phys. Lett.,* **62**, 2634 (1993).
14. P. S. Lee, K. L. Pey, D. Mangelinck, J. Ding, D. Z. Chi, and L. Chan, *IEEE Electron Device Lett.,* **EDL-22**, 568 (2001).
15. F. Deng, R. A. Johnson, P. M. Asbeck, S. S. Lau, W. B. Dubbelday, T. Hsiao, and J. Woo, *J. Appl. Phys.,* **81**, 8047 (1997).
16. J. P. Gambion and E. G. Colgan, *Mater. Chem. Phys.,* **52**, 99 (1998).
17. J. K. Kittl, Q. Z. Hong, H. Yang, N. Yu, S. B. Samavedam, and M. A. Gribelyuk, *Thin Solid Films,* **332**, 404 (1998).
18. Q. Z. Hong, W. T. Shiau, H. Yang, J. A. Kittl, C. P. Chao, H. L. Tsai, S. Krishnan, I. C. Chen, and R. H. Havemann, *Tech. Dig. Int. Electron Devices Meet.,* **1997**, 107.
19. K. Maex, A. Lauwers, P. Besser, E. Kondoh, M. de Potter, and A. Steegen, *IEEE Trans. Electron Devices,* **ED-46**, 1545 (1999).
20. A. Lauwers, P. Besser, M. De Potter, E. Kondoh, N. Roelandts, A. Steegen, M. Stucchi, and K. Maex, *IEEE International Interconnect Technology Conference (IITC)*, p. 99 (1998).
21. T. Morimoto, H. S. Momose, T. Iinuma, I. Kunishima, K. Suguro, H. Okana, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, and H. Iwai, *Tech. Dig. Int. Electron Devices Meet.,* **1991**, 653.
22. T. Ohguro, S. Nakamura, M. Koike, T. Morimoto, A. Nishiyama, Y. Ushiku, T. Yoshitomi, M. Ono, M. Saito, and H. Iwai, *IEEE Trans. Electron Devices,* **ED-41**, 2305 (1994).
23. T. Ohguro, S. Nakamura, E. Morifuji, M. Ono, T. Yoshitomi, M. Saito, H. S. Momose, and H. Iwai, *Tech. Dig. Int. Electron Devices Meet.* **1995**, 453.
24. T. Morimoto, T. Ohguro, S. Momose, T. Iinuma, I. Kunishima, K. Suguro, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, and H. Iwai, *IEEE Trans. Electron Devices,* **ED-42**, 915 (1995).
25. D. X. Xu, S. R. Das, C. J. Peters, and L. E. Erickson, *Thin Solid Films,* **326**, 143 (1998).
26. M. C. Poon, F. Deng, M. Chan, W. Y. Chan, and S. S. Lau, *Appl. Surf. Sci.,* **157**, 29 (2000).
27. A. Lauwers, A. Steegen, M. de Potter, R. Lindsay, A. Satta, H. Bender, and K. Maex, *J. Vac. Sci. Technol. B,* **B19**, 2026 (2001).
28. S. P. Murarka, *Silicides for VLSI Applications*, Academic Press, New York (1983).
29. Y. Tsuchiya, A. Tobioka, O. Nakatsuka, H. Ikeda, A. Sakai, S. Zaima, and Y. Yasuda, *Jpn. J. Appl. Phys., Part 1,* **41**, 2450 (2002).
30. Q. Xiang, C. Woo, E. Paton, J. Foster, B. Yu, and M. R. Lin, *Symposium on VLSI Technology Digest*, p. 76 (2000).
31. R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barkage, B. Doyle, R. Arghavani, A. Murtht, and G. Deewy, *Tech. Dig. Int. Electron Devices Meet.,* **2000**, 45.
32. P. S. Lee, K. L. Pey, D. Mangelinck, J. Ding, A. T. S. Wee, and L. Chan, *IEEE Electron Device Lett.,* **EDL-21**, 566 (2000).
33. R. Mukai, S. Ozawa, and H. Yagi, *Thin Solid Films,* **270**, 567 (1995).
34. M. Y. Tsai and B. G. Streetman, *J. Appl. Phys.,* **50**, 183 (1979).
35. S. S. Lau and N. W. Cheung, *Thin Solid Films,* **71**, 117 (1980).
36. B. Y. Tsui, J. Y. Tsai, T. S. Wu, and M. C. Chen, *IEEE Trans. Electron Devices,* **ED-40**, 54 (1993).
37. T. P. Nolan, R. Sinclar, and R. Beyers, *J. Appl. Phys.,* **71**, 720 (1992).
38. A. A. Brown, P. B. Moynagh, and P. J. Rosser, *Semiconductor Silicon*, **13**, 280 (1989).
39. B. A. Julies, D. Knoesen, R. Pretorius, and D. Adams, *Thin Solid Films,* **347**, 201 (1999).
40. K. Goto, J. Watanabe, A. Fushida, T. Sakuma, and T. Sugii, *IEEE International Reliability Physics Symposium (IRPS)*, p. 363 (1998).