Mechanical Properties in Small Dimensions: Comments from Industry

The following are commentaries provided by representatives from industry. These short articles lend an additional context in which to appreciate the importance of the issues and mechanisms discussed in the technical articles. The authors of the commentaries point out that the basic principles that underlie the influence of scale on material behavior are not only interesting in their own right, but also are directly applicable to issues of great significance to designers and manufacturers of small-scale devices and structures. In addition, directions for future emphasis are suggested.

Richard P. Vinci
Shefford P. Baker
Guest Editors

Control of Stresses in Silicon-Device Manufacturing

In the development and manufacturing of silicon devices, the control of thin-film stresses continues to be a major challenge. High stresses can cause deformation, delamination, cracking, and void formation. They may also directly affect device characteristics. In multilevel interconnections now being developed, low-dielectric-constant insulators are being introduced that have drastically weaker mechanical properties than the glassy SiO_2 used for decades. These factors, together with rapidly decreasing dimensions, require a greater understanding of the origins of thin-film stresses. High stresses are created by thermal-expansion mismatch during the heating cycles required for fabrication, and they are also a by-product of the film microstructure. These microstructure-induced stresses are referred to as "intrinsic" stresses and are the subject of the article by Floro et al. in this issue.

The article provides a discussion of several prior models and mechanisms related to thin-film stresses and gives enough detail to examine the differences experimentally. Since many of the thin films used in silicon devices, such as contacts and diffusion-barrier layers, are barely thicker than their coalescence thickness, a careful evaluation of the mechanisms described by Floro et al. may help to control their properties to even smaller dimensions.

James M.E. Harper
Manager, Thin-Film Metallurgy and Interconnections
IBM T.J. Watson Research Center

Fracture in Small Dimensions

Ensuring long-term integrated-circuit interconnect reliability has always been challenging, given that a single electrical failure of an individual interconnect line or via, among millions of such microfeatures, can destroy the whole chip. Furthermore, a crack need only be of the order of 1 μm in size to cause such a failure. Traditionally, this problem was addressed in two ways: by modifying materials in order to enhance thin-film strength and interface adhesion as well as to reduce various stresses, and by rigorous reliability testing to reveal any weak links that can be fixed by altering local structures. While these approaches were not systematic, they did apply thin-film fracture mechanics empirically or intuitively. In fact, because fracture-related failures were often observed to occur after exposure to moisture or temperature cycles, reliability tests were designed to mimic such environments, and structures—guard rings and passivation layers—were widely used to keep moisture out.

Recently, it is increasingly being recognized that more systematic studies of fracture mechanisms/mechanics are of critical importance. This has been driven by shortened technology-development cycles and the adoption of new interconnect materials such as copper and low-*k* dielectrics. Progress made so far has already provided more accurate root-cause analyses for observed failures and several clear directions for further materials development. Studies are also showing that failure sites in IC interconnects are often isolated with a locally maximized fracture driving force; therefore, eliminating vulnerable structures by using fracture-mechanics-based design rules can dramatically increase the reliability safety margin.

Qing Ma
Technical Manager, Intel Laboratories
Intel Corporation

Diffusion and Stresses in Interconnect Structures

Diffusion processes play an important role in determining the reliability of interconnect structures in semiconducting devices. In particular, diffusional growth of voids in metal lines can cause resistance shifts in interconnects that lead to circuit failure. The driving force for diffusion is frequently a gradient in hydrostatic stress, although shear deformation by diffusional-creep mechanisms can be important in some instances. One of the primary sources of stress is the mismatch in thermal expansion between the metal interconnects and the surrounding dielectric. On cooling from processing temperatures, the metal lines tend to contract more than the surrounding dielectric, resulting in hydrostatic tension in the lines that can exceed 1 GPa. In the

absence of preexisting imperfections, only shear stresses in a line are relaxed. Relaxation of the hydrostatic-stress component requires the nucleation of a void. Once formed, voids can locally relax hydrostatic tension, leading to hydrostatic-stress gradients that drive further void growth. A second process that can lead to void growth is electromigration. In this case, diffusion takes place due to the momentum transfer from an electron flux in the line to metal atoms in the line. The motion of atoms due to the electron "wind" can result in atoms piling up at one end of the line, leaving a void at the other end. In lines that are confined in a dielectric, a corresponding hydrostatic-stress gradient arises that opposes the atom flux. In short lines, this gradient can become sufficient to completely shut down the electromigration flux.

It can be seen that diffusion and void growth in interconnect structures is intimately connected with their stress state. Complete modeling of void-growth phenomena therefore requires simultaneous modeling of both the stress state and diffusional fluxes in the structure. Considerable advances have been made in understanding the behavior of isotropic metal lines encased in a rigid dielectric. While such models are appropriate for the case of aluminum lines encased in an oxide dielectric, more advanced modeling is required when considering the case of anisotropic metals such as copper and soft, low-permittivity dielectrics that are currently being introduced to enhance circuit performance. With anisotropic metals, discontinuities in the elastic modulus can occur on crossing grain boundaries, resulting in grain-to-grain variations in the stress state of a line. Such effects may enhance void nucleation and growth when specific grain orientations or textures are present. An understanding of the specific effects that details of the line microstructure have on void growth is likely to require computer models in which stress and diffusion modeling are linked at the microstructure scale.

A further important aspect of void growth is understanding the diffusion paths that contribute to vacancy fluxes. Rarely is bulk diffusion active at the operating temperatures for semiconductors, and frequently there are multiple parallel paths that contribute to void growth. These may include metal/metal grain boundaries and phase boundaries and metal/dielectric interfaces. In many cases, the addition of small amounts of additives can have a significant effect on diffusion at one or more of these interfaces. A classic example is copper at grain boundaries in aluminum metal lines that can reduce the rate of void growth by electromigration by orders of magnitude. Despite more than 30 years of study, the fundamental origin of this effect has still to be found. Such understanding is likely to require detailed atomistic modeling of the interaction of solutes with grain boundaries as well as simulations of how diffusion processes take place at grain and phase boundaries. Thus, computer modeling has an important role to play in understanding diffusion in interconnects at both the atomistic and microstructural scales.

Thomas M. Shaw
Research Staff Member,
Silicon Technology Department
IBM T.J. Watson Research Center

The Industrial Significance of Understanding Dislocation Behavior in Thin Films

Electrochemically deposited (ECD) copper films are now commonly used in the high-performance microelectronics industry to increase ULSI (ultralarge-scale integration) circuit performance and to reduce manufacturing costs. However, ECD copper has unique physical properties that pose significant challenges during ULSI processing. For example, as-deposited ECD copper thin films are unstable, even at room temperature, due to the small grain size and the presence of a significant number of atomic defects. The grain size is often on the nanometer scale, and the dislocation density can be large, leading to a ~20% higher electrical resistance than in bulk copper. These characteristics are undesirable in an interconnect material.

As a result, atomic defects need to be removed during processing in order to improve circuit performance and device reliability. One of the common techniques is to employ thermal annealing, which promotes grain growth and reduces electrical resistance. However, due to the copper/dielectric thermal-mismatch-induced stress and other unknown mechanisms, trench and via voids can form if the annealing condition is not optimized. To avoid the formation of stress-induced voids, process engineers require knowledge of dislocation-mediated stress-relaxation behavior for different thermal conditions, film textures, and interconnect-structure geometries. Other length-scale-dependent mechanical properties such as strain-gradient plasticity should also be investigated as circuit design layout reduces to sub-0.1-μm dimensions for the coming generations of devices.

Ting Y. Tsui
Member of Technical Staff,
Silicon Technology Research
Texas Instruments Inc.