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Improvement of memory performance by high temperature annealing of the Al_2O_3 blocking layer in a charge-trap type flash memory device

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The effect of postdeposition annealing (PDA) of the Al_2O_3 blocking layer in a charge-trap type memory device is investigated. Significant improvements are achieved by high temperature PDA at 1100 °C, achieving faster operation speed, good charge retention, and a wide program/erase window. Experimental evidence shows that the underlying mechanism is not the changes in the band gap of the crystallized Al_2O_3 but is due to the higher trap density in the Si_3N_4 trapping layer at a deeper energy level by the intermixing between Al_2O_3 and Si_3N_4. The reduced trapping efficiency of the annealed Al_2O_3 also helps improve the retention property. © *2010 American Institute of Physics*. [doi:10.1063/1.3442502]

Charge-trap type memory device, otherwise known as TANOS ($TiN-Al_2O_3-Si_3N_4-SiO_2-Si$), is one of the most promising candidates for next generation flash memory technology. This paper reports that the high-temperature postdeposition annealing (PDA) of Al_2O_3 in a TANOS device can significantly improve the memory performance of the device. It also presents experimental evidence that the dominant mechanism behind such an improvement is not a change in the band structure of Al_2O_3, as expected, but is a change in the charge trapping property of Al_2O_3 and silicon nitride.

After standard gate precleaning, a 4.5 nm thick tunnel oxide (SiO_2) was thermally grown on a p-type Si substrate, and 6 nm thick Si_3N_4 was deposited by low-pressure chemical vapor deposition to form the charge-trapping layer. For the blocking oxide, a Al_2O_3 layer with a thickness of 15 nm was deposited on the top of the nitride layer by means of atomic layer deposition (ALD) using Eureka 3000 from Jusung Engineering. The ALD temperature was fixed at 300 °C. $Al(CH_3)_3$ from UP Chemical Co. was used as a precursor and ozone was used as an oxidant. After the deposition of the Al_2O_3 layer, PDA was performed in the temperature range of 800–1100 °C in a N_2 ambient for 30 s. A 150-nm-thick TaN layer was deposited by reactive sputtering for the gate metal. As plasma etching of crystallized Al_2O_3 can cause plasma-induced damage to the gate stack, the gate stack etching was stopped after the metal gate etching in order to exclude the effect of plasma etch damage. Then, source/drain implantation was done through the dielectric stacks, and all of the samples underwent a rapid thermal annealing process at 900 °C for 30 s for activation of the dopant. The charge trap devices were fabricated with the gate length of 100 μm and width of 100 μm.

Figures 1(a) and 1(b) show a comparison of the program/erase (P/E) characteristics and charge retention properties of TANOS devices with different PDA temperatures. For erase characteristic comparison, the devices were programmed to ΔV_{FB} (programmed V_{FB}—initial V_{FB}) =4 V. To reach ΔV_{FB}=4 V programmed state, programming conditions used were 160 μs, 250 μs, and 100 μs at 18 V for 900 °C, 1000 °C, and 1100 °C annealed samples, respectively. Both the P/E speed and the charge retention property were greatly improved by the high-temperature PDA process, and the improvement is most apparent when the PDA temperature is 1100 °C.

To investigate the mechanism of such an improvement by the high-temperature PDA process, the leakage current performance was initially checked. The results in Fig. 2(a) do not show a reduction in the leakage current due to the high-temperature PDA compared to the low temperature PDA. Therefore, the improved P/E properties after an annealing process at a higher temperature are not likely due to reduced back tunneling current from the gate electrode.

The band structure of the high-temperature annealed Al_2O_3 was also carefully measured by high-resolution x-ray photoelectron spectroscopy (XPS).[1] The result in the inset of

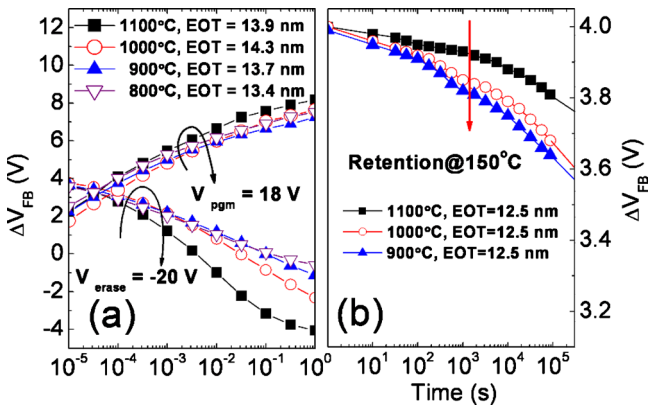

FIG. 1. (Color online) Comparisons of (a) program and erase characteristics and (b) charge retention property of TANOS devices with different PDA temperatures. For more accurate comparison of retention property, the devices with the equal EOT values were selected for (b).

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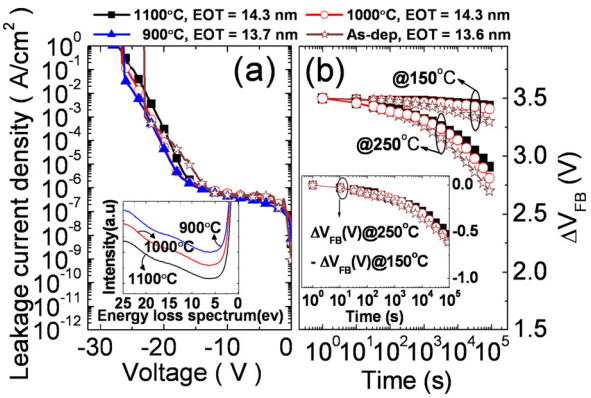

FIG. 2. (Color online) (a) Comparison of the gate stack leakage currents of TANOS devices with different PDA temperatures. The inset shows the energy loss spectrum derived from the O 1*s* spectrum as measured by XPS. (b) Retention property of TANOS devices with different PDA temperatures measured at 150 and 250 °C. The inset is the flat-band voltage difference between 150 and 250 °C (ΔV_{FB} at 250 °C − ΔV_{FB} at 150 °C) as calculated from the results in (b).

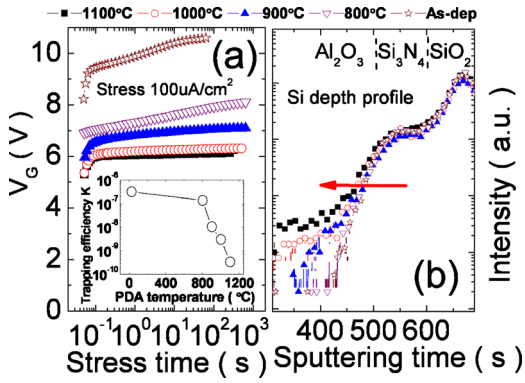

FIG. 3. (Color online) (a) Change in the gate voltage during a constant current stress test of MIM capacitors with Al_2O_3 dielectrics annealed at different temperatures. The inset is the trapping efficiency *K* as a function of the PDA temperature, as calculated from the results in (a). (b) Si depth profiles in the gate stacks after high-temperature PDA, as measured by TOF-SIMS.

Fig. 2(a) shows that there is no meaningful difference in the extracted energy band gap of the annealed Al_2O_3 (E_{G,Al_2O_3} =7.58 eV, 7.59 eV, and 7.59 eV for samples exposed to 900 °C, 1000 °C, and 1100 °C PDA, respectively). This result implies that the improvement of the P/E property and the charge retention characteristics cannot be explained simply in terms of an increase in the conduction band offset of the crystallized Al_2O_3, as claimed in a previous report on Al_2O_3 for floating gate type flash memory devices.[2,3] The high-temperature retention analysis in Fig. 2(b) also supports the fact that there is no difference in the extracted band gap. The higher the temperature becomes, the greater the charge loss is, as shown in Fig. 2(b). If the difference of the charge loss is monitored between 150 and 250 °C, it can be considered to be the pure thermionic emission component of the charge loss.[4] The inset of Fig. 2(b) shows the difference of the charge loss amount monitored by the flat-band voltage difference between 150 and 250 °C (ΔV_{FB} at 250 °C − ΔV_{FB} at 150 °C) calculated from the results in Fig. 2(b). Surprisingly, all of the samples (as-deposited, 1000 °C annealed, and 1100 °C annealed Al_2O_3) show an identical curve, proving that the difference of the charge loss measured at 150 and 250 °C does not depend on the Al_2O_3 PDA temperature. This is strong evidence that the memory performance improvement observed in the Al_2O_3 sample annealed at a high temperature is not due to the increased band gap caused by the crystallization of Al_2O_3.

As another possible mechanism, the trapping property of Al_2O_3 was investigated. For this test, separate samples with metal-insulator-metal (MIM: TaN−Al_2O_3−TaN) capacitor structure were prepared to study the property of the Al_2O_3 dielectric itself. Figure 3(a) shows the change in the gate voltage during a constant current stress test performed on the MIM capacitors. The amount of trapped charge in Al_2O_3 as a function of the injected charge was calculated from the gate voltage shift (not shown here).[5] From the result, the trapping efficiency *K* was extracted.[6] The result of the trapping efficiency *K* in the inset of Fig. 3(a) clearly shows that the trapping efficiency is significantly reduced when the PDA temperature increases. This implies that the trap-assisted tunneling current through the Al_2O_3 defect in a programmed state can be effectively suppressed by a high-temperature PDA process, which in turn improves the retention property.

However, the reduced trapping efficiency of Al_2O_3 alone does not by itself sufficiently explain the significant enhancement of the P/E speed and the window shown in Fig. 1(a). On the other hand, it has been reported that a deeper saturated erase flat-band voltage indicates a higher density of accessible charge traps.[7] Moreover, the properties of the Si_3N_4 trapping layer/Al_2O_3 interface have been postulated to play a key role in the erase mechanism.[8] Based on such considerations, it is speculated that intermixing at the interface between the Al_2O_3 blocking layer and the Si_3N_4 trapping layer may occur during high-temperature PDA, leading to the diffusion of Al into Si_3N_4, which results in yielding additional traps at a deeper trapping energy level. Figure 3(b) shows the Si depth profiles of TANOS gate stacks with different PDA temperatures, as measured by time-of-flight secondary ion mass spectrometry (TOF-SIMS). Additional Si ions diffuse out from Si_3N_4 into the Al_2O_3 blocking oxide due to the higher PDA temperature, which is evidence of intermixing between Al_2O_3 and Si_3N_4. If such intermixing occurs, the diffusion of Al ions toward the Si_3N_4 trapping layer will also take place, resulting in additional traps at a deeper trapping energy level.

The charge loss rate as a function of the PDA temperature was also investigated. Based on the slope of the plot in Fig. 4(a) and the charge loss rate, the relative trap density amount could be extracted as a function of the trap energy level, as shown in Fig. 4(b).[9] The result in Fig. 4(b) shows that the 1100 °C PDA sample has a higher trap density at a deeper trap energy level in the Si_3N_4 trapping layer. Therefore, it can be concluded that the additional traps at the deeper trapping energy level of Si_3N_4 caused by the intermixing between Al_2O_3 and Si_3N_4 during the high-temperature PDA process is the main reason for the improved P/E properties.

Generally in flash memory devices, the charge retention characteristics and a wide erase window (or a fast erase speed) have a trade-off relationship.[10] The real improvement in the charge retention characteristics can only be claimed when both properties are improved together. The result in Fig. 4(c) clearly shows the benefit of the high-temperature PDA of Al_2O_3. In this result, the higher the PDA temperature

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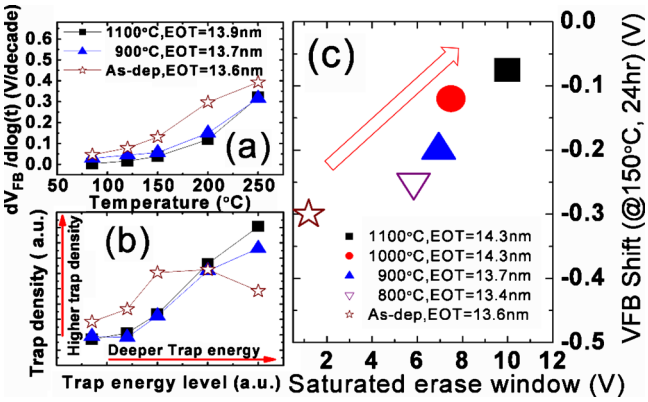

FIG. 4. (Color online) (a) Charge loss rate as a function of the PDA temperature. (b) Relative trap density amount as a function of the trap energy level. (c) A plot of the retention vs the saturated erase window for TANOS devices with different PDA temperatures. The saturated erase window was determined as the change in V_{FB} from the programmed V_{FB} to the V_{FB} which showed the onset of the saturation during the erasing.

becomes, the more the charge retention is improved. As analyzed in Figs. 2–4, the wide erase window and enhanced retention property upon high-temperature PDA contribute to the pre-existing intrinsic Si_3N_4 trap density plus a high trap density at a deeper trap energy level, possibly due to the diffusion of Al ions toward Si_3N_4 and the low trapping efficiency of the annealed Al_2O_3 dielectric which suppresses the trap-assisted tunneling current.

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[1]S. Miyazaki, J. Vac. Sci. Technol. B **19**, 2212 (2001).
[2]J. R. Power, D. Shum, Y. Gong, S. Bogacz, J. Haeupel, H. Estel, R. Strenz, R. Kakoschke, K. van der Zanden, R. Allinger, and G. Jaschke, *Proceedings of the IEEE Non-Volatile Semiconductor Memory Workshop, 2008* (IEEE, Monterey, 2008), p. 93.
[3]D. Wellekens, J. De Vos, J. Van Houdt, and K. van der Zanden, *Proceedings of the IEEE Non-Volatile Semiconductor Memory Workshop, 2008* (IEEE, Monterey, 2008), p. 12.
[4]Y. Wang and M. H. White, Solid-State Electron. **49**, 97 (2005).
[5]J. Buckley, G. Molas, M. Gély, F. Martin, B. De Salvo, S. Deleonibus, G. Pananakakis, C. Bongiorno, and S. Lombardo, *Proceedings of the European Solid-State Device Research Conference, 2006* (IEEE, Montreux, 2006), p. 246.
[6]C. Papadas, G. Ghibaudo, G. Pananakakis, C. Riva, and P. Mortini, J. Appl. Phys. **71**, 4589 (1992).
[7]M. Sadd, J. A. Yater, J. Bu, C. M. Hong, W. M. Paulson, C. T. Swift, R. Singh, L. Parker, and M. G. Khazhinsky, *IEEE Non-Volatile Semiconductor Memory Workshop* (IEEE, New York, 2003), p. 71.
[8]S.-C. Lai, H.-T. Lue, J.-Y. Hsieh, M.-J. Yang, Y.-K. Chiou, C.-W. Wu, T.-B. Wu, G.-L. Luo, C.-H. Chien, E.-K. Lai, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, IEEE Electron Device Lett. **28**, 643 (2007).
[9]Y. Yang and M. H. White, Solid-State Electron. **44**, 949 (2000).
[10]S. Y. Wang, H. T. Lue, P. Y. Du, C. W. Liao, E. K. Lai, S. C. Lai, L. W. Yang, T. Yang, K. C. Chen, J. Gong, K. Y. Hsieh, R. Liu, and C. Y. Lu, IEEE Trans. Device Mater. Reliab. **8**, 416 (2008).

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