AIP Applied Physics Letters

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Citation: Applied Physics Letters **96**, 082904 (2010); doi: 10.1063/1.3313946
View online: http://dx.doi.org/10.1063/1.3313946
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/96/8?ver=pdfcov
Published by the AIP Publishing

Bilayer metal oxide gate insulators for scaled Ge-channel metal-oxide-semiconductor devices

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(Received 17 December 2009; accepted 18 January 2010; published online 23 February 2010)

We investigate the electrical properties of germanium-channel metal-oxide-semiconductor capacitors with an amorphous atomic-layer-deposited (ALD)-Al_2O_3 interlayer (IL) and higher-k ALD-TiO_2 gate dielectric. An ALD-Al_2O_3 IL of ~1 nm thickness reduces the gate leakage current density at the otherwise low band-offset TiO_2/Ge interface by six orders of magnitude at flatband. Devices with the thinnest Al_2O_3 IL exhibited a low capacitance equivalent thickness of 1.2 nm. The hysteresis of the capacitance-voltage curves was <10 mV for $TiO_2/Al_2O_3/Ge$ capacitors with different Al_2O_3 thicknesses. We obtained a relatively low minimum density of interface states, D_{it} $\sim 3\times 10^{11}$ cm^{-2} eV^{-1}, suggesting the potential of Al_2O_3 ILs for higher-k/Ge interface passivation. © *2010 American Institute of Physics*. [doi:10.1063/1.3313946]

Aggressive dimensional scaling of field-effect-transistors (FETs) has prompted interest in high mobility channel materials like germanium as an alternative to conventional Si-based complementary-metal-oxide-semiconductor (MOS) devices. The difficulty of controlling the stoichiometry and achieving thin physical thickness of GeO_2 surface layers on Ge motivates studies of high-k gate dielectrics on Ge.[1] The figure of merit, f, for direct tunneling-limited gate leakage current density of a gate stack is $f=k\sqrt{\phi_b}$ where k is the dielectric constant of the gate dielectric and ϕ_b is the tunnel barrier height.[2] Empirically, it is found that the inverse scaling behavior of ϕ_b and permittivity makes dielectrics with $k\sim 40$ especially suitable for future scaling,[3] prompting interest in oxide gate insulators with k higher than that of HfO_2 (~20), the state-of-the-art gate dielectric for Si-based MOS devices. Also, an important requirement for the high-k gate dielectric is a conduction band offset (CBO) to the semiconductor channel in excess of 1 eV,[4–6] to minimize gate leakage current density. Titanium dioxide (TiO_2) is a potential candidate for a higher-k dielectric with the bulk rutile crystalline phase of TiO_2 exhibiting k values as high as 60–80.[4] However, TiO_2 is predicted to possess zero CBO to Si or Ge substrates.[4] Therefore, there is a need to engineer ultrathin, large band gap interlayers (ILs) between Ge FET channels and higher-k oxides that would, by themselves, have low band offsets to Ge.

Aluminum oxide is promising as an IL owing to its excellent thermal stability, large band gap (~8.8 eV for the α-Al_2O_3 crystalline phase) and moderately-high dielectric constant ($k\sim 8$ in the bulk oxide[4]) to enable continued gate capacitance scaling. Atomic layer deposition (ALD) is an important tool to fabricate these proposed ILs because it offers precise, monolayer-level thickness control.[7] In this study, we report on the application of *in situ* deposited ALD-Al_2O_3 ILs between the Ge channel and the overlying higher-k TiO_2 layer.

Acceptor-doped (Ga, 2 Ω cm resistivity) Ge (100) substrates were given a de-ionized (DI) H_2O clean for five minutes to remove the native oxide, blown dry with N_2 and transferred immediately to the high-vacuum loadlock of an ALD chamber. ALD-Al_2O_3 ILs of different thicknesses (0.8, 1.2, and 3 nm) were deposited at 250 °C from 8, 12, and 30 cycles of a trimethyl aluminum (TMA)/H_2O process. Forty cycles of ALD-TiO_2 deposition (~7 nm) were performed using a tetrakisdimethylamino titanium/H_2O process *in situ* after Al_2O_3 deposition to fabricate p-Ge/Al_2O_3/TiO_2 structures. These bilayer samples will be henceforth referred to as 8 IL, 12 IL, and 30 IL for different Al_2O_3 IL thickness (8, 12, and 30 cycles), respectively. A control sample

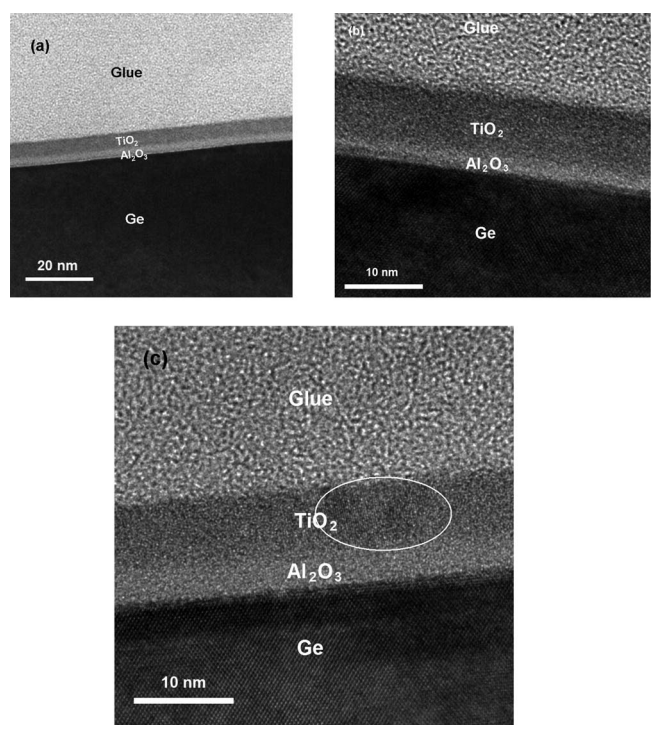

FIG. 1. Cross-sectional TEM images of the bilayer stacked structure (a) 30 IL sample showing smooth, conformal deposition, and well-defined Al_2O_3/Ge and TiO_2/Al_2O_3 interfaces (b) as-deposited 12 IL sample with amorphous Al_2O_3 and TiO_2 (c) Postannealed 30 IL sample with partially crystalline TiO_2 region highlighted within an oval.

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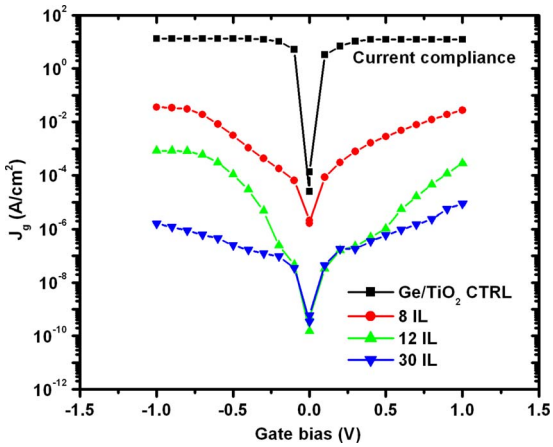

FIG. 2. (Color online) Gate leakage characteristics (J–V) of Pt-gated MOS capacitors: CTRL, 8 IL, 12 IL, and 30 IL. The insertion of an Al_2O_3 IL at the TiO_2/Ge interface is beneficial in reducing the gate leakage by six orders of magnitude at V_{fb}.

(CTRL) was prepared by depositing 40 cycles of TiO_2 (~4 nm) directly on the DI H_2O cleaned-Ge substrate. Platinum gate metal of 50 nm thickness was deposited by e-beam evaporation through a shadow mask, followed by deposition of a 15 nm Ti/50 nm Al backside contact to reduce the contact resistance. Postmetal forming gas annealing (FGA) (5% H_2/95% N_2) was done on these capacitors for 30 min at 350 °C. Parallel-mode, bidirectional, multifrequency capacitance–voltage (C–V) sweeps on these MOS capacitors were carried out using a HP4284A precision LCR meter. Leakage current density–voltage (J–V) measurements used a Keithley 230 programmable voltage source and electrometer. The density of interface states, D_{it}, was extracted by low temperature conductance measurements[8] in a cryostation at 230 K to ensure factors such as thermal generation and weak inversion response that interfere with D_{it} extraction at room temperature were avoided.[9,10]

Cross-sectional transmission electron microscopy (XTEM) was done using Tecnai G2 microscope operating at 200 kV, to inspect the microstructure and thickness of the samples. Figure 1(a) shows an XTEM image of the 30 IL bilayer stacked structure indicative of smooth, conformal ALD of ~3 nm Al_2O_3 and ~7 nm TiO_2 over a large surface area, with well-defined, nearly-abrupt Al_2O_3/Ge and TiO_2/Al_2O_3 interfaces. The similarity in atomic numbers of Ge and Al limits the ability of TEM to distinguish between possible interfacial GeO_x and Al_2O_3. However, the sharp nature of the Al_2O_3/Ge interface and Al_2O_3 thicknesses consistent with deposition rates for our TMA/H_2O process (~0.1 nm/cycle) are indicative of an ultrathin GeO_x layer of thickness less than the limit of resolution for measurements of imperfect/disordered interfaces in the microscope (<2 Å layer thickness). The as-deposited Al_2O_3 and TiO_2 films were amorphous, consistent with the low deposition temperatures employed during ALD [Fig. 1(b) for the 12 IL sample]. Thickness calibration of the TiO_2 growth on the Al_2O_3 starting surface revealed an enhanced deposition rate of ~0.17 nm/cycle when compared to ALD-TiO_2 on DI-H_2O cleaned Ge(100) (0.1 nm/cycle for the CTRL sample), suggestive of a smaller incubation regime for ALD-TiO_2 on Al_2O_3 than on the virgin Ge(100) surface. While the TiO_2 layer was observed by TEM to be amorphous in most electron-transparent regions after the FG anneal; we observed a partially crystalline TiO_2 region in one postannealed 30 IL TEM sample, indicated by finely spaced lattice fringes [Fig. 1(c)].

Figure 2 plots the leakage current density, J, as a function of the gate bias for the Pt-gated as-deposited bilayer stack structures. The CTRL sample exhibited high leakage current densities reaching the current compliance of the electrometer (13 A/cm^2 areal current density), as shown in Fig. 1. This is likely a consequence of the low CBO at the TiO_2/Ge interface. The introduction of an ultrathin Al_2O_3 IL (8 IL and 12 IL) reduces the leakage current significantly, by approximately six orders of magnitude at the flatband voltage (V_{fb}). This is evidence of reduced tunneling of carriers across the gate stack resulting from the increased CBO and greater insulator thickness caused by the introduction of the Al_2O_3 IL. Consistent with this observation, an experimental value of 2.85 eV has been reported for the CBO for the Al_2O_3/Ge interface.[11] The gate leakage current density further reduces to $\sim 8\times10^{-8}$ A/cm^2 at V_{fb} for the 30IL sample, consistent with an exponential reduction in direct tunneling current with the IL thickness. In comparison, it should be pointed out that a Pt/30cyc ALD-Al_2O_3 (3 nm)/Ge MOS capacitor exhibits a leakage current of 2.2×10^{-4} A/cm^2 at V_{fb}, three orders of magnitude higher than the 30 IL sample (data not shown).

Figure 3 shows the bidirectional C–V sweeps of postannealed stacks with different IL thickness from 1 to 100 kHz. Multifrequency correction for the series resistance R_s was done[8] but an inconsistent value for R_s was obtained from the three samples. The stack with the thinnest Al_2O_3 IL (8 IL) has a low capacitance equivalent thickness (CET) of 1.2 nm [Fig. 3(a)]. This suggests that, with ultrathin deposited ILs,

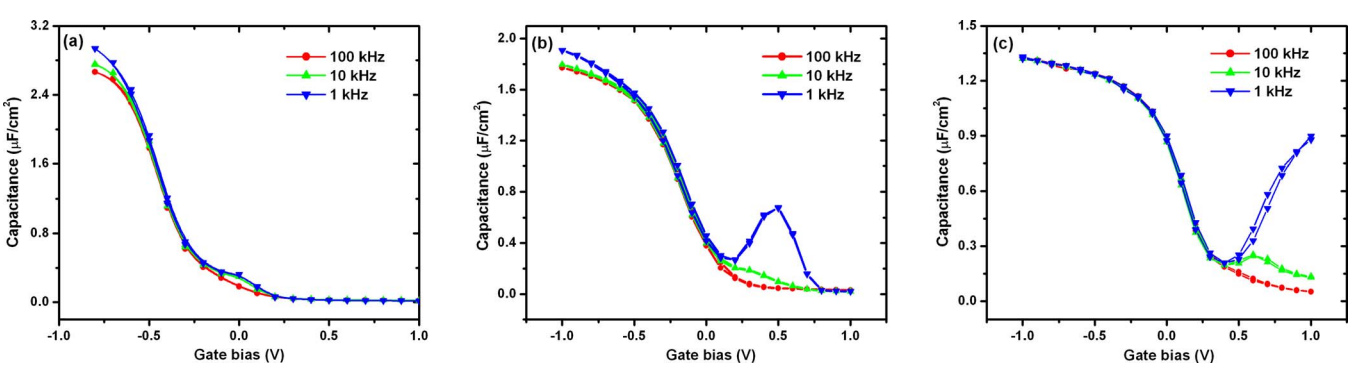

FIG. 3. (Color online) Capacitance–voltage (C–V) characteristics of postannealed, Pt-gated MOS capacitors (a) 8 IL, (b) 12 IL, and (c) 30 IL. Sample 8 IL shows a low capacitance-derived electrical thickness of 1.2 nm.

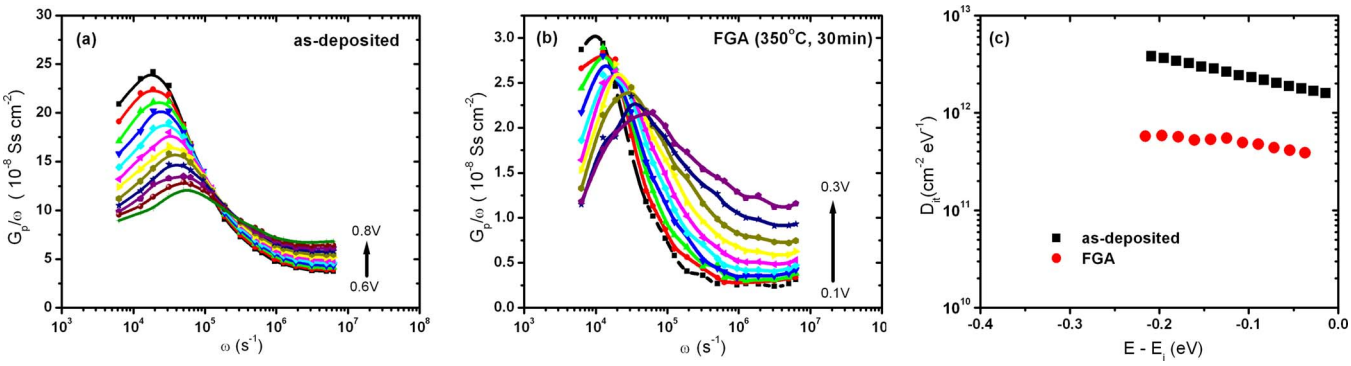

FIG. 4. (Color online) Parallel conductance loss peaks (G_p) in the frequency domain for (a) as-deposited 12 IL sample (b) Postannealed 12 IL sample. (c) D_{it} distribution in the p-type Ge band gap for as-deposited and postannealed 12 IL samples. D_{it} extraction was done by conductance measurements at 230 K.

subnanometer equivalent oxide thickness (EOT) can potentially be reached if the substrate capacitance is taken into consideration (beyond the scope of this study). The CETs for the 12 IL and 30 IL stacks were observed to be 1.8 and 2.5 nm, respectively [Figs. 3(b) and 3(c)]. Assuming a k value of 7 for the ALD-Al_2O_3 layer, as determined in our previous studies,[12] k for TiO_2 was calculated from the C–V plots and TEM thickness calibration to be in the range of 32–35. This k value is lower than the expected value of ~60 for bulk rutile phase, as described earlier, and is attributed to the largely amorphous nature of the ALD-TiO_2. The hysteresis for all three samples was observed to be <10 mV at V_{fb}, indicative of low density of defects contributing to charge trapping in the IL and the TiO_2 film. The frequency dispersion in accumulation appears to decrease as the IL thickness increases [Figs. 3(a)–3(c)]. This suggests an increasing influence of traps in the dielectric layers on the measured C–V characteristics as the Al_2O_3 IL is thinned down. The V_{fb} is observed to shift toward positive gate bias as we increase the IL thickness. This shift is consistent with a large negative fixed charge incorporated in Al_2O_3/Ge stacks. As will be reported elsewhere,[12] the fixed charge for these ALD-Al_2O_3/Ge stacks resides predominantly at the interface rather than in the "bulk" of the Al_2O_3 layer.

We performed low temperature conductance measurements on the 12 IL sample to extract the interface state density (D_{it}). The weak inversion response that gives rise to the "bump" in the 1 kHz curve at room temperature [Fig. 3(b)] is completely suppressed at 230 K (not shown). Figures 4(a) and 4(b) show the interface trap conductance G_p/ω, as a function of the angular frequency ω, in the depletion-to-weak inversion surface potential regime for the as-deposited and the post-FGA stacks, respectively. It can be seen that the conductance in the post-FGA case is an order of magnitude less for the as-deposited gate stack. Figure 4(c) shows the D_{it} distribution across a portion of the Ge band gap, extracted from the conductance peaks for both the as-deposited and FG annealed samples. It is evident that FGA reduces the D_{it} significantly, both at midgap and approaching the band edges. The minimum D_{it} of the postannealed samples was calculated to be 3×10^{11} cm^{-2} eV^{-1}. This indicates that the electrical quality of the interface is comparable to that reported for much thicker, stoichiometric GeO_2 surface passivation layers on Ge.[10,13] The extent to which FGA promotes H-induced passivation of dangling bonds is unclear. *Ab initio* simulations and some experimental results suggest that Ge dangling bond defects are negatively charged and are unlikely to be passivated by atomic hydrogen, which also behaves an acceptor in Ge.[14,15] Water-vapor based, oxidant-rich ALD promotes residual –OH incorporation in as-deposited oxide thin films. The interaction of atomic hydrogen with –OH groups in the high-k oxide may cause monolayer-level oxidation of the Ge (100) surface, producing GeO_2-like bonding which has been shown to provide a passive interface.[16]

In summary, we have demonstrated that ultrathin Al_2O_3 ILs deposited by *in situ* ALD are effective in reducing gate leakage at the low-CBO, TiO_2/Ge interface. We were able to scale down the CET of these devices to 1.2 nm, indicating the capacitance scaling potential of such bilayer stacks. We have also established that FGA is beneficial in lowering the interface state density; annealed devices exhibited a minimum $D_{it}\sim3\times10^{11}$ cm^{-2} eV^{-1} near midgap. This study suggests the potential of ALD-Al_2O_3 ILs as a route to achieving interface passivation in higher-k/Ge MOS devices.

This research was supported by the MSD FCRP Focus Center and Stanford INMP. S.S acknowledges financial support from the Yansouni Stanford Graduate Fellowship.

[1] Y. Kamata, Mater. Today **11**, 30 (2008).
[2] Y. Yeo, T.-J. King, and C. Hu, Appl. Phys. Lett. **81**, 2091 (2002).
[3] P. W. Peacock and J. Robertson, J. Appl. Phys. **92**, 4712 (2002).
[4] J. Robertson, Eur. Phys. J.: Appl. Phys. **28**, 265 (2004).
[5] J. Robertson, J. Vac. Sci. Technol. B **18**, 1785 (2000).
[6] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[7] M. Ritala, M. Leskelä, J.-P. Dekker, C. Mutsaers, P. J. Soininen, and J. Skarp, Chem. Vap. Deposition **5**, 7 (1999).
[8] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1981).
[9] K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, IEEE Trans. Electron Devices **55**, 547 (2008).
[10] D. Kuzum, T. Krishnamohan, A. J. Pethe, A. K. Okyay, Y. Oshima, S. Yun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, IEEE Electron Device Lett. **29**, 328 (2008).
[11] V. V. Afanas'ev, A. Stesmans, A. Delabie, F. Bellenger, M. Houssa, and M. Meuris, Appl. Phys. Lett. **92**, 022109 (2008).
[12] S. Swaminathan, Y. Oshima, and P. C. McIntyre (unpublished).
[13] A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. V. Elshocht, M. Caymax, M. Heyns, and M. Meuris, Appl. Phys. Lett. **91**, 082904 (2007).
[14] V. V. Afanas'ev, Y. G. Fedorenko, and A. Stesmans, Appl. Phys. Lett. **87**, 032107 (2005).
[15] R. Weber, A. Janotti, P. Rinke, and C. G. Van de Walle, Appl. Phys. Lett. **91**, 142101 (2007).
[16] Y. Oshima, Y. Sun, D. Kuzum, T. Sugawara, K. C. Saraswat, P. Pianetta, and P. C. McIntyre, J. Electrochem. Soc. **155**, G304 (2008).