AIP Applied Physics Letters

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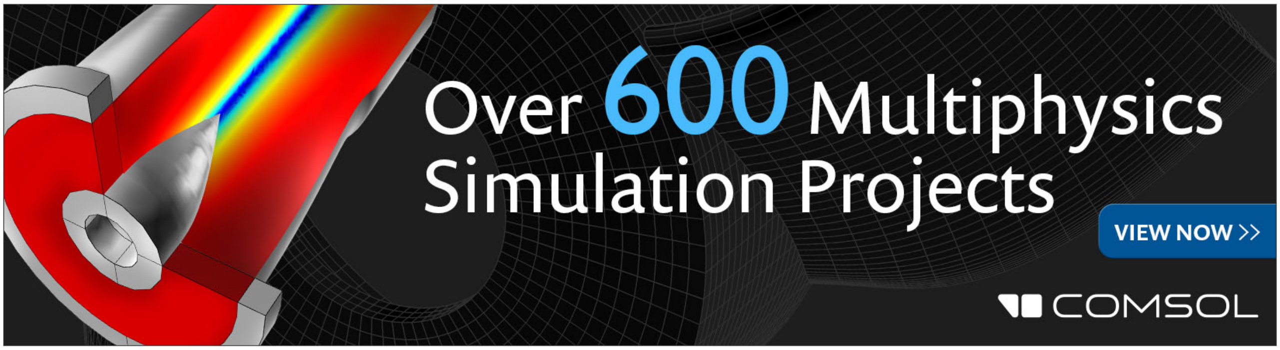
Citation: Applied Physics Letters **93**, 113506 (2008); doi: 10.1063/1.2987428
View online: http://dx.doi.org/10.1063/1.2987428
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/93/11?ver=pdfcov
Published by the AIP Publishing



APPLIED PHYSICS LETTERS **93**, 113506 (2008)

Comparison of *n*-type and *p*-type GaAs oxide growth and its effects on frequency dispersion characteristics

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The electrical characteristics of *n*- and *p*-type gallium arsenide (GaAs) capacitors show a striking difference in the "accumulation" capacitance frequency dispersion. This difference has been attributed by some to a variation in the oxide growth, possibly due to photoelectrochemical properties of the two substrates. We show that the oxide growth on *n*- and *p*-type GaAs substrates is identical when exposed to identical environmental and chemical conditions while still maintaining the diverse electrical characteristics. The difference in electron and hole trap time constants is suggested as the source of the disparity of the frequency dispersion for *n*-type versus *p*-type GaAs devices. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2987428]

Gallium arsenide (GaAs) metal oxide semiconductor (MOS) capacitors have long been known to display a frequency dispersion of the "accumulation" capacitance.[1–7] This phenomenon has been attributed to a high density of interface traps (D_{it}) and the associated Fermi level pinning arising from problems associated with native or deposited oxides.[8–11] This dispersion is significantly more pronounced on an *n*-type GaAs surface than for a *p*-type substrate.[12,13] Previous studies on molecular beam epitaxy grown GaAs and air-grown native oxides on *n*- and *p*-type GaAs have suggested that there is an inherent stability to maintain a low surface-state density for the *p*-type substrates compared to the *n*-type surfaces.[14,15] The differences in the stabilities have been attributed to photoelectrochemical properties of the two surfaces in which illuminated GaAs surfaces oxidize differently.[12,15] In this letter, *n*-type and *p*-type GaAs substrates were carefully treated and exposed to identical chemical and phototreatments in an effort to determine the oxidation differences of the two surfaces and their effect on the electrical characteristics of MOS capacitors.

The samples used in this work were *n*-type Si-doped GaAs wafers and *p*-type Zn-doped GaAs wafers with doping concentration of $1-4\times10^{17}$ cm^{-3}. The GaAs surfaces were prepared by degreasing the wafers in acetone, methanol, and isopropyl alcohol for 1 min each, followed by a 3 min etch in 29% NH_4OH.[16] *In situ*, 1.0 nm Al_2O_3 thin films were deposited on GaAs in a Picosun SUNALE® atomic layer deposition (ALD) reactor integrated to an ultrahigh vacuum (UHV) multitechnique deposition/characterization system (base pressure$=2\times10^{-11}$ mbar)[17] at a substrate temperature of 300 °C and a base pressure of ~7 Torr. Trimethyl aluminum was used as the precursor for Al_2O_3 formation. The oxygen source was de-ionized H_2O. Analysis of the chemically treated GaAs surfaces and deposited films was done using *in situ* monochromatic x-ray photoelectron spectroscopy (XPS) using an Al $K\alpha$ (1486.7eV) x-ray source with a line width of ~0.25 eV and pass energy of 15 eV. The *n*-type and *p*-type samples were removed from sealed containers simultaneously and were subjected to identical atmospheric, chemical, and UHV conditions at all times as companion specimens until capped with a gate metal electrode. The native oxides of freshly unpacked samples were analyzed using XPS to ensure that the starting surfaces were chemically identical (not shown). The samples were then exposed to atmospheric conditions and ambient fluorescent lighting for 30 min prior to chemical treatment. After chemical exposure, the wafers were exposed to the same ambient (laboratory air and lighting) conditions for (a) 12 min or (b) 5 min preceding pumpdown to UHV. The surfaces after degrease and chemical treatment were then analyzed using XPS (not shown) and also display the same chemical bonding to within the level of detection of XPS for both *n*-type and *p*-type substrates, regardless of ambient exposure. It is noted that the 12 min *ex situ* exposure between chemical cleaning and introduction to the UHV environment has been shown previously to be long enough to reoxidize the surface to near completion (assuming no passivation), while the 5 min exposure time should have an incomplete reoxidation.[18] This previous work then implies that the indistinguishable oxides of the *n*-type and *p*-type substrates are not due to minimal atmospheric exposure or due to a saturation of the oxides during reoxidation. After the initial ALD and analysis, another 9 nm of Al_2O_3 was deposited (10 nm total) and the samples were removed from UHV and annealed at 600 °C for 60 s in 99.999% pure N_2. The TaN gate electrodes were deposited by rf sputtering through shadow masks. Ohmic contacts were formed by depositing Ti/Au for *p*-type GaAs and Ni/Au/Ge for *n*-type GaAs each annealed at 450 °C for 60 s in N_2.[19]

The background-subtracted normalized XPS spectra of the two companion GaAs substrates with chemical treatment followed by 12 min atmospheric exposure and 1 nm deposition of ALD Al_2O_3 (Fig. 1) fully overlap, clearly showing that the surfaces exhibit the same bonding environment to within detectable limits. The NH_4OH does not passivate the GaAs surface and, therefore, does not inhibit oxide growth in air [in contrast to $(NH_4)_2S$ treatment],[20] and was chosen as a chemical treatment specifically for this reason. Of particular note are the ratios of the As–O and Ga–O bonding to their respective bulk peaks in the As $2p$ and Ga $2p$ spectra. The

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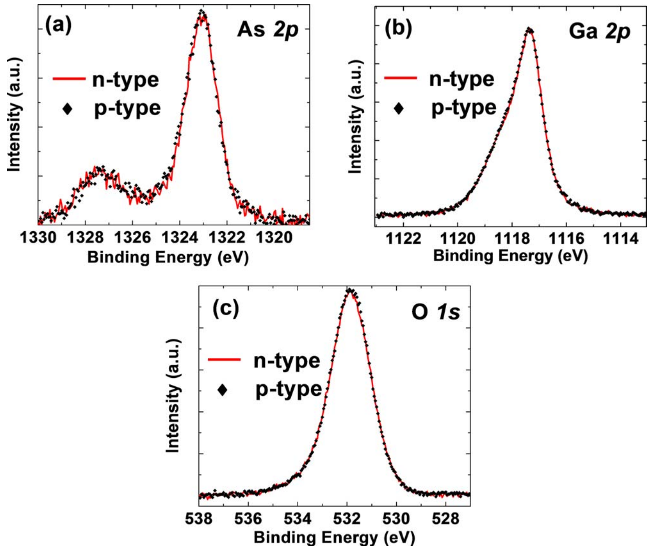

FIG. 1. (Color online) XPS data of (a) As 2*p*, (b) Ga 2*p*, and (c) O 1*s* spectra for *n*- and *p*-type GaAs surfaces after chemical treatment, 12 min atmospheric and fluorescent lighting exposure, and 1 nm Al_2O_3 deposition.

oxide growth and chemical states of those oxides are identical for both *n*- and *p*-type surfaces despite the fact that the surfaces were illuminated, suggesting that there was no detectable photoelectrochemical reaction from ambient light among the two substrates. Moreover, the O 1*s* spectrum shows the bonding environment and total amount of surface oxygen to be identical for the two wafers. Figure 2 shows the two types of GaAs substrates with chemical treatment followed by 5 min atmospheric exposure and 1 nm deposition of ALD Al_2O_3. The extent of oxidation on these samples, while being noticeably different from the 12 min exposure samples, is chemically identical to each other for an *n*-type and a *p*-type substrate. This shows that there is no difference detected in the oxidation rate or chemical state of the *n*- or *p*-type substrates as long as they are exposed to identical conditions. It is noted that the As 2*p* and Ga 2*p* spectra are very surface sensitive due to the binding energies of those core level electrons and are therefore particularly useful in analyzing interfacial oxides. All other individual spectral ranges analyzed (Al 2*p*, As 3*d*, Ga 3*d*, and C 1*s*) also show identical chemical states for both *n*-type and *p*-type substrates (not shown).

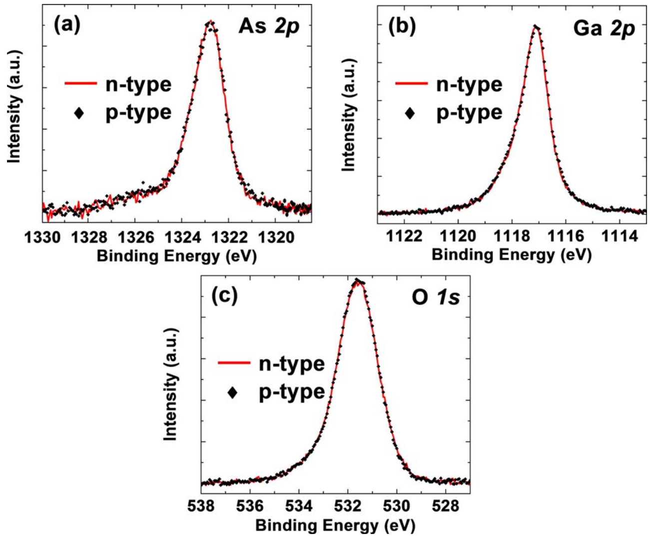

FIG. 2. (Color online) XPS data of (a) As 2*p*, (b) Ga 2*p*, and (c) O 1*s* spectra for *n*- and *p*-type GaAs surfaces after chemical treatment, 5 min atmospheric and fluorescent lighting exposure, and 1 nm Al_2O_3 deposition.

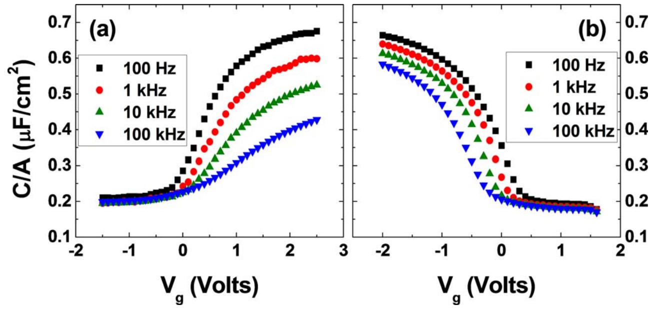

FIG. 3. (Color online) *C-V* data of the same samples used for XPS analysis showing different (a) *n*-type and (b) *p*-type frequency dispersion characteristics despite having chemically identical gate oxides and interfaces.

The XPS spectra shown have been aligned to the *n*-type Ga–As bulk peak binding energy for direct comparison of the chemical states of the two substrates and their overlayers. The difference in binding energy between the same core level electrons (for example, the Ga 2*p* photoelectrons) of *n*-type versus *p*-type substrates arises due to the differences of the Fermi levels as well as band bending associated with oxide charge.[21,22] As the binding energy of the photoelectrons is measured with respect to the Fermi level, the *n*-type substrate shows a higher binding energy for the core levels with respect to photoelectrons from the *p*-type sample, and we have therefore shifted the *p*-type curves to a higher binding energy. The actual peak shifts were 0.15 eV for Fig. 1 (As 2*p* positions at 1322.85 and 1323.0 eV, Ga 2*p* positions at 1117.25 and 1117.4 eV, and O 1*s* positions at 531.7 and 531.85 eV) and 0.3 eV for Fig. 2 (As 2*p* positions at 1322.4 and 1322.7 eV, Ga 2*p* positions at 1116.8 and 1117.1 eV, and O 1*s* positions at 531.3 and 531.6 eV). The curves shown have all been normalized in counts as well in order to show the relative ratios of the oxides to the bulk signals for each of the spectra.

Having established that the *n*-type and *p*-type substrates have indistinguishable interfacial oxides and bonding environments, perusal of the corresponding MOS capacitor electrical characteristics is quite revealing. Figure 3 shows the capacitance-voltage (*C*-*V*) characteristics of the same *n*-type and *p*-type GaAs substrates and dielectrics analyzed by XPS. These characteristics are typical of oxides on GaAs when compared to published literature.[1–4] The fact that the frequency dispersion is clearly distinct between the two starting surfaces with the same interfacial chemistry strongly indicates that the observed dispersion is not due to a different surface-state density caused by dissimilar oxide growth on the two types of substrates.

Rather, these data suggest that the source of the different electrical characteristics is due to a difference in time constants of electron and hole interface traps in this system. Simulations of capacitance-voltage characteristics have been performed to demonstrate the effects of various factors on the electrical characteristics of MOS devices.[3] Two separate models have been employed in this effort. The first is a classical formulation using numerically calculated oxide, substrate, and interface trap capacitances using surface potentials derived from total semiconductor charge.[23] The second

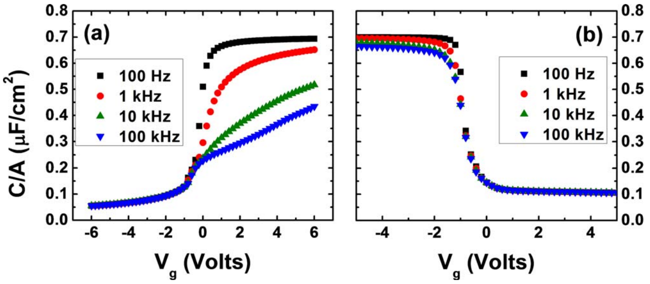

FIG. 4. (Color online) Simulated *C-V* data using a tunneling modified interface state model. The D_{it} distribution is the same for both (a) *n*-type and (b) *p*-type simulations as suggested from the XPS data. The simulation differences arise from trap time constant differences for electrons and holes.

modifies the classical model by introducing a lower bandgap interfacial region along the lines of the model suggested by Hasegawa and Sawada.[24] Using a D_{it} distribution similar to those suggested in prior reports[9,24,25] (although any distribution shows qualitatively similar results), the modified model produces the *C-V* curves shown in Fig. 4. Based on these models, the reason for the differences in the *n*- and *p*-type simulated *C-V* curves stems from the differences in the capture time constants for electrons and holes, respectively. These time constants vary with differences in the conduction and valence band densities of states, capture cross sections of electrons versus holes, and any energetic asymmetries in the D_{it} distribution.[23,24] We also note that reaching the assumed value of oxide capacitance (C_{ox}) is not necessarily evidence of an accumulation layer. The high D_{it} results in a very small number of free carriers in accumulation and an associated small substrate capacitance as compared to the interface state capacitance. Because of the extremely high interface state capacitance at low frequency, the total capacitance in accumulation is close to C_{ox} despite a very small number of free carriers present.

In summary, we have shown that oxide growth on *n*-type and *p*-type GaAs surfaces are identical under matching environmental conditions and cannot be the origin of the observed difference in capacitance dispersion of devices made on the two substrates. No photoelectrochemical reaction variation between the two starting surfaces before or after chemical treatment or after dielectric deposition was detected. The difference in electron and hole trap time constants is the source for the disparity of the capacitance frequency dispersion for *n*-type versus *p*-type GaAs devices.

This work is supported by the National Institute of Standards and Technology, Semiconductor Electronics Division, the FCRP Materials Structures and Devices (MSD) Center, and the U.S./Korea FUSION project.

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