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Defect reduction in Ge_xSi_{1-x} epitaxy by rapid thermal processing chemical vapor deposition using a low-temperature *in situ* preclean and a Si buffer layer

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For chamber base pressure $\approx 5\times10^{-4}$ mbar in a rapid thermal processing chemical vapor deposition system, a 900 °C H_2 prebake for 60 s results in relatively high defect densities in the Ge_xSi_{1-x} epitaxial layer due to surface damage caused by the H_2 prebake. We have demonstrated that a very low thermal budget *in situ* preclean (800 °C/15 s) can reduce the defect densities. In addition, the use of a Si buffer layer grown at 1000 °C for 60 s prior to the Ge_xSi_{1-x} growth is capable of significantly reducing defect densities.

Preparation of the substrate prior to growth plays a critical role in any Si epitaxial growth technique. For chemical vapor deposition (CVD), the typical approach is to perform an *ex situ* clean (e.g., RCA clean[1]) and then form a thin protective layer (typically oxide) over the wafer before loading into the reactor. A high-temperature H_2 (also with HCl) prebake is the most common method of *in situ* cleaning used to remove the oxide and expose the atomically clean Si surface for epitaxial growth. A considerable amount of work has been done to reduce the contribution of the *in situ* clean to the total process thermal exposure. Numerous novel methods have been demonstrated for low-temperature *in situ* cleaning involving plasmas, ion beams, and ultra high vacuums. Recently, considerable interest has been directed toward utilization of a simple HF clean without rinsing with deionized (DI) water. The method is based on the hydrogen passivation effect at temperatures below $\approx$400 °C.[2] Hydrogen passivation has been observed to be stable in air for several tens of minutes,[2] with epitaxial growth demonstrated at 550 °C by molecular beam epitaxy[2] and from $\approx$425 to $\approx$650 °C and $>$750 °C by ultrahigh vacuum CVD (UHV/CVD).[3]

However, the most convenient and readily adaptable method is still a simple H_2 prebake. Therefore, we have examined the approach of reducing the processing temperature and time of the conventional H_2 prebake. Conventional H_2 prebakes are performed at temperatures $\geqslant$ 1000 °C at pressures on the order of 10–100 Torr. The reaction of O_2 and H_2O with the Si surface has been extensively studied.[4,5] At high O_2 and H_2O partial pressures and low substrate temperatures, the surface is covered with SiO_2 via the net reactions of $Si(s)+O_2(g)\rightarrow SiO_2(s)$ and $Si(s)+2H_2O(g)\rightarrow SiO_2(s)+2H_2(g)$. At low O_2 and H_2O partial pressures and high substrate temperatures, the surface is free of SiO_2 due to the production of volatile SiO via the net reactions of $2Si(s)+O_2(g)\rightarrow 2SiO(g)$ and $Si(s)+H_2O(g)\rightarrow SiO(g)+H_2(g)$. The four net reactions are part of a growth-etch model characterizing the nature of the Si surface and oxide under various processing conditions.

Several low-temperature epitaxial growth techniques, such as UHV/CVD[6] and atmospheric pressure CVD,[7] have been successfully demonstrated based on operation in a region of the growth-etch model that allows for an oxide-free surface. The most important factor is the reduction of O_2 and H_2O partial pressures. The development of epitaxial reactors with low base pressures and low leak rates has resulted in lower background levels of impurities, allowing lower temperatures for *in situ* cleaning and epitaxial growth.[8] A H_2 prebake temperature as low as 850 °C for 5 min at 10 Torr has been reported.[9] Provided the partial pressures of O_2 and H_2O are kept below the critical values for a given temperature, the fast oxide etching rates reported by Ghidini and Smith[5] should allow the prebake time to be reduced to seconds. Studies of SiO_2 thermal decomposition in an ultrahigh vacuum, N_2, or Ar ambient indicate that voids form through the oxide to the Si surface and grow via reaction of SiO_2 with Si atoms diffusing to the periphery of the voids.[10] Thus, the continued and nonuniform etching may cause surface damage in a prolonged and/or high-temperature prebake process.

We have studied the use of lower H_2 prebake temperatures for epitaxial growth by rapid thermal processing CVD (RTPCVD).[11] RTPCVD, similar to limited reaction processing[12] and rapid thermal CVD,[13] has received considerable attention because of its ability to reduce many of the processing problems associated with thermal exposure in conventional CVD, such as autodoping, outdiffusion, and the inability to reproducibly grow thin layers. The precise temperature and time control of RTPCVD is advantageous for studying the effects of prebake conditions on wafer surface damage. In this letter, we report the effects of prebake temperature and time on defect densities in epitaxial Ge_xSi_{1-x} layers grown by RTPCVD. H_2 was used as the carrier gas while SiH_2Cl_2 and GeH_4 were used as the source gases. The H_2 purity was 99.9995% ($H_2O<1$ ppm), the SiH_2Cl_2 purity was 99.9%, and the GeH_4 purity was 99.99% ($H_2O<10$ ppm). No additional in-line purification was performed on the process gases. Chamber base pressure was used as an indicator of the background moisture level. At the typical chamber base pressure used ($\sim10^{-4}$ mbar), the partial pressure of water vapor already in the chamber is orders of magnitude higher than the water vapor partial pressure introduced by the process

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TABLE I. Summary of growth parameters and defect densities. All samples were grown with a SiH_2Cl_2 flow rate of 20 sccm, a GeH_4 flow rate of 0.5 sccm, and a H_2 flow rate of 979.5 sccm for a total gas flow rate of 1 lpm.

Sample No.	H_2 prebake	Ge_xSi_{1-x} deposition	Base pressure ($\times 10^{-4}$ mbar)	Defect density ($\times 10^3$ cm^{-2})
122	900 °C/60 s	900 °C/180 s	5	800
123	850 °C/60 s	900 °C/180 s	5	500
124	800 °C/60 s	900 °C/180 s	5	20
256	800 °C/60 s	1000 °C/120 s	4	30
257	800 °C/15 s	1000 °C/120 s	4	10
263	800 °C/15 s	900 °C/180 s	5	100
264	800 °C/15 s	1000 °C/60 s (Si buffer layer) 900 °C/180 s	5	3
265	800 °C/15 s	1000 °C/60 s (Si buffer layer) 850°C/180 s	5	3

gases under typical process flow rates.

Each (100)Si wafer was etched in dilute HF and rinsed in DI water prior to loading into the chamber. The process gases were introduced into the chamber when the chamber pressure reached the desired base pressure. The chamber pressure during processing was 5 Torr. All samples were grown with a SiH_2Cl_2 flow rate of 20 sccm, a GeH_4 flow rate of 0.5 sccm, and a H_2 flow rate of 979.5 sccm for a total gas flow rate of 1 lpm. Data on the samples are summarized in Table I. The defect densities listed are for defects in the epitaxial layer that have propagated to the surface and do not include misfit dislocation densities.

The Nomarski micrographs of samples 122 and 124 are shown in Fig. 1. For samples 122–124 defect densities of 8×10^5, 5×10^5, and 2×10^4 cm^{-2} are observed for 60 s H_2 prebakes at 900, 850, and 800 °C, respectively. Since our processing was not performed in a clean room environment and no elaborate *ex situ* clean was done before loading the wafers into the chamber, the defect densities can be expected to be no better than 10^2–10^3 cm^{-2}. The results indicate that for our reactor conditions, lowering the prebake temperature from the conventional prebake temperature of 1000 down to 800 °C can reduce the surface damage and the resulting defects in the Ge_xSi_{1-x} epitaxial layer.

For samples 256–257, the H_2 prebake was performed at 800 °C for 60 and 15 s, yielding defect densities of 3×10^4 and 1×10^4 cm^{-2}, respectively. The defect density for sample 256 is slightly higher than for sample 124, despite the fact that the deposition temperature for 256 is higher, possibly because of the slightly lower chamber base pressure. We have observed a significant increase (orders of magnitude) in defect density for Si epitaxial growth when the chamber base pressure is reduced from 7×10^{-4} to 1.5×10^{-4} mbar.[14]

In one set of runs, we experienced difficulty in obtaining low defect densities (e.g., sample 263). We suspect that the problem may have been due an improperly performed *ex situ* clean. We grew samples 264–265 to study the effectiveness of a Si buffer layer in reducing the defect densities. We have observed that Si epitaxial layers grown at 1000 °C had very low defect densities ($\leqslant 10^3$ cm^{-2}), even when prebake conditions were such that significant surface damage could be expected.[14] We attribute the improved crystalline quality primarily to the higher surface mobility of the adsorbed Si species at higher growth temperatures.

Nomarski micrographs of samples 263 and 265 are shown in Fig. 2. Sample 263 was grown under the same conditions as sample 124 with exception that the H_2 prebake was shortened from 60 to 15 s. The trend set by samples 256–257 and by work with Si epitaxy[14] indicates that the defect density should decrease with the shortened

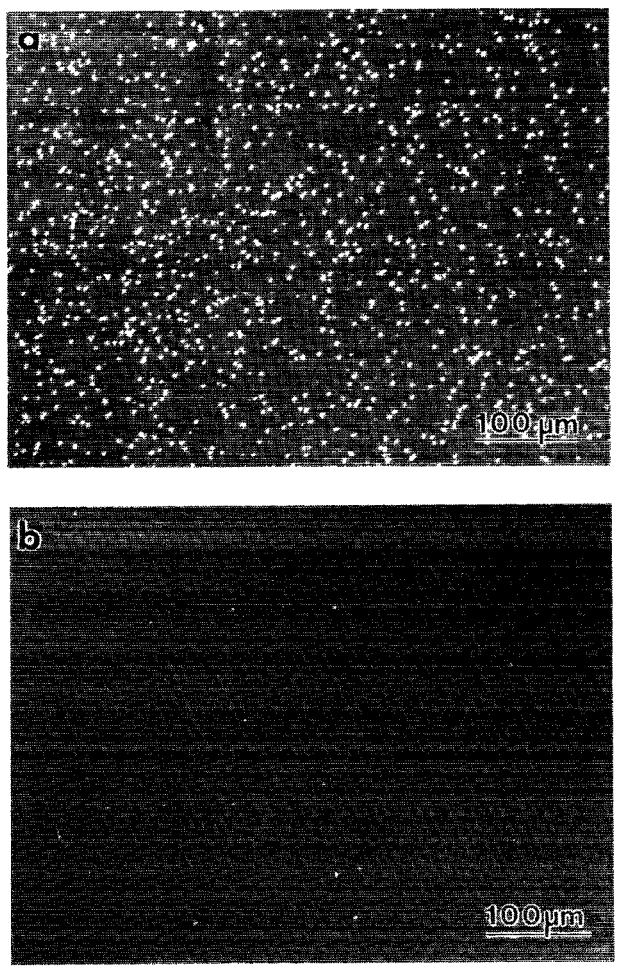

FIG. 1. Nomarski micrographs of epitaxial Ge_xSi_{1-x} layers with a 60 s H_2 prebake at (a) 900 °C and (b) 800 °C.

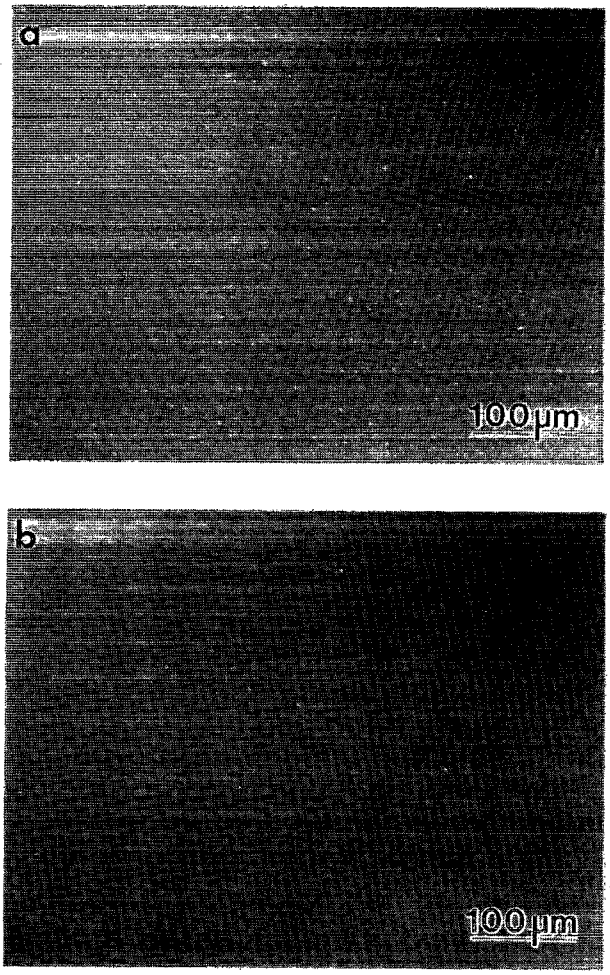

FIG. 2. Nomarski micrographs of epitaxial Ge_xSi_{1-x} layers grown (a) without and (b) with a 1000 °C Si buffer layer.

prebake. However, due to the *ex situ* clean problem, the defect density for sample 263 (1×10^5 cm^{-2}) is significantly higher than the defect density for sample 124 (2×10^4 cm^{-2}). For sample 264, conditions were identical to sample 263 with the exception that a Si buffer layer was grown for 60 s at 1000 °C with a SiH_2Cl_2 flow rate of 20 sccm prior to the growth of the Ge_xSi_{1-x} layer. The defect density of 3×10^3 cm^{-2} for sample 264 is two orders of magnitude lower than the defect density for sample 263.

Sample 265 was grown at 850 °C with all other conditions similar to sample 264, including the Si buffer layer. Again, the defect density of 3×10^3 cm^{-2} for sample 265 is two orders of magnitude lower than the defect density for sample 263. Under 1000× magnification, a slight surface roughness was observed for sample 265. Since the surface roughness could not be accurately resolved by the microscope and the exact cause of the surface roughness (most likely reduced surface mobility of the adsorbed Si species due to the lower growth temperature) is not known, the defect density for sample 265 does not include any defects that might be associated with the surface roughness.

In summary, we have demonstrated that the defect densities in our Ge_xSi_{1-x} layers are strongly dependent upon the H_2 prebake temperature and time. In general, lower chamber base pressures, higher prebake temperatures, and longer prebake times introduce more surface damage, resulting in increased defects in the Ge_xSi_{1-x} layer. However, without lowering the chamber base pressure to the 10^{-4} Torr range, the lower prebake temperatures were ineffective in removing surface oxides. A high temperature Si buffer layer provides a much better surface for the subsequent growth of Ge_xSi_{1-x}. We have demonstrated that a H_2 prebake of 800 °C for 15 s is sufficient for Si and Ge_xSi_{1-x} epitaxial growth with defect densities in the 10^3 cm^{-2} range. We believe that the prebake thermal budget (temperature and time) can be further decreased.

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[1] W. Kern and D. A. Puotinen, RCA Rev. **31**, 187 (1970).
[2] S. S. Iyer, M. Arienzo, and E. de Fresart, Appl. Phys. Lett. **57**, 893 (1990).
[3] B. S. Meyerson, F. J. Himpsel, and K. J. Uram, Appl. Phys. Lett. **57**, 1034 (1990).
[4] F. W. Smith and G. Ghidini, J. Electrochem. Soc. **129**, 1300 (1982).
[5] G. Ghidini and F. W. Smith, J. Electrochem. Soc. **131**, 2924 (1984).
[6] B. S. Meyerson, Appl. Phys. Lett. **48**, 797 (1986).
[7] T. O. Sedgwick, M. Berkenblit, and T. S. Kuan, Appl. Phys. Lett. **54**, 2689 (1989).
[8] J. A. Friedrich, G. W. Neudeck, and S. T. Liu, Appl. Phys. Lett. **53**, 2543 (1988).
[9] V. J. Silvestri, K. Nummy, P. Ronsheim, R. Bendernagel, D. Kerr, V. T. Phan, J. O. Borland, and J. Hann, J. Electrochem. Soc. **137**, 2323 (1990).
[10] R. Tromp, G. W. Rubloff, P. Balk, F. K. LeGoues, and E. J. van Loenen, Phys. Rev. Lett. **55**, 2332 (1985).
[11] S. K. Lee, Y. H. Ku, and D. L. Kwong, Appl. Phys. Lett. **54**, 1775 (1989).
[12] J. F. Gibbons, C. M. Gronet, and K. E. Williams, Appl. Phys. Lett. **47**, 721 (1985).
[13] M. L. Green, D. Brasen, H. Luftman, and V. C. Kannan, J. Appl. Phys. **65**, 2558 (1989).
[14] T. Y. Hsieh, K. H. Jung, and D. L. Kwong (unpublished).