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The Influence of Moisture Barrier Films in ZnO-Based Thin Film Transistors

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We investigated the impact of ALD-deposited moisture barrier films on the stability of ZnO and HfZnO thin film transistors. While the device without a moisture barrier film showed a large turn-on voltage shift under negative bias temperature stress, the suitably protected device with the lowest water vapor transmission rate showed a dramatically improved device performance. As the water vapor transmission rate of the barrier films decreased, the turn-on voltage instability was reduced. The charge trapping model alone could not explain this stability improvement. Instead, the improvement was attributed to effective blockage of bias-enhanced moisture in the ambient atmosphere during gate voltage stress.

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Transparent thin film transistors (TFTs) based on oxide semiconductors have been intensively studied as alternative active matrix backplanes for next-generation flat panel displays. Oxide semiconductor-based TFTs have several advantages compared to conventional amorphous silicon (a-Si) TFTs including their low temperature processing, excellent uniformity due to the amorphous nature of the oxide, and high saturation field effect mobility.[1–4] Moreover, they are transparent in the visible range. A significant amount of research has been devoted to the most promising applications including TFT backplanes for active matrix liquid crystal displays (AMLCD) and active matrix organic light emitting diode (AMOLED) displays. Since the report by Nomura et al., InGaZnO semiconductors, in particular, have received considerable attention, and flat panel displays utilizing amorphous InGaZnO TFTs as active matrix backplanes have been successfully fabricated.[5,6] However, the electrical properties of oxide semiconductors are significantly affected by interactions with the outside atmosphere. Jeong et al. reported that the channel of InGaZnO TFTs is very sensitive to water vapor adsorption. The water molecules induce the formation of an accumulation layer of extra electron carriers in the a-InGaZnO film. In addition, it was shown that the positive V_{th} shift during positive bias stress is not only due to charge trapping, but also to the dynamic interaction between the exposed backchannel and the ambient atmosphere.[7,8] Therefore, water vapor barrier films are necessary for the long-term stability of oxide-based TFTs. Also, OLEDs are sensitive to moisture (H_2O) and oxygen (O_2), which can cause device degradation, and must be protected from these species.[9] Simple calculations, primarily based on the degradation of the OLED cathode material when exposed to water vapor, suggest that the water vapor protection layer must provide a barrier that limits the water vapor permeation rate to less than 10^{-6} g/m^2/day in order to achieve a device lifetime of 10,000 hours at room temperature. In FPD (flat panel display) fabrication processes such as AMLCD and AMOLED, a water vapor barrier film or encapsulation layer will also cover the TFT backplane. To date, various organic or inorganic protection layers such as polymers, SiO_2, SiN_x, and Al_2O_3 have been investigated.[10–13] There has been no report on the relationship between the water vapor transmission rate (WVTR) and characteristics of oxide semiconductor TFTs. In this regard, we investigated the atomic layer deposition (ALD) of Al_2O_3 and TiO_2 thin films as water vapor barrier films and their suitability for stable ZnO-based TFTs.

Experimental

Figure 1a shows a cross-sectional schematic of a bottom-gate ZnO-based TFT with a staggered structure. The devices were prepared on heavily doped n-type silicon substrates containing a buffered gate insulator (plasma enhanced chemical vapor deposition SiO_2 layer of 10 nm /low pressure chemical vapor deposition SiN_x layer of 100 nm). A 40-nm-thick channel layer was grown using a DC magnetron sputtering system. A 4-inch-diameter target was placed 4 cm from the substrate, and a base pressure of 2.7×10^{-4} Pa, a working pressure of 6.6×10^{-1} Pa, and a plasma discharge power density of 0.5 W/cm^2 were applied. The channel was patterned using shadow masks with a channel length and width:length ratio of 100 μm and 10:1, respectively. After S/D (Mo) electrode deposition, Al_2O_3 and TiO_2 barrier films were deposited using a plasma enhanced atomic layer deposition (PEALD) system. The barrier layer was etched using a dilute HF solution for the S/D contact. After deposition, the devices were subjected to thermal annealing at 300°C for 60 min in ambient air. The precursors used in the PEALD of the Al_2O_3 and TiO_2 films were trimethylaluminum (TMA) and tetrakis(dimethylamino)titanium (TDMATi), respectively. The TMA and TDMATi sources were injected into the reaction chamber without a carrier gas. The injection times of the TMA, TDMATi, and O_2 plasma were fixed at 0.1 s, 1 s, and 10 s, respectively. The total cycle consisted of four steps to deposit the multilayer structure. The first and third step sequences consisted of TMA (0.1 s)/Ar (20 s)/O_2 plasma (10 s)/Ar (20 s), while the second and fourth steps included TDMATi (1 s)/Ar (20 s)/O_2 plasma (10 s)/Ar (20 s). The multilayer stacks with alternating Al_2O_3 and TiO_2 layers were deposited repeatedly. To control the thickness of the Al_2O_3 and TiO_2 layers, the number of repeated cycles was varied. The temperatures of the TMA and TDMATi sources were maintained at 20°C by a cooling system and at 40°C by a heating system, respectively, and the base pressure inside the reactor was maintained at 13.3 Pa. The device structure was analyzed using high resolution transmission electron microscopy. The channel layer had a polycrystalline structure regardless of Hf insertion, as shown in Fig. 1b. It was confirmed in the micrograph that the amorphous water vapor barrier film was well formed on the device. Electron cyclotron resonance (ECR) plasma was used for deposition of the water vapor barrier layers because it is produced as a high density plasma under low pressure, and substrate damage due to ion collisions is not a major concern because no electrode was present. The ECR plasma power and the deposition temperature were varied from 100 to 700 W and from 40 to 100°C, respectively. In order to measure the WVTR of the water vapor barrier films, a 200-μm-thick 50×50 mm^2 polyethersulfone (PES) substrate was employed. Prior to the deposition of the barrier films, the PES substrate was washed with isopropyl alcohol (IPA) and methanol in an ultrasonic bath before drying in a stream of nitrogen. The measurements of the WVTR were carried out at 38°C and 100% RH using a PERMATRAN W 3/33 (Modern Controls, Inc.). All electrical characterizations were performed using a semiconductor parameter analyzer (Agilent HP 4145B) at room temperature in the dark. To investigate the density of the deposited films, X-ray reflectometry (XRR, PANalytical X'Pert PRO) was utilized.

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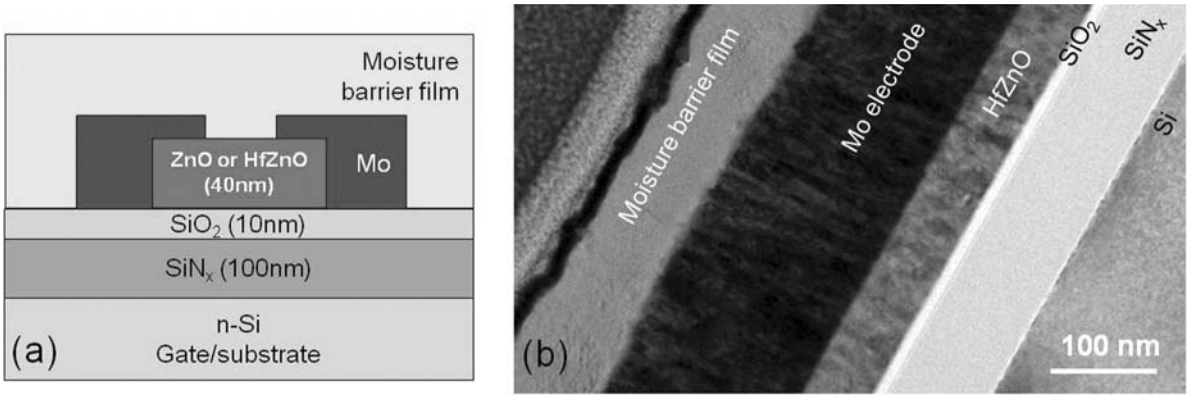

Figure 1. (a) Cross-sectional schematic of a bottom-gate-type ZnO-based TFT with a staggered structure and (b) TEM cross-sectional image of a HfZnO TFT with a TiO_2 water vapor barrier film.

Results and Discussion

Figure 2 shows the dependence of the growth rate and density of the Al_2O_3 and TiO_2 films on the plasma power, which was varied in the range of 100 to 700 W at a deposition temperature of 80°C. The growth rate and density of the Al_2O_3 and TiO_2 films increased when the plasma power was increased from 100 to 500 W. At a plasma power of 700 W, however, the growth rate and density decreased. It appears that the O_2 plasma reactant was accompanied by energetic ion bombardment, resulting in plasma damage at a high plasma power. Also, when the density of the films increases, it is expected that the WVTR value of the films will slightly increase as the plasma power increases due to plasma-induced damage to the films.[14]

To date, considerable effort has been undertaken to develop simple single layer barrier coatings, but their resulting performance has not been adequate for the most demanding next-generation electronics applications. The newly designed multilayer deposition approach provides adequate barrier properties (including buffer layer deposition). The basic idea is to have multilayers separated by an inorganic film, the purpose of which is to decouple the growth of defects from one layer to another. Figures 3a and 3b display the WVTR as a function of (a) film thickness and (b) deposition temperature for three different types of barrier films (single layer, buffered, and multilayer) deposited on a PES substrate. To investigate the effect of a buffered barrier layer or multilayer structure, single layer (Al_2O_3 and TiO_2), buffered barrier layer (Al_2O_3 (30 nm)/TiO_2 (10 nm)), and multilayer (Al_2O_3 (10 nm)/TiO_2 (10 nm)/Al_2O_3 (10 nm)/TiO_2 (10 nm)) films with thicknesses of 40 nm were prepared. As the film thickness and deposition temperature were increased, the WVTRs of the three samples showed decreasing tendencies. Compared to the bare PES film (50 g/m^{2}day), the TiO_2 and Al_2O_3 films showed considerable improvement of the WVTR. However, in the case of a single layer, although the thickness and deposition temperature increased, the WVTR did not reach the detection limit of the measurement system (5×10^{-3} g/m^2 day). The most widely quoted value for the required WVTR for an OLED is 10^{-6} g/m^{2}day. However, none of the commercially available systems based on these techniques meet the sensitivity requirements for the

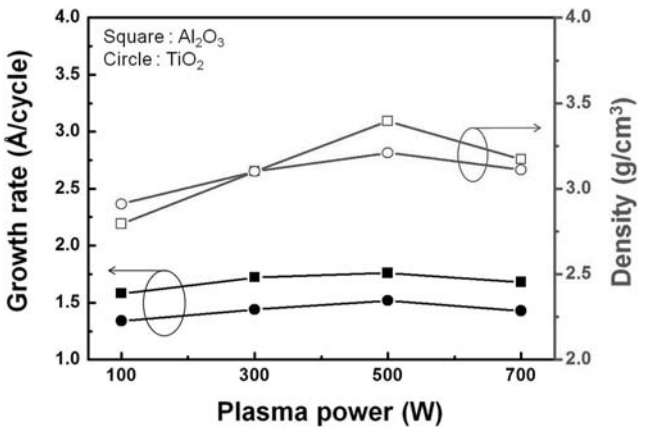

Figure 2. The growth rate and packing density of Al_2O_3 and TiO_2 films as a function of plasma power.

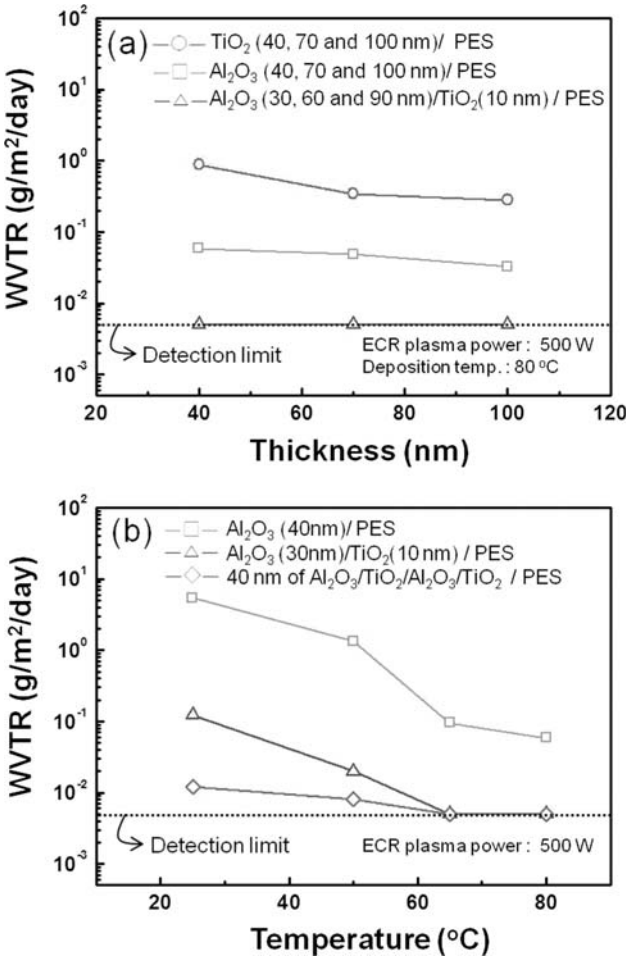

Figure 3. The WVTR values of the water vapor barrier films as a function of (a) film thickness and (b) deposition temperature.

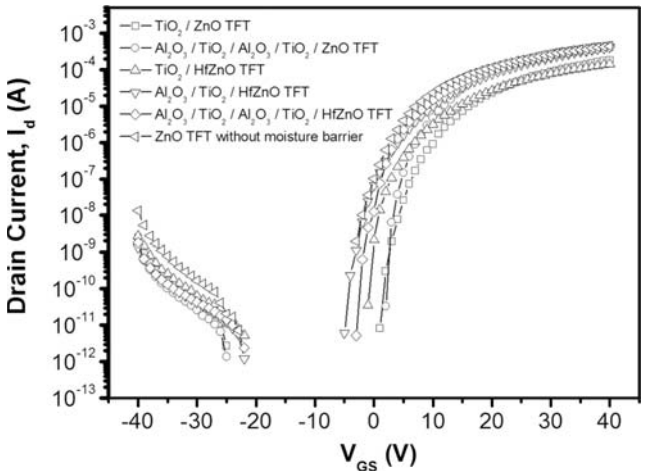

Figure 4. Transfer characteristics of ZnO and HfZnO TFTs with different water vapor barrier films. The devices had a width of 1,000 μm, a length of 100 μm, and $V_{DS} = 1$ V.

low permeation rates required for OLEDs. In this study, the minimum measurable WVTR value using the PERMATRAN W 3/33 system was 5×10^{-3} g/m^2 day. The system could be used to obtain the relative WVTR characteristics of the films.

In order to protect the film from plasma damage, a 10-nm-thick TiO_2 layer was first deposited at a plasma power of 100 W as a buffer layer. Next, dense, amorphous Al_2O_3 and TiO_2 films were alternately deposited onto the buffer layer. All buffered barrier layers and multilayers exhibited a WVTR less than the detection limit above a deposition temperature of 65°C and a thickness of 40 nm. Therefore, it was shown that the individual layers in a buffered barrier layer or multilayer can act to effectively block moisture penetration.

In order to investigate the relationship between moisture and the TFT oxide characteristics, three kinds of barrier films were prepared on the ZnO and HfZnO TFTs. The atomic ratio of Hf in the HfZnO film analyzed by inductively coupled plasma mass spectroscopy (ICPMS) was 0.8 atom%. Figure 4 and Table I show the transfer curves and the device parameters, respectively, of the ZnO TFTs and HfZnO TFTs after the deposition of barrier films and annealing at 300°C. The apparent field-effect mobility, which is defined as $\mu_{FE} = Lg_m/WC_iV_{DS}$, was extracted using the transconductance measured at a low drain voltage ($V_{DS} \leq 1$ V), where W is the channel width, L is the channel length, C_i is the gate capacitance per unit area of the gate insulator, and g_m is the transconductance. The subthreshold swing (SS), defined as the voltage required to increase the source-to-drain current by a factor of 10, was calculated from $SS = dV_{GS}/d(\log I_{DS})$, where SS was the maximum slope in the transfer curve expressed in the log scale for $V_{GS} < V_{ON}$.

Table I. Comparison of the electrical properties of ZnO and HfZnO TFTs.

Water vapor barrier film structure	μ_{FE} (cm^2/V s)	I_{ON}/I_{OFF}	SS (V/decade)	V_{ON} (V)
TiO_2/ZnO TFT	1.00	1.84×10^8	0.64	1
Multilayer/ZnO TFT	5.37	3.33×10^8	0.44	2
TiO_2/HfZnO TFT	2.08	4.50×10^7	0.56	−1
Buffered barrier layer/HfZnO TFT	5.12	3.49×10^8	0.50	−5
Multilayer/HfZnO TFT	6.23	4.96×10^8	0.48	−3
ZnO TFT without a barrier[18]	6.14	6.13×10^7	2.24	−3

Possible explanations for the transfer characteristic changes of the TFTs were examined. The transfer characteristic changes including μ_{FE} and SS can be explained by (*i*) plasma induced damage and (*ii*) ambient effects. The field-effect mobilities (μ_{FE}) of the multilayer and buffered barrier layer TFTs were comparable to each other and were higher than those of the other TFTs. The decreased mobilities of the TFTs with a TiO_2 barrier layer indicate plasma damage due to the direct barrier deposition process. In general, μ_{FE} is affected by shallow traps near the conduction band, and the interaction of oxygen vacancies and zinc interstitials is an important source of n-type conductivity in ZnO.[15] During the O_2 plasma process, ionized oxygen with a high bombardment energy enters active layers and reduces the oxygen vacancies at the top surface of the channel layer and thereby decrease the mobility. Therefore, suppressing the defect-related plasma damage with the buffer layer deposition process can effectively protect the channel layers. Also, the SS values of the TiO_2 barrier layer TFTs were higher than those of the other devices. The increase in SS value can be attributed to the increase in total trap density in deep-level states in the channel layer including the interface trap and bulk trap density.[16,17] It can be noted that the similar SS value for the TiO_2 barrier TFTs suggests an increase of the total trap density caused by plasma damage during the barrier deposition process. Also, the μ_{FE} and SS values of the ZnO TFT without the barrier deposition process were higher and lower than that of the TFT subjected to the direct barrier deposition process, respectively. It is possible that the 10-nm-thick TiO_2 buffer layer effectively prevented the plasma-induced damage that occurs during water vapor barrier deposition. These results indicate that the plasma-induced damage during the direct deposition process on the channel layer may be responsible for degradation of the TFT properties.

As mentioned above, the device characteristic changes of the μ_{FE} and SS values can be attributed to interactions between the active backchannel and the ambient environment. It is well known that adsorbed oxygen/moisture can capture/release an electron and the resulting adsorbed species form a depletion/accumulation layer in the channel, respectively. Furthermore, water vapor adsorption involves trap creation in the channel layer, which is in contrast to oxygen adsorption.[7,8] The traps can be in either the shallow state or deep level state in the forbidden bandgap of the oxide semiconductor. It is believed that an increase in the deep state trap density is the dominant mechanism causing the degradation of the SS value. In addition, the traps created due to water vapor adsorption are in the deep-level state. However, in this work, water vapor adsorption is not the dominant origin of the transfer characteristic changes because, if this were the case, simultaneous deterioration of the μ_{FE} and SS values would not be observed.

Figures 5b–5d show the variations in ΔV_{ON} shift, SS/SS_0, and μ_{FE}/μ_{FE0} values as a function of time for the HfZnO TFT without a barrier film, the ZnO TFT without a barrier film, and the HfZnO TFT with a TiO_2 barrier film, respectively. As shown in Figs. 5a–5c, there was very little change in the ΔV_{ON} shift, SS/SS_0, and μ_{FE}/μ_{FE0} values for roughly 21 days in ambient air when the device was fabricated without a barrier layer. Otherwise, the μ_{FE}/μ_{FE0} ratio of the HfZnO TFT with a TiO_2 barrier film decreased to about 60% of the initial value after 30 days in ambient air. It is noted that, even though a barrier layer was beneficial to maintain the ΔV_{ON} and SS/SS_0 values, the barrier layer deposition process accompanied by plasma-induced damage resulted in a reduction of the initial value of μ_{FE}. This is in agreement with the assumption that plasma-induced damage results in transfer characteristic changes and thus a degraded μ_{FE} value. This indicates that ambient effects can be excluded as the possible reason for the changes in transfer characteristics. Therefore, we can conclude that plasma-induced damage more likely resulted in the transfer characteristics changes of the devices. As a result, the multilayer and buffer layer barrier deposition processes (protecting the channel layers from the plasma-induced damage) play an important role in the achievement of superior device performance.

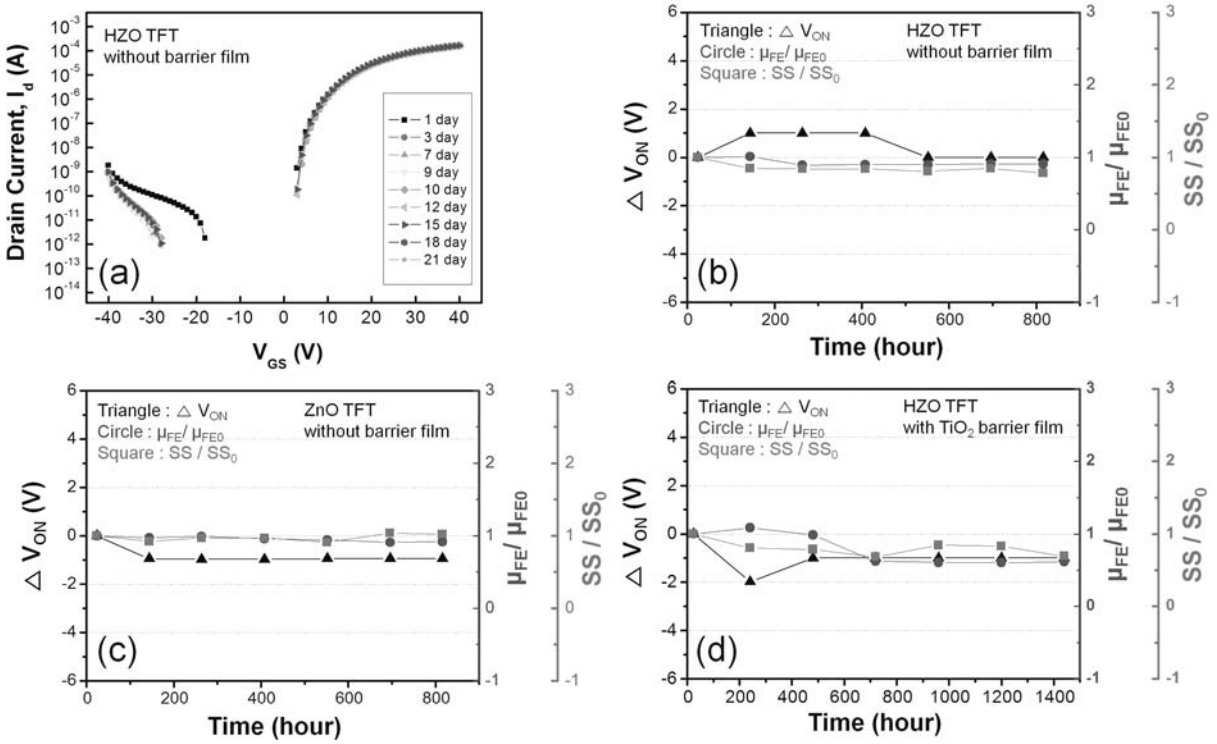

Figure 5. The variations in ΔV_{ON} shift, SS/SS_0, and μ_{FE}/μ_{FE0} values for (a, b) the HfZnO TFT without a barrier film, (c) the ZnO TFT without a barrier film, and (d) the HfZnO TFT with a TiO_2 barrier film as a function of time in ambient air.

Figures 6a and 6b show the evolution of the transfer curves as a function of the applied negative bias stress time for the HfZnO TFT without a water vapor barrier film and with a multilayer, respectively. In particular, in commercial AMLCD devices, the total stress time of the negative gate bias was more than 500 times that of the positive gate bias. Thus, device degradation due to negative bias temperature instability (NBTI) is a critical issue. The devices were stressed under a −20 V gate source voltage relative to the turn on voltage (V_{ON}) and at a 0.1 V drain source bias at 60°C. The V_{ON} shifted gradually from −3 to −5 V after a total stress time of 3 h for the HfZnO TFT with a multilayer. As in previous reports, the device showed a negative rigid log (I_D)-V_{GS} transfer curve shift and a negligible change in SS value. These results can be explained by simple charge trapping rather than by defect creation.[19–22] In this study, because the devices shown in Figs. 6a and 6b have identical gate dielectrics and HfZnO channels, the charge trappings at or near the channel/dielectric interface during the gate voltage stress were expected to be similar. However, the V_{ON} shifts for the HfZnO TFTs with a multilayer and without a water vapor barrier were −2 and −5 V, respectively. Therefore, the charge trapping model alone cannot entirely account for the observed results. Obviously, the interaction between the channel layer and ambient species can play a critical role in determining the V_{ON} instability. Therefore, the contribution of the interaction effect between the channel and the ambient on V_{ON} instability can be suppressed by the insertion of a proper water vapor barrier film. The negative V_{ON} shift during bias temperature stress was dramatically improved by protecting the HfZnO channel layer with a multilayer water vapor barrier at the lowest WVTR value.

Figure 7 shows the effect of the water vapor barrier films on each device. The variations in ΔV_{ON} shift of the HfZnO and ZnO TFTs as a function of gate voltage stress duration are shown. All devices with barrier films showed parallel V_{ON} changes in the negative direction for negative bias stress with increasing stress time, without any significant changes in the field-effect mobility, SS, or $I_{ON/OFF}$ ratio. The ZnO TFT without a barrier showed a large negative V_{ON} shift of −18 V and a large increase in SS after application of bias stress for 3 h.[18] In contrast, the HfZnO TFT with a multilayer barrier had the smallest V_{ON} shift under a bias stress of −20 V and a duration of 10,000 s. Previous reports suggest that Hf ions may be oxygen binders in ZnO-based TFTs because of their electronegativity of 1.3, resulting in a reduction of the carrier concentration.[23] Hf ions, due to their high oxygen binding energy, may play a key role in improving the stability of TFTs, and the water vapor barrier films with superior barrier properties may affect the stability enhancement. Therefore, the HfZnO TFTs with a barrier layer showed an excellent bias stability improvement. In the case of ZnO TFTs, there was a decrease in the WVTR value of the barrier layer, and the V_{ON} stability of the devices was improved. Therefore, the devices with a lower WVTR value are much more stable against the application of the negative bias stress than the devices with a higher WVTR value. Previous reports showed that the water adsorption/desorption process on the oxide channel involves trap creation/removal in the active layer, indicating that water molecules can act as electron trap centers as well as electron donors.[8] The interaction between the active backchannel and ambient played a critical role in determining the V_{ON} instability. The adsorbed water vapor can release an electron to the conduction band, and the resulting water vapor can be charged, resulting in a positive charge. As a result of charge transfer, an accumulation layer is formed beneath the backchannel surface, leading to a decrease in V_{ON} of the transistor. Also, it is expected that some of the positively-charged water molecules at the backchannel surface will be desorbed upon the application of a positive bias during the transfer characteristic measurements (measurement range of −40 to +40 V). Following this, the re-adsorbed water vapor can release an electron, and the resulting V_{ON} can more dramatically shift in the negative direction. Therefore, water vapor desorption would result in a simultaneous additional V_{ON} shift. The large shift in the V_{ON} and change in the SS value for the ZnO TFT without a barrier was attributed to the electric-field-induced water desorption.[7] Briefly, the water molecules adsorbed onto the back channel surface can act as donors. The enhanced adsorption of positively-charged water molecules induces the delocalized electron

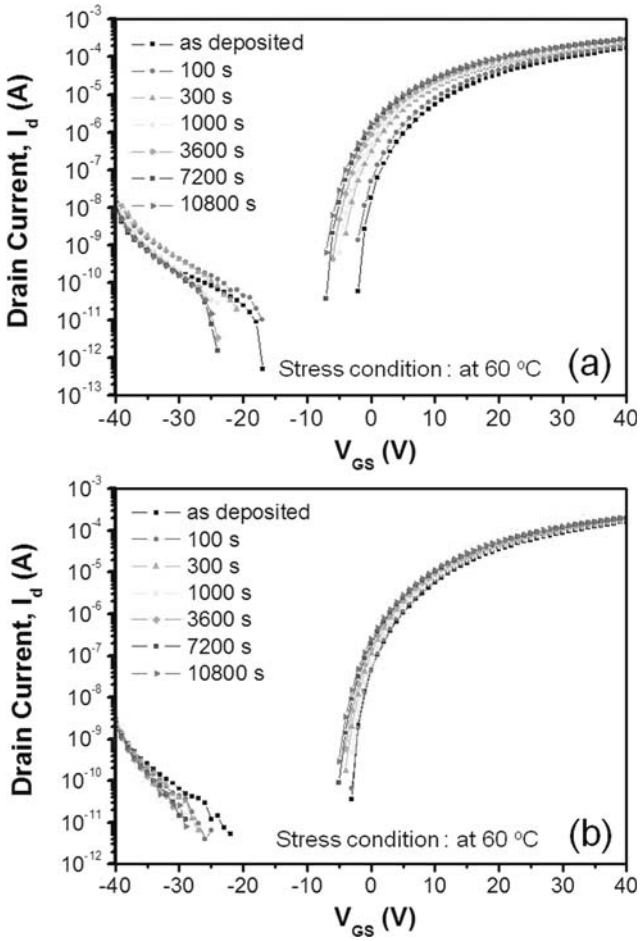

Figure 6. The evolution of transfer curves for the (a) HfZnO TFTs without water vapor barrier films and (b) HfZnO TFTs with a multilayer barrier (40 nm) as a function of applied stress time.

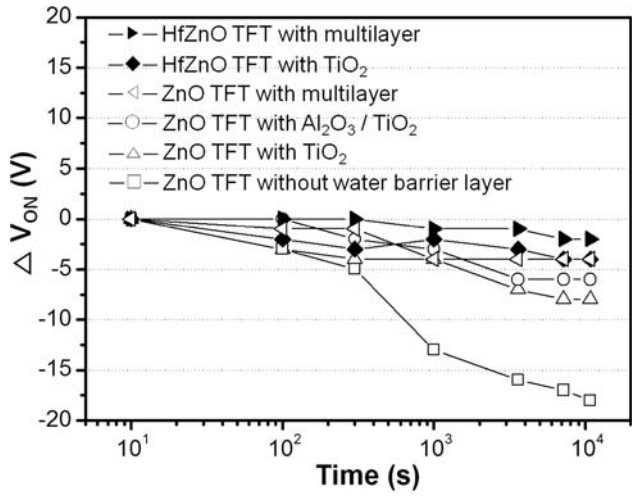

Figure 7. Logarithmic dependence of the turn-on voltage shift (ΔV_{ON}) on the duration of gate bias stress for the ZnO and HfZnO TFTs.

carrier, leading to a negative V_{ON} shift. The water dynamic interaction in the ambient environment can cause a negative V_{ON} shift. We note that the multilayer device showed improved stability compared to those of the other devices. As a result, the origin of the V_{ON} instability was strongly affected by moisture permeation, which was overcome by the use of a moisture-blocking layer such as the multilayer.

Conclusions

In summary, we investigated the changes in device characteristics of ZnO and HfZnO TFTs using PEALD-deposited Al_2O_3 and TiO_2 water vapor barrier films. By adopting a superior barrier, the device properties were improved, and the V_{ON} stability under the negative bias stress was considerably improved in the ZnO and HfZnO TFTs. It was shown that the negative V_{ON} shift during bias stress was due not only to charge trapping, but also to dynamic interactions between the exposed backchannel and the ambient atmosphere. Therefore, a suitable barrier layer with the lowest WVTR is essential to improve the long term reliability of ZnO and HfZnO TFTs.

Acknowledgments

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