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# Inverter made of complementary *p* and *n* channel transistors using a single directly deposited microcrystalline silicon film

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We report a *p* channel thin-film transistor (TFT) made of directly deposited microcrystalline silicon ($\mu c$-Si). By integrating this *p* TFT with its *n* channel counterpart on a single $\mu c$-Si film, we fabricated a complementary metal-silicon oxide-silicon (CMOS) inverter of deposited $\mu c$-Si. The $\mu c$-Si channel material was grown at 320 °C by plasma-enhanced chemical vapor deposition in a process similar to the deposition of hydrogenated amorphous silicon. The highest postdeposition TFT process temperature was 280 °C. The low-temperature *p* channel $\mu c$-Si TFT and the integrated CMOS inverter represent building blocks of a digital circuit technology based on ultralow-temperature silicon. © *1999 American Institute of Physics.* [S0003-6951(99)04634-3]

An ultralow-temperature, large-area silicon technology that could furnish a tool kit of standard devices, including transistors, rectifying diodes, and photodiodes is of great interest for applications in macroelectronics,[1] and in add-on electronics for application-specific integrated circuits (ASICs).[2] The latter application requires that all process temperatures lie below 400 °C, and in general a reduction of the process temperature expands the applicability of macroelectronics. A widely usable ultralow-temperature technology needs *p* channel and *n* channel field-effect transistors, which are the building blocks for complementary digital circuits. The *n* channel thin-film transistors (TFTs) made of directly deposited microcrystalline silicon ($\mu c$-Si) indeed have been reported.[3–7] Microcrystalline films can be obtained at temperatures as low as ~200 °C,[8] but since raising the growth temperature improves transistor performance, the $\mu c$-Si layers for these *n* channel TFTs were grown at higher temperature, e.g., 350 °C.[4] The fabrication of solar cells of $\mu c$-Si[9] suggests that useful hole mobilities can be obtained in $\mu c$-Si. (However, of hydrogenated amorphous silicon (*a*-Si:H), which is an efficient solar cell material,[10] no *p* channel TFTs have been made.) In this letter we report two key steps toward a complete, ultralow-temperature semiconductor technology based on directly deposited $\mu c$-Si. One step is the successful fabrication of *p* channel thin-film transistors deposited at 320 °C and processed at a maximum temperature of 280 °C. The other step is the integration of this *p* channel TFT with an *n* channel TFT to an inverter, which represents a complementary metal-oxide-silicon (CMOS) circuit made of microcrystalline silicon. A third step, an improved *n* channel TFT of $\mu c$-Si, will be reported separately.[11]

We describe the $\mu c$-Si CMOS process with Fig. 1. Both the *p*-type and the *n*-type TFT use one single directly deposited $\mu c$-Si layer as the conducting channel. The $\mu c$-Si channel material was grown by plasma-enhanced chemical vapor deposition (PECVD) in a process similar to the deposition of *a*-Si:H. The undoped channel and the $p^+$ and $n^+$ contact layers were grown by PECVD in two separate (*i* layer/doping) chambers. The $SiO_2$ gate dielectric also was grown by PECVD but in a different system. Growth parameters are listed in Table I. The channel layers of undoped $i\,\mu c$-Si were grown on Corning 7059 glass, by dc excitation of a mixture of $SiH_4$, $SiF_4$ and $H_2$. X-ray diffraction and Raman scattering,[12] and an electron mobility of 4.9 $cm^2/V\,s$ in separately made *n* channel TFTs[6] prove that the films are microcrystalline. Adding $SiF_4$ to the source gas changes the growth chemistry,[13] provides a wider range of structure,[14] and a lower growth temperature[15] than deposition from

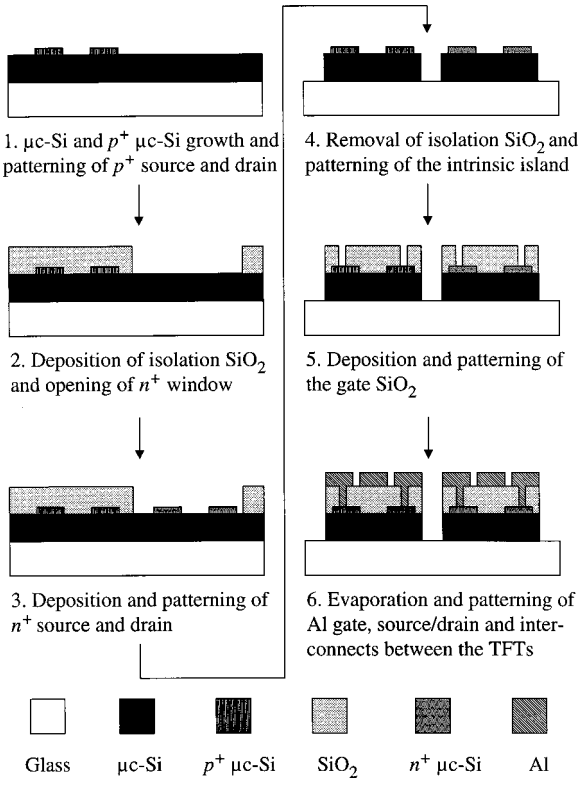


FIG. 1. Schematic process sequence for the microcrystalline silicon CMOS inverter.

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TABLE I. Gas flow rates, deposition temperature, power density, pressure, and thickness of the films grown for the undoped microcrystalline silicon of the TFT channels, the doped source/drain contact layers, and the $SiO_2$ used for isolation.

| Layer | $SiH_4$ (sccm) | $H_2$ (sccm) | $SiF_4$ (sccm) | $PH_3$, $B_2H_6$, or $N_2O$ (sccm) | Temp (°C) | Power density ($mW/cm^2$) | Pressure (mTorr) | Film thickness (nm) |
|---|---|---|---|---|---|---|---|---|
| $\mu c$-Si | 1 | 200 | 20 | 0 | 320 | 160 | 900 | 300 |
| $p^+\mu c$-Si | 2 | 100 | 0 | 50 | 280 | 324 | 900 | 60 |
| $n^+\mu c$-Si | 2 | 100 | 0 | 12 | 280 | 324 | 900 | 60 |
| $SiO_2$ | 35 | 0 | 0 | 160 | 250 | 85 | 400 | 200 |

$H_2$-diluted $SiH_4$ alone.[14] The *n* channel TFTs of $\mu c$-Si grown with $SiF_4$ have exhibited the highest electron mobility reported to date.[3] The growth rate was 0.6 Å/s at a power density of 160 $mW/cm^2$. The dark conductivity of the $i\mu c$-Si is $1\times10^{-7}$ S/cm, and its thermal activation energy is 0.55 eV. The $p^+$ and $n^+$ source/drain contact layers were grown from $SiH_4$, $H_2$, and $B_2H_6$ or $PH_3$ by rf excitation at 13.56 MHz. Their dark conductivities are 0.01 S/cm ($p^+\mu c$-Si) and 20 S/cm ($n^+\mu c$-Si).

The TFTs were made in the top-gate configuration shown in Fig. 1. The CMOS inverter is made of a *p* channel TFT and an *n* channel TFT of identical structure. A six-level mask process with specially designed masks was used in the inverter fabrication. First, 300 nm of $i\mu c$-Si and 60 nm of $p^+\mu c$-Si layer were grown on the substrate without breaking vacuum. Next, we patterned the $p^+\mu c$-Si source and drain for the *p* channel TFT using reactive ion etching (RIE) with 10% $O_2$ and 90% $CCl_2F_2$. Deposition of 200 nm layer of isolation $SiO_2$ followed. Then we opened a window in the $SiO_2$ using buffered oxide etch (BOE) to deposit a 60 nm $n^+\mu c$-Si layer. After RIE patterning of the $n^+\mu c$-Si source and drain for the *n* channel TFT, we removed the $SiO_2$ layer with BOE, and followed by the definition of the $i\mu c$-Si island using RIE. The channel $\mu c$-Si now exposed was oxidized for 10 min in 1:3 $H_2O_2$:$H_2SO_4$, then dipped for 10 s in BOE, rinsed in de-ionized water, blow dried in nitrogen, and immediately introduced into the system for gate insulator deposition. After we deposited 200 nm $SiO_2$ as gate insulator, we patterned the $SiO_2$ gate and opened contact holes to the *n* and *p* channel TFT source and drain using BOE. Then we thermally evaporated Al, and patterned the Al using a wet etch to form the gate, source, and drain electrodes of the *n* and *p* channel TFTs, as well as the metal interconnects between the two gates, and the two drains of the *p* TFT and the *n* TFT. The pull-up *p* channel TFT and pull-down *n* channel TFT both have 180-$\mu$m-wide and 45-$\mu$m-long channels. These large dimensions result from our use of a laser printer for mask making.

Figure 2 shows the transfer characteristics of the *p* channel and *n* channel TFTs of the inverter. We define the ON current $I_{ON}$ as the drain current $I_d$ at a gate voltage $V_{gs}$ of ($-$ or $+$) 25 V, and the OFF current $I_{OFF}$ as the lowest drain current, both at a drain voltage of $V_{ds}$ of ($-$ or $+$) 10 V. Figure 2(a) shows a *p* channel TFT ON/OFF current ratio of $>10^3$, a threshold voltage $V_{TH}$ of $-16$ V, and a subthreshold slope $S\equiv d(V_{gs})/d(\log_{10} I_d)$ of 2.7 V/decade. The hole field-effect mobilities $\mu_h$ of the *p* channel TFT extracted from the linear and saturated regimes are 0.023 and 0.031 $cm^2/V$ s, respectively. The ON/OFF current ratio of the *n* channel TFT of Fig. 2(b) is $\sim10^4$, its $V_{TH}$ is 3 V, and $S=4.2$ V/decade. The electron field-effect mobilities $\mu_n$ of the *n* channel TFT extracted from the linear and saturated regimes are 0.72 and 1.0 $cm^2/V$ s, respectively. These $\mu_n$ values lie substantially below those obtained in a separately fabricated $\mu c$-Si *n* channel TFT.[7,11] We ascribe the reduction in field-effect mobility to the unoptimized process sequence for CMOS inverter fabrication, which also is reflected in the values for $V_{TH}$ and *S*.

The voltage transfer characteristic of the CMOS inverter made of the pull-up *p* channel TFT and the pull-down *n* channel TFT is shown in Fig. 3 for supply voltages of $V_{DD}=30$ V and $V_{SS}=-20$ V. The inverter exhibits a nearly full rail-to-rail swing, and an abrupt and well-defined voltage transfer characteristic with a gain of 7.2. The output HIGH is

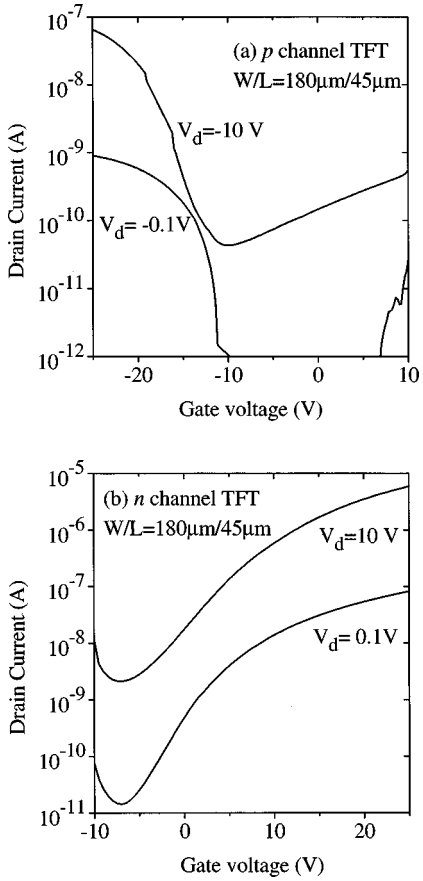


FIG. 2. Transfer characteristics of the (a) *p* channel $\mu c$-Si TFT, and (b) *n* channel $\mu c$-Si TFT of the CMOS inverter.

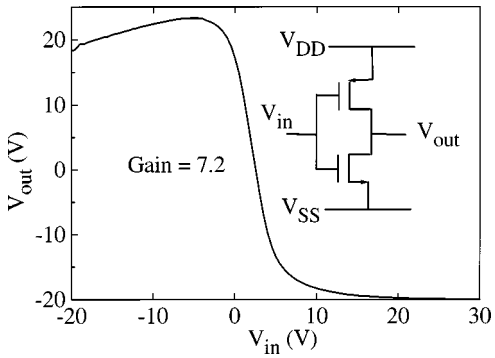


FIG. 3. Voltage transfer characteristics of a CMOS inverter made of $\mu c$-Si. The $p$ channel and $n$ channel TFTs have identical channel dimensions. $V_{DD}=30$ V and $V_{SS}=-20$ V.

about 90% of the full voltage range and the output LOW is at the same voltage as $V_{SS}$.

Thus we have introduced a digital device and circuit technology based on directly deposited microcrystalline thin-film silicon. Its maximum process temperature of 320 °C is ideally suited to glass substrates, and of course is suitable to more refractory substrates such as steel.[16] It also is suited as a complementary metal-oxide-silicon (CMOS) technology for add-on circuits to application-specific integrated circuits (ASICs). The $\mu c$-Si TFTs need improvements in two directions. One is higher field-effect mobilities, to enable higher ON current for high speed and high fan outs. The other is a further reduction in process temperature, to take advantage of a wider variety of substrate materials. We are confident that progress can be made in both directions.

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