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Evidence of carrier number fluctuation as origin of 1/*f* noise in polycrystalline silicon thin film transistors

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A systematic study of the noise performances of polycrystalline silicon thin film transistors is presented. The drain current spectral density of these devices shows an evident 1/ *f* behavior and scales, when operating in the linear regime, with the square of the mean value of the drain current. The origin of the noise can be ascribed to carrier number fluctuations related to the dynamic trapping and detrapping of the oxide traps. © *1995 American Institute of Physics.*

Polycrystalline silicon (polysilicon) thin-film transistors (TFTs) are currently investigated for application in static random access memories (SRAMs) and for addressing and driving in active matrix liquid crystal displays (AMLCD). In these applications there is a common demand for high performances, high stability, and low noise devices. A number of technological efforts have been devoted in order to increase the field effect mobility, now exceeding 400 cm^2/V s in polysilicon TFTs recrystallized by excimer laser.[1,2] The assessment of the long term reliability of the electrical stability has been the subject of a number of recent investigations,[3,4] while the noise characterization of such devices has received little attention and only preliminary data exist in the literature.[5–7] On the other hand the noise is the main limitation to the use of polysilicon TFTs in large area image sensors. In fact, the performances of such applications would greatly improve using a local amplification of the signal, but the equivalent noise charge has to be lower than about 1000 electrons.[8,9]

In the present letter we have studied the noise performances of polysilicon TFTs fabricated with a four mask sequence. The active layer (100 nm thick) was deposited amorphous by pyrolysis of Si_2H_6 in an UHVCVD reactor[10] and subsequently furnace crystallized at 580 °C. After definition and reactive ion etching (RIE) of the active polysilicon islands, the gate SiO_2 was deposited to a thickness of 120 nm by distributed electron cyclotron resonance (DECR) plasma enhanced CVD (PECVD).[10] The gate electrode was defined by RIE of an *in situ* doped amorphous silicon layer deposited by LPCVD at 560 °C. The self-aligned source and drain contacts were formed by a phosphorous implant, which was activated by a furnace anneal at 580 °C. This thermal treatment also converted the amorphous gate material to low resistivity degenerated polycrystalline silicon. The contacts were defined by lift-off of an evaporated aluminum film and the devices were then annealed at 450 °C under flowing forming gas (10% H_2 in N_2). Finally, the samples were covered with a SiO_2 passivation layer. Field effect mobility in these devices, without posthydrogenation treatment and with a maximum processing temperature of 580 °C, is around 50 cm^2/V s.

The noise measurements were performed biasing the device with constant source-drain voltage V_{ds}, and measuring the fluctuations of the drain current I_d, through a low noise current amplifier (PAR 181) connected to a spectrum analyzer (HP 3561A). The noise contribution of the source/drain contact resistance was found negligible. Polysilicon TFTs with channel width 40 μm (W) and channel lengths; 5, 10, 20, 30, and 40 μm (L) were studied. Figure 1 shows the transfer characteristics for different channel lengths, where an high on/off ratio (more than 5 orders of magnitude) is observed. Figure 2 shows a typical drain current spectral density S_I, measured in a device operating in the linear regime: $V_{ds}=2$ V and gate voltage, $V_g=14$ V. As can be noted the noise shows a $1/f$ behavior, commonly observed in crystalline Si (*c*-Si) MOSFETs.[11–14] When the device is biased in the linear regime with a constant gate voltage the drain current spectral density increases as V_{ds}^2, or, equivalently, as the square of the mean value of I_d, in agreement with the $1/f$ theory,[11] as confirmed by Fig. 3, where S_I/I_d^2 is plotted versus the mean value of I_d.

The origin of the low frequency noise in MOSFETs has been related to either carrier number fluctuation or carrier mobility fluctuation. In the carrier number fluctuation model, based on the McWorther theory,[12,15,16] the fluctuations of the

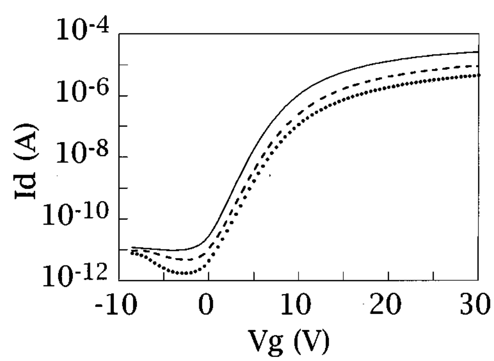

FIG. 1. Transfer characteristics measured at $V_{ds}=0.2$ V for different channel lengths: continuous line $L=5$ μm dashed line $L=20$ μm, and dotted line $L=40$ μm.

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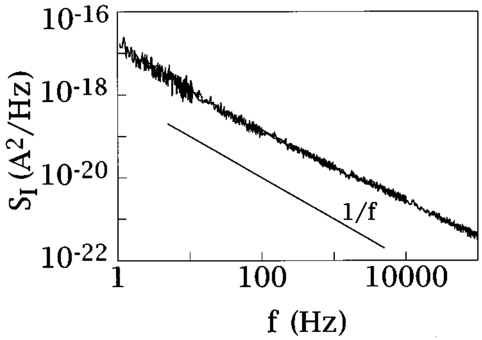

FIG. 2. Drain current spectral density for a TFT with channel length $L = 10$ μm $V_{ds}=2$ V and $V_g=14$ V.

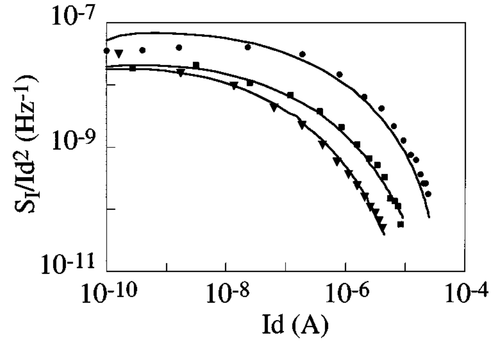

FIG. 4. Normalized drain current spectral density, S_I/I_d^2, at 20 Hz vs the mean value of the drain current I_d, for TFTs with channel length $L=5$ μm (●), $L=20$ μm (■), and 40 μm (△). Continuous lines are the best fit to Eq. (1).

drain current are induced by fluctuations of the interfacial oxide charge due to the dynamic trapping and detrapping of free carriers into slow oxide traps. In other words, due to the interface charge fluctuations, the flatband voltage V_{fb} fluctuates and, therefore, also the charge induced in the semiconductor fluctuates. In the mobility fluctuation model,[17] the fluctuations of the drain current arise from the fluctuations of the carrier mobility possibly through a fluctuation of the scattering cross section. This results in a $1/f$ noise whose intensity is inversely proportional to the total number of carriers in the system. In order to discriminate between the two mechanisms the normalized drain current spectral density can be analyzed. In fact, according to the carrier number fluctuations, at low values of the drain current, S_I/I_d^2 shows a plateau before decreasing as I_d^{-2} as the TFT is turned on.[16] Vice versa, in case of mobility fluctuations, S_I/I_d^2 is expected to be inversely proportional to I_d.[16]

Figure 4 shows S_I/I_d^2 versus I_d for different channel lengths. The measurements were performed biasing the TFTs in the linear regime ($V_{ds}=0.2$ V) and changing V_g. From the shape of the S_I/I_d^2 the noise the polysilicon TFTs can be ascribed to carrier number fluctuations. In order to confirm this point we have fitted the experimental data with the theoretical expression for the S_I/I_d^2 in the case of carrier number fluctuations:[16]

$$S_I/I_d^2=(1+\alpha\mu_{eff}I_d/g_m)^2(g_m/I_d)^2S_{Vfb}, \tag{1}$$

where α is a constant, μ_{eff} is the effective carrier mobility in the channel, C_{ox} is the gate oxide capacitance per unit area, g_m is the device transconductance (evaluated from the data shown in Fig. 1), and S_{Vfb} is the flatband voltage spectral density. The continuous lines shown in Fig. 4 represent the best fit of the data with Eq. (1) and, as can be easily recognized, a very good agreement is observed. The mean value of the fitting parameter α was found 1.5 10^4 V s/C, close to that reported for *c*-Si MOSFETs [10^4 V s/C (Ref. 16)], while the value of the fitting parameter S_{Vfb} was around 1.2 10^{-8} V^2/Hz. The noise in polysilicon TFTs appears much higher than in *c*-Si MOSFETs[7,13,14] and such an higher noise level could be related to fluctuations of the barrier heights present at the polysilicon grain boundaries[7] or to an higher density of traps in the oxide close to the interface. Assuming a predominance of the latter mechanism and according to the conventional tunneling mechanism,[12,15] the oxide trap state density N_t can be evaluated from the following expression:

$$S_{Vfb}=(q^2KT\lambda N_t)/(WLC_{ox}^2f), \tag{2}$$

where λ is the tunnel attenuation distance [around 0.1 nm (Ref. 13)], q is the unit charge, and KT is the thermal energy. From Eq. (2) we obtain, by using the fitted values for S_{Vfb}, a N_t value around 10^{20} states/eV cm^3, which is about three orders of magnitude higher than the N_t value generally found for CMOS technology.[13,14]

In conclusion, we have, for the first time, systematically studied the noise performances in polysilicon TFTs. These devices are characterized by the presence of a strong $1/f$ noise. From the analysis of the drain current spectral density we have identified the origin of the low frequency noise in the carrier number fluctuations. The noise level appears to be much higher than in *c*-Si MOSFETs. This increased noise level could be related to several effects including the presence of localized states at the polysilicon grain boundaries[7] or an higher oxide trap density. In the latter case we have estimated an oxide trap density around 10^{20} states/eV cm^3, which is three order of magnitude higher than typical values for *c*-Si MOSFETs.[13,14] Although our DECR PECVD oxide, deposited at low temperature (<100 °C), contains an higher density of traps if compared to thermal oxide, the estimated value of N_t is not compatible with the quality of our oxide.[18]

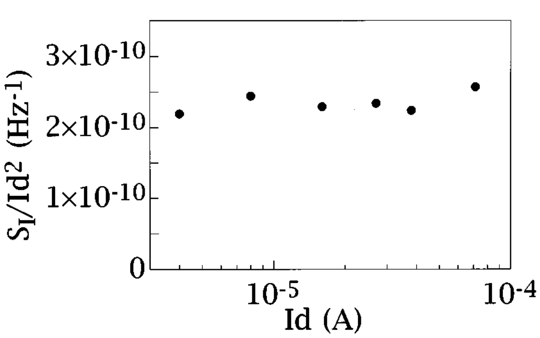

FIG. 3. Normalized drain current spectral density, S_I/I_d^2, at 20 Hz vs the mean value of the drain current I_d, for a TFT operating in the linear regime with $L=10$ μm and $V_g=14$ V.

Therefore, further investigations are needed to clarify the microscopic mechanisms causing the excess noise observed in polysilicon TFTs.

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