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High quality thin gate oxide prepared by annealing low-pressure chemical vapor deposited SiO_2 in N_2O

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In this letter, the electrical properties of thin low-pressure chemical vapor deposited (LPCVD) SiO_2 annealed in N_2O ambient have been studied and compared with thermal oxide of identical thickness. It is shown that N_2O-annealed CVD oxide exhibits less interface state generation and less flatband voltage shift under constant current stress than thermal oxide. It also has excellent uniformity and comparable breakdown characteristics. An oxynitride film formation at the Si/SiO_2 interface by annealing in N_2O is speculated to be the cause of these improvements.

The as-deposited chemical vapor deposited (CVD) oxide generally has inferior electrical characteristics for metal-oxide-semiconductor (MOS) gate dielectric applications due to a large number of silicon and oxygen dangling bonds at the Si/SiO_2 interface. This is because the low CVD deposition temperature does not allow the deposited species to have enough energy or mobility to move around to the dangling bond sites.[1] As a result, low-temperature CVD oxide films are used mostly in noncritical applications with thickness of 1500 Å or greater. However, CVD oxide has a potential advantage that it is, in principle, independent of defects originating from the Si substrate since the film is deposited on, rather than grown from, the substrate. It has been reported that postdeposition high-temperature annealing in O_2 and N_2 (or Ar) can improve low-pressure chemical vapor deposited (LPCVD) oxide characteristics which are close to or better than those of thermal oxide.[1-3] It was speculated that a thin thermal oxide formation at the Si/SiO_2 interface would improve these properties. It also has been reported that the oxidation of Si in pure N_2O ambient produces better quality oxide (oxynitride) than thermal oxide due to nitrogen incorporation at the Si/SiO_2 interface.[4,5] One would expect that similar advantages of forming an oxynitride layer at Si/SiO_2 interface can be obtained by annealing the CVD oxide in pure N_2O ambient.

This letter reports the first study of high quality thin (90 Å) gate oxide obtained by annealing low-temperature (450 °C) LPCVD oxide in pure N_2O ambient. This CVD oxide shows less interface state generation (ΔD_{it}) and less flatband voltage shift (ΔV_{FB}) under constant current stress than thermal oxide. It has comparable dielectric breakdown characteristics and excellent thickness uniformity.

Polycrystalline silicon gate MOS capacitors were fabricated by an etch-back process on 3–5 Ω cm, (100) p-type 4 in. Si wafers. CVD oxide and control thermal oxide samples were fabricated for comparison. A 5000 Å field oxide was grown in steam at 950 °C. Active areas were defined by lithography and etching. Standard RCA cleaning was done on both wafers prior to the gate oxidation. A CVD SiO_2 film was deposited at 450 °C by LPCVD in a hot-wall multiwafer reactor with silane and oxygen and annealed in pure N_2O ambient at 950 °C for 10 min, followed by annealing in N_2 at 950 °C for 5 min with a final thickness of 90 Å. The control thermal oxide of identical thickness was grown by atmospheric pressure thermal oxidation in dry O_2 at 950 °C followed by 15 min annealing in N_2 at the same temperature. Standard polycrystalline silicon gate technology was used for the completion of the MOS capacitor fabrication. High-frequency and quasistatic capacitance-voltage (C-V) measurements before and after constant current stress were used to characterize the hot-electron resistance of these gate dielectrics. Breakdown histograms were obtained through voltage ramping method on 40 large area (1×10^{-2} cm^2) capacitors by defining the breakdown field (E_{BD}) as an applied field at which the current exceeded -1 μA.

Figure 1 shows an Auger electron spectroscopy (AES) depth profile of nitrogen in CVD oxide annealed in N_2O at 950 °C for 10 min. This profile shows a nitrogen peak at the Si/SiO_2 interface with a small amount of nitrogen in the bulk. The Si/SiO_2 interface was defined as the depth at which oxygen concentration is equal to the average value of substrate and bulk oxide. This overall profile is similar to that of oxynitride film grown by thermal oxidation of Si in N_2O ambient, although the nitrogen concentration in N_2O-annealed CVD oxide is lower than that in oxynitride.[4,5] The thickness increase by annealing in N_2O at 950 °C for 10 min was about 25 Å by ellipsometric measurement and the thickness uniformity of the as-deposited CVD oxide was significantly improved by the annealing in N_2O (within ± 1.5% deviation). A fixed refractive index (1.46) was used for ellipsometry because the nitrogen concentration in the bulk oxide is small.

Breakdown histograms of 40 capacitors with N_2O-annealed CVD oxide and control thermal oxide are shown in Fig. 2. As can be seen, breakdown field distributions of N_2O-annealed CVD oxide and control thermal oxide are comparable. Earlier reports regarding reduced low-field breakdown of CVD oxide due to oxide weak spots as compared to thermal oxide[6] cannot be verified in our work. This is because it is difficult to distinguish breakdown induced by oxide weak spots from intrinsic breakdown for thin oxide ($\leqslant$150 Å).[7] The other reason may be that the

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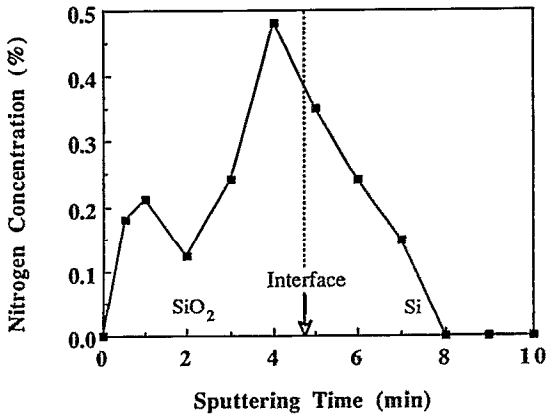

FIG. 1. AES depth profile of nitrogen for CVD oxide annealed in N_2O at 950 °C for 10 min.

low-field breakdown of the control thermal oxide may have been eliminated by high-temperature postoxidation annealing.[8]

Figure 3 shows quasistatic C-V curves of MOS capacitors with control thermal oxide and N_2O-annealed CVD oxide, before and after constant current stress (-10 mA/cm^2). Interface state densities (D_{it}) were also obtained from high-frequency and quasistatic C-V curves. The N_2O-annealed CVD oxide shows smaller distortions in quasistatic C-V curves, i.e., less ΔD_{it} (5.6×10^{11} cm^{-2} eV^{-1} and 9.0×10^{11} cm^{-2} eV^{-1} at midgap for N_2O-annealed CVD oxide and control thermal oxide, respectively, after 0.1 C/cm^2 stress) than control thermal oxide. The initial midgap interface state density (D_{itm}) of the N_2O-annealed CVD oxide was 5×10^{10} cm^{-2} eV^{-1}, very close to that of the control thermal oxide (4×10^{10} cm^{-2} eV^{-1}). The annealing of CVD oxide in N_2O causes densification, mobilizing the deposited species to dangling bond sites, and oxynitride formation at the Si/SiO_2 interface. As reported earlier for nitrided thermal oxides, nitrogen incorporation at the Si/SiO_2 interface leads to interfacial strain relaxation, resulting in less ΔD_{it} which comes from breaking the Si—O strained bonds near the interface by hot electrons.[9]

The flatband voltage shift (ΔV_{FB}) obtained by high-frequency C-V curves is much smaller in the CVD oxide

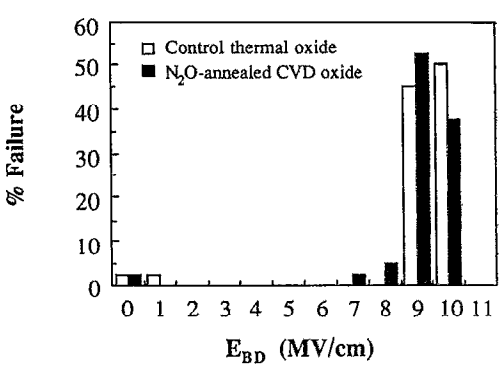

FIG. 2. Breakdown histograms of 40 capacitors with control thermal oxide and N_2O-annealed CVD oxide (capacitor area $= 1\times10^{-2}$ cm^2).

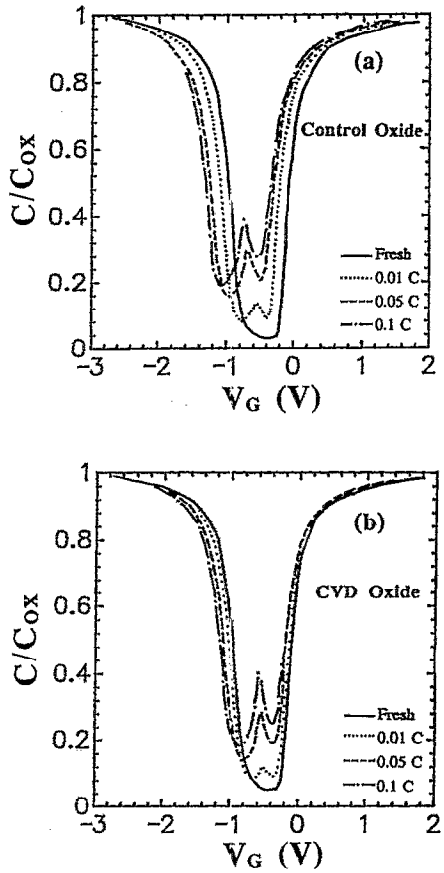

FIG. 3. Quasistatic C-V curves of capacitors with (a) control thermal oxide and (b) N_2O-annealed CVD oxide, before and after constant current stress (-10 mA/cm^2).

than in the control oxide, as can be seen in Fig. 4. In both cases ΔV_{FB}'s are negative which implies a net positive charge trapping at the Si/SiO_2 interface. Less positive charge trapping is due to the fact that the formation of Si—N bonds at the Si/SiO_xN_y interface replaces strained Si—O bonds, reducing the number of trivalent Si defects generated during electrical stress.[10] So, by annealing CVD oxide in N_2O ambient it is possible to take advantage of the oxynitride formation at Si/SiO_2 interface which was re-

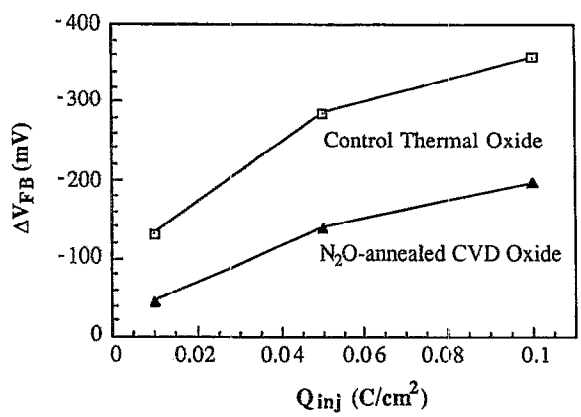

FIG. 4. Flatband voltage shift under constant current stress (-10 mA/cm^2).

ported to have less ΔD_{it} and ΔV_{FB} under electrical stress.[4,5]

In conclusion, high quality thin N_2O-annealed CVD oxide has been fabricated and compared with thermal oxide. The results show that N_2O-annealed CVD oxide has less ΔD_{it} and ΔV_{FB} than control thermal oxide under constant current stress. N_2O-annealed CVD oxide also shows excellent uniformity with comparable breakdown characteristics. These improvements are speculated to be due to an oxynitride film formation at the Si/SiO_2 interface caused by postdeposition annealing in pure N_2O ambient.

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