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Tantalum Oxide Thin Films for Dielectric Applications by Low-Pressure Chemical Vapor Deposition

Physical and Electrical Properties

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ABSTRACT

High quality Ta_2O_5 films suitable for 64 Mb DRAM use have been deposited by low-pressure chemical vapor deposition (LPCVD) from $Ta(OC_2H_5)_5$ (tantalum pentaethoxide) and oxygen. The films have been deposited on silicon, polysilicon, and SiO_2. Thickness reproducibility, across-the-wafer uniformity, and conformality and step-coverage all are excellent. As-deposited films are amorphous with smooth surfaces. Annealed films are polycrystalline, and their surfaces are characterized by 2 nm high, 1 μm diam nucleation centers surrounded by circular crystallization fronts. The films must be annealed to get acceptable leakage currents. Leakage currents for annealed 10 to 40 nm Ta_2O_5 films are independent of film thickness and are $\leq 10^{-9}$ A/cm^2 at a gate voltage of 1.5 V. Effective dielectric constants decrease with Ta_2O_5 film thickness. The smallest observed equivalent SiO_2 thickness, $t_{ox,eff}$, is 3.5 nm for 7.5 nm Ta_2O_5/Si. The minimum practical $t_{ox,eff}$ for the Ta_2O_5/Si system is approximately 3 nm. These electrical results are explained by the presence of a thin SiO_2 layer at the Ta_2O_5/Si interface. The SiO_2 layer dominates the electrical behavior of thin annealed Ta_2O_5 films on Si. Effects of the surface structure and minimum $t_{ox,eff}$ on device integration are discussed.

The increasing densities of metal oxide semiconductor-dynamic random access memories (MOS-DRAMs) and of other integrated circuits have reduced the cell area available for capacitors with no corresponding decrease in their capacitance[1,2] and has put ever-increasing demands on the design of these capacitors and on the performance of their dielectrics. Two approaches are being used to solve this problem. The first is to develop three-dimensional capacitor structures such as stacked[3] or trench[4] structures, thus increasing the capacitor storage area without increasing the cell area. The second is to use higher dielectric constant materials to replace the SiO_2-based (ON or ONO) dielectrics presently used for capacitors, because shrinking cell areas have forced the reduction of SiO_2-based dielectric thicknesses to near their minimum useful values. They cannot be used below about 4 nm thickness because of increased leakage currents due to tunneling.[5] Ta_2O_5 is an attractive candidate for replacing SiO_2-based dielectrics because of its higher dielectric constant, low leakage currents, and reasonable breakdown voltages.[6-17]

This paper discusses the development of CVD Ta_2O_5 for such dielectric applications. Included are descriptions of the Ta_2O_5 CVD process, annealing conditions, and the physical and electrical properties of the films when deposited on silicon, polysilicon, and CVD SiO_2.

Experimental

The Ta_2O_5 was deposited in a Watkins-Johnson SELECT™ 7000P single-wafer reactor by LPCVD. A schematic diagram of this reactor is shown in Fig. 1. The reactants used are oxygen and tantalum pentaethoxide, $Ta(OC_2H_5)_5$. The tantalum pentaethoxide is vaporized in a custom-designed, labyrinth-type bubbler and is transported to the reaction chamber with N_2 carrier gas. There is a run-vent valve between the bubbler and the reaction chamber. This valve provides the precise control of $Ta(OC_2H_5)_5$ needed to yield acceptable run-to-run reproducibility in film properties. The reactants are injected into the reaction chamber with especially designed gas distribution manifold. It consists of several concentric circular gas channels, each with its own set of adjustable nozzles. The O_2 and $Ta(OC_2H_5)_5$ are not premixed but rather alternate between adjacent channels. This alternation prevents prereaction, ensures adequate distribution in the chamber, and the adjustable nozzles allow for easy tuning of reactant delivery to optimize the uniformity of the films. Although the reactor is a cold-wall reactor, the Ta precursor delivery lines and the gas distribution manifold must be heated above the temperature of the bubbler to prevent condensation of the $Ta(OC_2H_5)_5$.

During deposition, the wafer is supported on a quartz platform in near-vertical position. This position reduces the probability of particle deposition on the wafer.[18] The platform is heated by a concentric 3-zone heater. The temperatures of the three zones are independently controlled and are set to give uniform wafer temperature during deposition, a necessity for achieving optimum Ta_2O_5 uniformity.

Typical deposition conditions are shown in Table I. These conditions were chosen to optimize both the physical and electrical properties of the Ta_2O_5.

In some cases, we deposited a thin film of SiO_2 prior to the Ta_2O_5 deposition. The SiO_2 was deposited in a separate reactor of similar configuration, employing hexamethyldisiloxane (HMDSo, $Si_2(OCH_3)_6$) and ozonated oxygen as reactants. We used an organic precursor instead of silane due to the superior conformality obtained by these meth-

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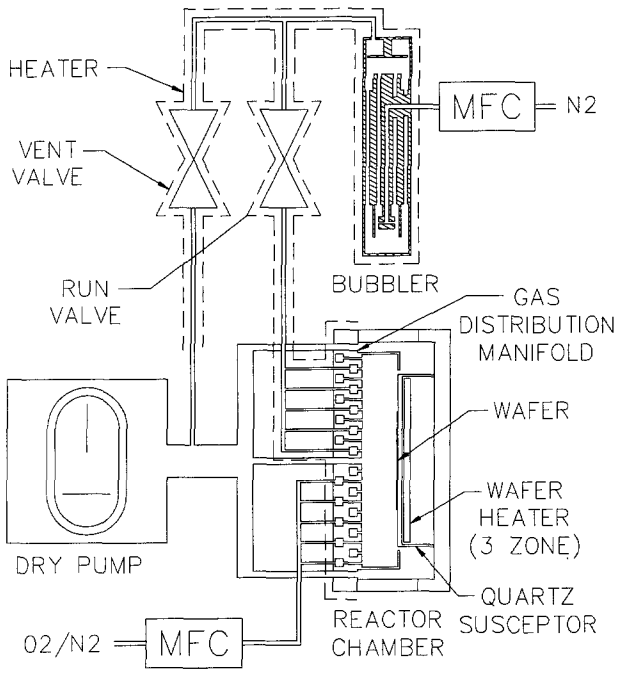

Fig. 1. Schematic Diagram of SELECT™ LPCVD Reactor.

ods;[19] we felt that a conformal thin film would be relatively insensitive to particulate contamination. The thickness of the films was monitored by ellipsometry, referenced to a wafer freshly stripped in HF and presumed to represent a clean surface. Deposition conditions are given in Table II.

The substrates used for the Ta_2O_5 depositions were either <100> p-type Si, <100> n^+ Si, or n^+ polysilicon. All were 150 mm diameter. They received three different surface treatments; as received for p-type and n^+ prime Si wafers, HF dip before CVD, and HF dip plus 3 nm of CVD SiO_2 from HMDSo and O_3. Those wafers that got Ta_2O_5 CVD as-received were first characterized by total x-ray fluorescence (TXRF) to ensure surface cleanliness. We observed no significant differences in the physical or electrical characteristics of Ta_2O_5 deposited on as-received *vs.* HF-dipped substrates.

After deposition, most of the films were annealed to stabilize their physical and electrical properties and to reduce their leakage currents.[10,13] All the anneals were done in dry O_2 in a horizontal tube furnace at 800°C for 30 min. These annealing conditions were chosen to optimize the desired physical and electrical properties of the films. Lower anneal temperatures and shorter anneal times gave higher leakage currents, while higher anneal temperatures and longer times resulted in lower dielectric constants. We chose to anneal in dry O_2 because films annealed in dry O_2 exhibited lower leakage currents than films annealed in dry N_2 for equivalent temperatures and times. Also, we chose dry O_2 to ensure that the Ta_2O_5 would remain fully oxidized during the could be reduced during the anneal. The Ta_2O_5 could be reduced during the anneal if there were

Table I. Typical Ta_2O_5 CVD deposition conditions.

Deposition parameter	Typical value
O_2 flow	100 sccm
Bubbler N_2 flow	100 sccm
$O_2/Ta(OC_2H_5)_5$ ratio	60/1
$Ta(OC_2H_5)_5$ bubbler temperature	110°C
Delivery line temperature	135°C
Manifold temperature	135°C
Wafer deposition temperature	450 to 470°C
Chamber pressure	600 mTorr
Deposition rate	7.5 nm/min
Thickness uniformity	≤1.2% one sigma
$C_{min} - C_{max}$ (10 nm films)	0.2 fF/μm² (1.1%)
Thickness reproducibility	≤1.0% one sigma
Particles added (10 nm)	≤0.2/cm² larger than 0.08 μm²

Table II. Typical SiO_2 deposition conditions from HMDSo.

Deposition parameter	Typical value
Temperature	380°C
Pressure	2 Torr
Oxygen + ozone flow	2 slpm
Ozone concentration	125 g/m³
HMDSo flow	125 sccm
Deposition time	30 s
Film thickness	3 nm

a solid-phase reaction at the Ta_2O_5/Si interface which forms SiO_2 and suboxides of tantalum. The presence of O_2 during the anneal would reoxidize the reduced tantalum, thus preserving the stoichiometry of the film.

The films' physical properties have been characterized by Auger electron spectroscopy (AES), scanning electron microscopy (SEM), atomic force microscopy (AFM), transmission electron diffraction (TED), and plan and cross-sectionaltransmission electron microscopy (TEM). Their thicknesses and uniformities have been measured by a Prometrix SpectraMap™ and by ellipsometer. Their particle counts have been measured by a Tencor Model 5500. Their electrical properties have been assessed by 1 MHz capacitance-voltage (C-V) and quasi-static current-voltage (I-V) measurements. For these measurements, MOS capacitors were made using 0.5 and 1 mm Hg contacts. We have determined that there is no significant difference in the electrical results between Hg and sputtered W contacts.

Results and Discussion

Physical Data.—Transmission electron diffraction measurements indicate the films are amorphous as-deposited and polycrystalline after annealing. Auger electron spectroscopy measurements establish that the Ta_2O_5 is stoichiometric as-deposited with O:Ta ratio of 2.5 ± 0.05:1. There was no detectable change in the stoichiometry of the films after the O_2 anneal discussed above. There are no detectable impurities in the Ta_2O_5. This result indicates carbon incorporation levels about 0.1 atomic percent (a/o) or less, the resolution limit of AES for carbon.

As shown in Table I, deposition rates are 7.5 nm/min. This yields a deposition time of about 1 min for the 7 to 10 nm needed for 64 Mbytes and larger DRAM capacitors.[12,15,20] We have observed no incubation time or any surface sensitivity with the Ta_2O_5 depositions: the deposition rate is the same whether the Ta_2O_5 is deposited on Si prime wafers, HF-stripped prime wafers, polysilicon, or SiO_2. Run-to-run thickness reproducibility for as-deposited films is excellent, with one sigma ≤1.0% for several consecutive 10 nm runs. This figure is at or below the limit of resolution of the ellipsometer used to make the measurements.

Prometrix™ 49-point thickness measurements on 40 nm films show excellent uniformity. The typical standard deviation is ≤1.2% for the deposition conditions given in Table I. 10 nm films measured by ellipsometer show similar uniformities. To obtain such uniformities, it is necessary to adjust the nozzles in the gas distribution manifold to give reasonably uniform reactant delivery to the substrate. Once such uniform gas flow has been established, the principal factor affecting thickness uniformity is the temperature uniformity of the substrate. An across-the-substrate temperature variation no greater than ±1.5°C is needed to obtain the thickness uniformity stated above.

Another measure of the uniformity of a dielectric film is the range of maximum capacitance C_{max} to minimum capacitance C_{min} which one would expect for MOS capacitors across a typical device wafer. We have made such measurements on several 10 nm annealed Ta_2O_5 films with 0.5 mm diam MOS capacitors. For the typical film, C_{max} is 8.8 fF/μm² and C_{min} is 8.6 fF/μm². This gives a $C_{max} - C_{min}$ of 0.2 fF/μm², or about 1.1%. These results confirm the excellent uniformity of the Ta_2O_5 film.

Conformality and step-coverage are excellent. Figure 2 is a cross-sectional SEM of 100 nm as-deposited Ta_2O_5 in a

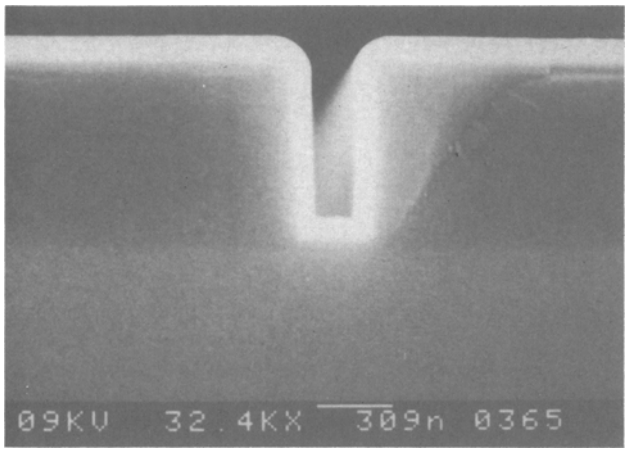

Fig. 2. Cross-sectional SEM of 100 nm Ta_2O_5 in 0.35 μm wide × 0.70 μm deep polysilicon trench.

0.35 μm wide × 0.70 μm deep polysilicon trench. Conformality is >90%, and coverage is good at the bottom corners of the trench.

Figure 3 is a high resolution cross-sectional TEM of 10 nm annealed Ta_2O_5 on n^+ polysilicon with 3 nm of CVD SiO_2 at the Ta_2O_5/polysilicon interface. The SiO_2 was deposited by LPCVD in a SELECT™ S7000P reactor from HMDSo and O_3. Its function was to provide a reproducible high quality SiO_2 layer between the Ta_2O_5 and the polysilicon. Four layers are visible, (*i*) the polysilicon, (*ii*) approximately 3 nm of SiO_2 between the polysilicon and the Ta_2O_5, (*iii*) 10 nm of Ta_2O_5, and (*iv*) an epoxy overlay used to facilitate the TEM sample preparation. The SiO_2 layer is amorphous, while atomic planes are faintly visible in the Ta_2O_5 layer and clearly visible in the polysilicon. This visibility indicates that the Ta_2O_5 was crystallized by the annealing process. The interfaces are planar with no sign of encroachment of the Ta_2O_5 upon the SiO_2 during CVD or anneal.

Figure 4 is a high contrast cross-sectional TEM of an annealed 10 nm Ta_2O_5 film deposited in a 0.35 μm wide × 1.0 μm deep polysilicon trench. The image was taken at the bottom corner of the trench. The film is highly conformal with no cracks or voids. The Ta_2O_5 at the bottom of the

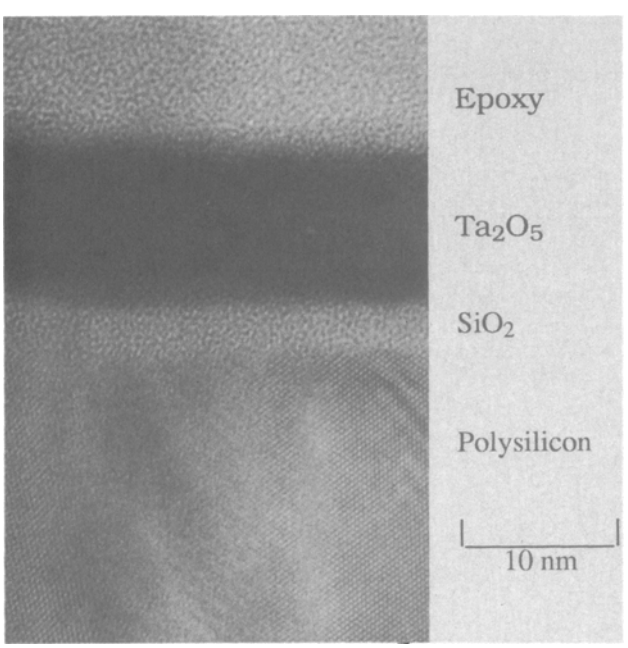

Fig. 3. Cross-sectional TEM of annealed 10 nm Ta_2O_5/3 nm SiO_2/polysilicon: top surface of trench structure.

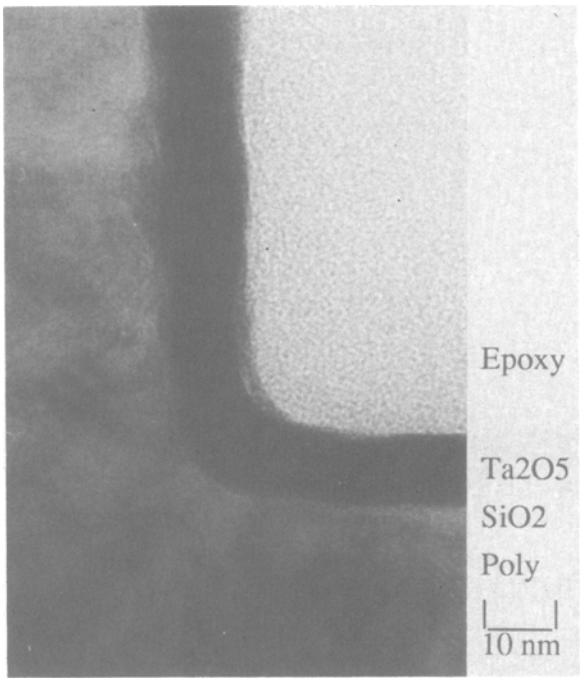

Fig. 4. Cross-sectional TEM of bottom corner of annealed 10 nm Ta_2O_5/polysilicon: bottom corner of trench structure.

trench is approximately 10 nm thick, thus confirming that conformality is ≥90%. A thin amorphous layer is faintly visible at the Ta_2O_5/polysilicon interface. We show later that this is consistent with the presence of a SiO_2-rich layer approximately 2 nm thick which forms during anneal.

Figure 5 is the AFM two-dimensional profile of a (100) prime Si control wafer. It shows the fine structure characteristic of polished Si surfaces. Its rms roughness is 0.4 nm. Figures 6, 7, and 8 are the AFM images of 10 nm Ta_2O_5 films deposited on other Si wafers from the same lot of prime wafers. Figure 6 is the AFM 2-dimensional profile for an unannealed film. It indicates a smooth surface similar to that of the control Si wafer. Its rms roughness is 0.2 nm. From this we conclude that thin Ta_2O_5 films are smooth as-deposited.

Figures 7 and 8 are AFM images of a 10 nm annealed film. Figure 7 shows the three-dimensional surface topography of the film, and Fig. 8 is the 2-dimensional profile of a scan across its surface. The annealed Ta_2O_5 surface shows unexpected surface structure. It is dominated by mounds that are approximately 1 μm in diam, 2 nm in height, and which lie randomly scattered every few micrometers over the wafer surface. Cross-sectional TEM of these films indicates that these mounds are caused by localized thickening of the

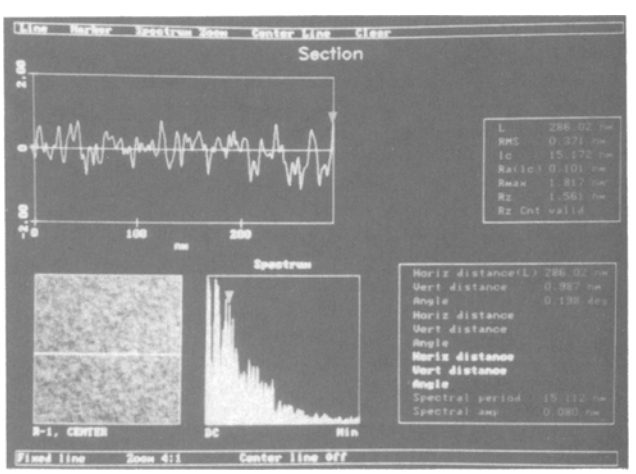

Fig. 5. AFM 2-dimensional profile of <100> Si wafer.

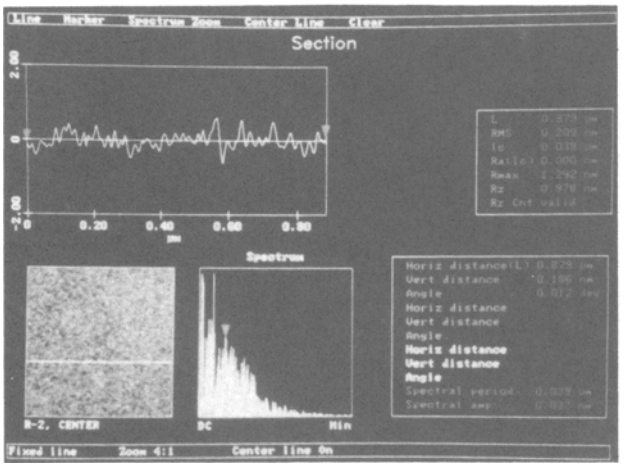

Fig. 6. AFM 2-dimensional profile of 10 nm unannealed Ta_2O_5/Si.

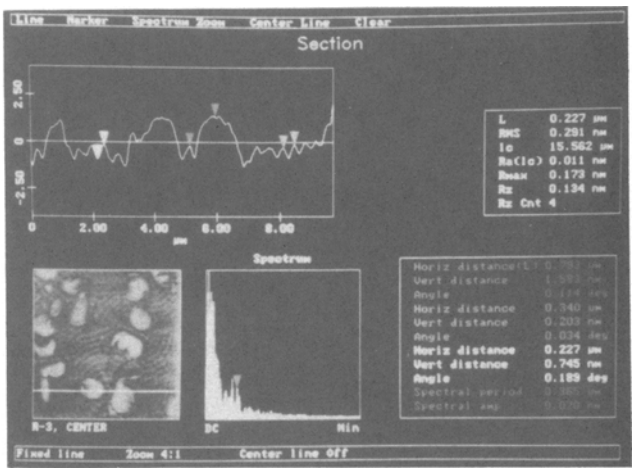

Fig. 8. AFM 2-dimensional profile of 10 nm annealed Ta_2O_5/Si film.

films, not by selective lifting of the film from the substrate. Surrounding these mounds are concentric rough rings that appear to be centered about each mound. At the point where these rings contact each other, they form interference like patterns. We propose that this structure reflects the process of crystallization of the Ta_2O_5 during the anneal. Each mound represents a crystal nucleation site, and the rings represent polycrystalline nucleation fronts that radiate outward from the central nucleation site. Sites which nucleate the earliest during the anneal have the largest rings surrounding them. This AFM image would explain the findings of grain boundaries and weak spots previously reported in Ta_2O_5.[10,21,22]

Figure 9 is a plan TEM image of the same 10 nm annealed film seen in Fig. 7 and 8. It shows remarkable crystalline structure, and is similar to images of annealed sputtered Ta_2O_5 previously published.[21,22] Most of the Ta_2O_5 crystals are highly elongated. They range in size from about 0.1 μm wide to several micrometers long. The dark bands that appear in the crystals are bend contours, artifacts of the TEM process. There are two distinct regions in the TEM image. In the center, there is a round mass of relatively small Ta_2O_5 crystals approximately 1 μm in diam. We feel this is one mound, or nucleation center, imaged by AFM in Fig. 7 and 8. Surrounding it, there are regions of large elongated parallel crystals. These crystals may represent the nucleation rings imaged by AFM. This surface structure for 10 nm films also is visible clearly with Nomarski interference contrast microscopy, though not in the detail afforded by AFM and TEM.

The surface roughness demonstrated by AFM and TEM may have a considerable impact on $C_{max} - C_{min}$ for DRAM capacitors. Assuming the capacitor has a ≤10 nm Ta_2O_5, one expects $C \approx 9$ fF/cm^2 based on the C_{max} and C_{min} data given above. To obtain the 35-40 fF needed for a typical DRAM storage cell,[23] the DRAM capacitor must be approximately 4 μm^2 in area. This area is significant because the size of the capacitor is approximately the same as the size of the nonuniform surface structure of the annealed Ta_2O_5. If a storage capacitor lies on top of a mound, it probably has markedly different capacitance from one that does not lie on such a mound, possibly as much as several percent. The mean thickness of the Ta_2O_5 is greater for the capacitor on the mound, and the dielectric constants of the Ta_2O_5 under each capacitor may be different due to different orientation of the crystals in the mound *vs.* those in the surface surrounding it.[17] This potential problem must be studied carefully during device integration of Ta_2O_5.

Electrical Data.—I-V measurements have been made on the films using a quasi-static measurement technique. The voltage on the sample is stepped and held for several seconds, then the current is sampled. This sampling provides more accurate leakage current measurements than swept voltage because it eliminates the spurious displacement currents (charging of the MOS capacitor) inherent in swept voltage measurements. The noise floor for these quasi-static I-V measurements is in the mid to high 10^{-11} A/cm^2 range.

Figure 10 shows the current density *vs.* voltage measurement for four Ta_2O_5 films on p-type Si substrates. The samples were illuminated so that an inversion layer of electrons forms at the oxide/Si interface when biased into depletion. The films are 10 nm as-deposited, and 10, 19, and 39 nm annealed. The leakage current for the unannealed

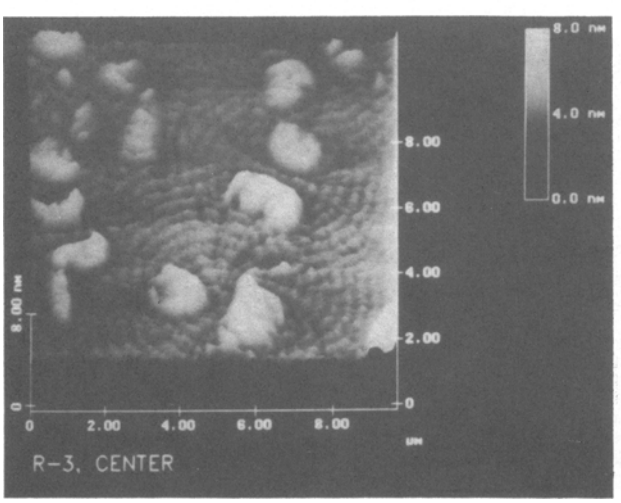

Fig. 7. AFM 3-dimensional topograph of 10 nm annealed Ta_2O_5/Si.

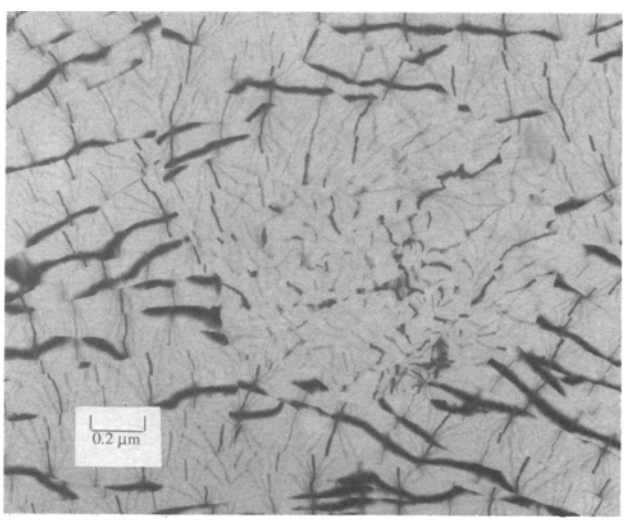

Fig. 9. TEM image of 10 nm annealed Ta_2O_5 film.

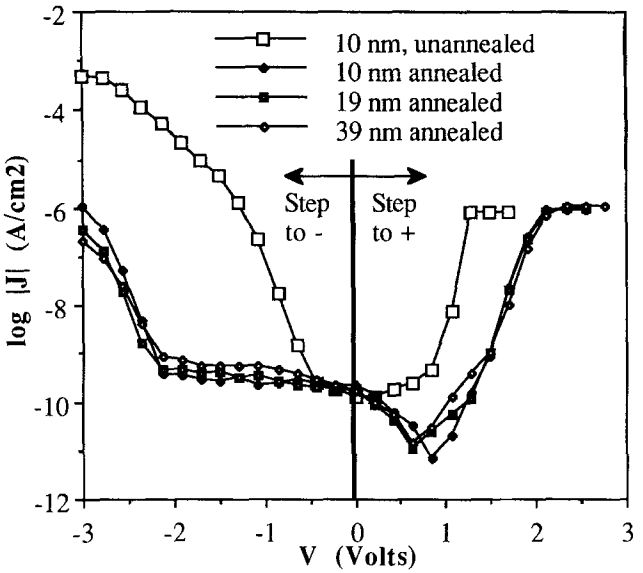

Fig. 10. Current density *vs.* voltage for Ta_2O_5/Si.

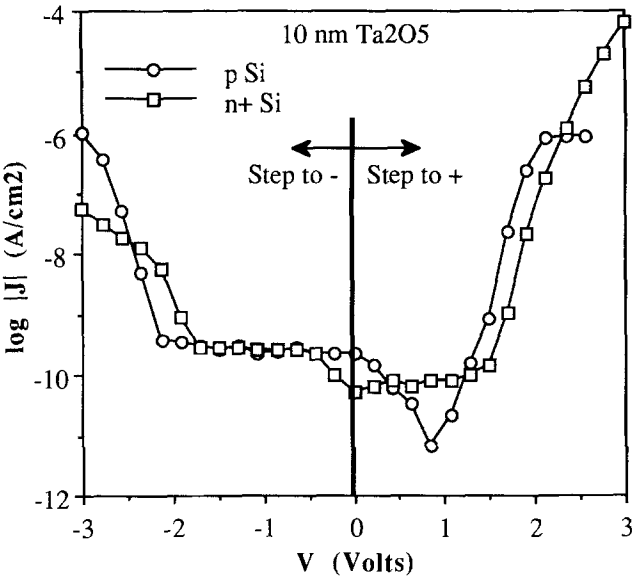

Fig. 12. Current density vs. voltage for annealed Ta_2O_5 on p-type and on n^+ Si.

Ta_2O_5 is several orders of magnitude higher than for annealed Ta_2O_5. This higher magnitude demonstrates the necessity for annealing Ta_2O_5 to get acceptable leakage currents.

The leakage currents for the 10, 19, and 39 nm annealed films are almost identical to each other, with the thinner films being slightly superior to the thicker ones. This superiority indicates that the leakage current of thin annealed Ta_2O_5 is virtually independent of the film thickness over a wide range of applied voltages (−3 V to +3 V). Some factor other than the thickness of the annealed Ta_2O_5 film limits its leakage current. The data are replotted in Fig. 11 as a function of calculated electric field in the Ta_2O_5, the method normally used to plot Ta_2O_5 I-V data. It is apparent that this approach obscures the simple pattern evident in Fig. 10, and hence is a less desirable format.

The minimum in leakage current that occurs between +0.5 and 1 V in Fig. 10 appears to be due to flatband voltage shift of the MOS capacitors by negative charge in the oxide or at the oxide/Si interface. All the J-V curves saturate at about 10^{-6} A/cm^2 for positive biases. This saturation implies that the dominant leakage current mechanism for these samples under positive bias is injection of photogenerated minority carriers (electrons) at the oxide/Si interface.

Figure 12 is a comparison of leakage current data for 10 nm annealed Ta_2O_5 on p-type and n^+ Si substrates. They are comparable except that the current for the n^+ Si does not saturate in forward bias (accumulation) and the n^+ Si does not exhibit the minimum in leakage current present for p-type Si at 0.5 to 1 V. The data appear to be shifted 0.25 to 0.5 V relative to each other, with the n^+ J-V data shifted more positive than the p-type data.

Figure 13 is a comparison of J-V curves for three annealed Ta_2O_5 films, all 10 nm thick: (*i*) n^+ Si, (*ii*) n^+ polysilicon, and (*iii*) 3 nm of SiO_2 deposited on n^+ Si. The SiO_2 was deposited from HMDSo and O_3 by the process in Table II. The J-V curves for n^+ Si and n^+ polysilicon are nearly identical up to +1.5V. This similarity is typical of our results with polysilicon, which exhibits nearly identical leakage current behavior to <100> Si. 1.5 V is generally accepted as the maximum voltage used for storage capacitors in 64 Mbyte and 256 Mbyte low power DRAMs.[12,20,23] Leakage current is ≤1*e*-9 A/cm^2 for both n^+ Si and n^+ polysilicon at this voltage.

We deposited the SiO_2 between the Ta_2O_5 and the Si for two reasons: to control the Ta_2O_5/Si interface during anneal and to determine its effect on the leakage currents and effective dielectric constants of Ta_2O_5. Leakage currents are

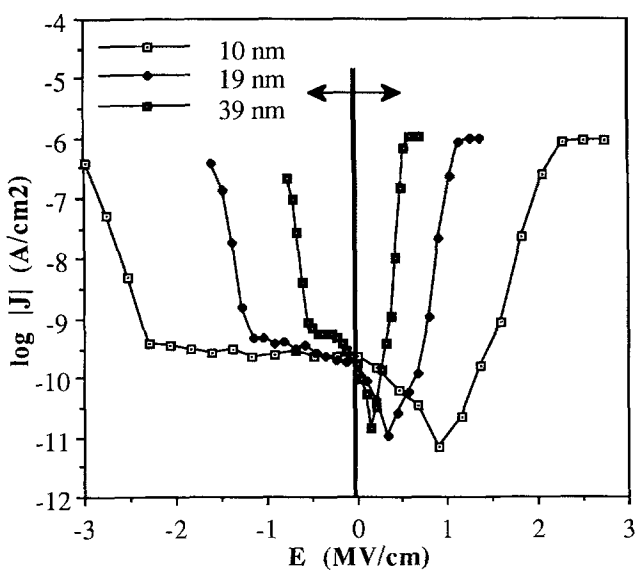

Fig. 11. Current density *vs.* electric field for Ta_2O_5/Si.

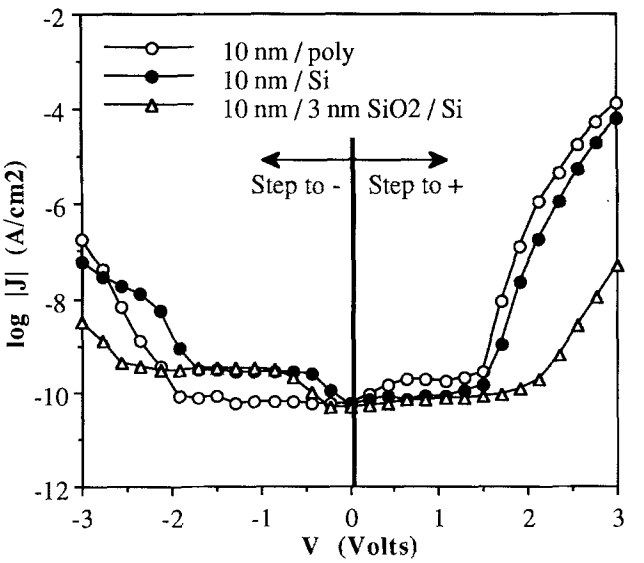

Fig. 13. Current density vs. voltage for annealed Ta_2O_5 on n^+ Si, n^+ polysilicon, and 3 nm CVD SiO_2/n^+ Si.

Table III. Effective dielectric constants of Ta_2O_5 films.

Ta_2O_5 thickness (nm)	Substrate	Annealed	ϵ_{eff}	$t_{ox,eff}$ (nm)	Ta_2O_5 dielectric constant
7.5	<100> Si	yes	8.3	3.5	24
10	<100> Si	no	12.4	3.1	N/A
10	<100> Si	yes	9.9	3.9	24
10	3 nm CVD SiO_2/ <100> Si	yes	9.4	4.1	N/A
18	<100> Si	yes	13.9	5.0	26
19	<100> Si	yes	15.0	4.9	28
26	<100> Si	yes	18.5	5.5	32
39	<100> Si	yes	24.2	6.2	39

lower and breakdown voltages higher with the 3 nm of SiO_2 than for Ta_2O_5 on a bare Si surface. As is shown in Table III, this improvement was achieved with little effect on the effective dielectric constant and equivalent oxide thickness of the film. We also saw a significant improvement in interfacial and bulk electron trapping for the samples with the interfacial CVD SiO_2 layer. We present these data in detail in a future publication.

Table III lists the effective dielectric constants (ϵ_{eff}) and equivalent SiO_2 thicknesses ($t_{ox,eff}$) for various Ta_2O_5 layers deposited on Si wafers. As shown in Fig.14, the effective dielectric constant of annealed Ta_2O_5 films rises with increasing thickness. This trend has been reported previously, and has been attributed to the formation of a SiO_2-rich layer at the Ta_2O_5/Si interface during anneal.[10,13,14] The thin amorphous layer we observe in Fig. 4 at the Ta_2O_5/polysilicon interface is consistent with the presence of a SiO_2 layer after anneal. Such a layer may form either due to reaction of the Si with oxygen that has diffused through the Ta_2O_5, or due to a solid-phase reaction between the Ta_2O_5 and the Si. When we fit a second-order polynomial to the data, the extrapolated curve intersects the y-axis (ϵ_{eff}) at 3.7, close to the dielectric constant of SiO_2.

The SiO_2 and the Ta_2O_5 layers act as series capacitors. Because the dielectric constant of SiO_2 is so much lower than that of the annealed Ta_2O_5, generally reported as about 25,[6-8] the SiO_2 layer dominates the effective dielectric constant of the film for thin Ta_2O_5 layers, causing it to decrease. Also, the effective dielectric constant for the 10.0 nm film is lower after anneal (9.9) than before (12.4). This effect probably is due to the growth of the interfacial SiO_2 layer during anneal.

Figure 15 is a graph of equivalent oxide thickness $t_{ox,eff}$ *vs.* the thickness of the annealed Ta_2O_5 CVD layer. $t_{ox,eff}$ falls with decreasing Ta_2O_5 thickness. Its lowest value is 3.5 nm

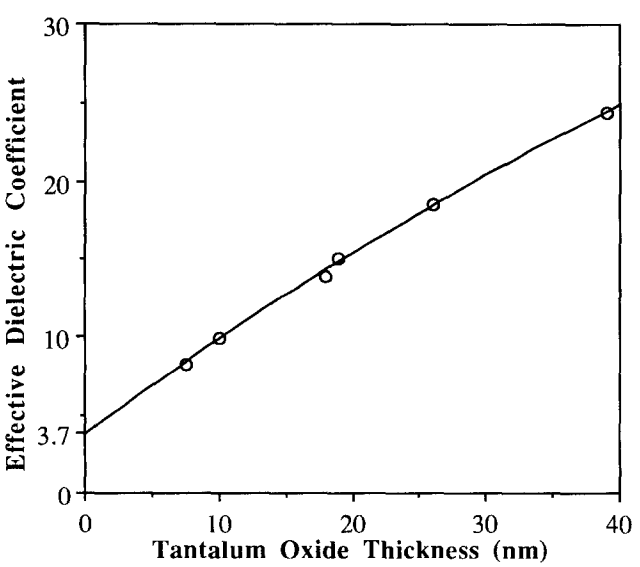

Fig. 14. Effective dielectric constant *vs.* annealed Ta_2O_5 film thickness.

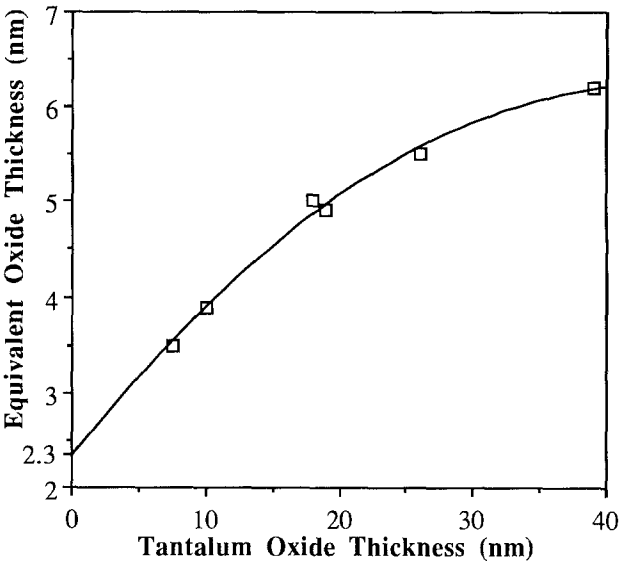

Fig. 15. Equivalent oxide thickness vs. annealed Ta_2O_5 film thickness.

for 7.5 nm Ta_2O_5. If we fit a second-order polynomial to the data, it intersects the $t_{ox,eff}$ axis at about 2.3 nm. This figure agrees with interfacial SiO_2 layer thicknesses reported by other authors.[9,11,14]

Table III includes a calculation, using a series capacitance model, of the actual dielectric constant of annealed Ta_2O_5/Si assuming that there is 2.3 nm SiO_2 at the Ta_2O_5/Si interface. For Ta_2O_5 thicknesses less than about 20 nm, the calculated dielectric constant of the Ta_2O_5 is nearly constant and is between 24 and 28. For films greater than 20 nm, the calculated dielectric constant of the Ta_2O_5 layer rises with increasing thickness. This effect may be due to changes in the properties of thicker Ta_2O_5 layers.[12,17,22]

These results explain the invariance of leakage current with Ta_2O_5 thickness shown in Fig. 10. The behavior of the dielectric constant data for thin Ta_2O_5 is explained by the presence of a thin, constant-thickness SiO_2 layer at the Ta_2O_5/Si interface. If the resistance of this layer is significantly higher than that of the Ta_2O_5 layers which overlie it, then the overall resistance of the film is dominated by the SiO_2 layer and is constant. Ta_2O_5 thickness does not have a significant effect on leakage current. Leakage current instead is dependent on the voltage across the film, not the computed electric field in the Ta_2O_5.

As noted above, 3.5 nm is the $t_{ox,eff}$ which we expect from the Ta_2O_5/Si system for 7.5 nm Ta_2O_5. Assuming that the leakage current of even thinner films continues to be dominated by the SiO_2-rich interfacial layer, the lower practical limit of $t_{ox,eff}$ for the Ta_2O_5/Si system is approximately 30 nm. This is the value which one calculates for 5 nm of Ta_2O_5 (e = 24) on about 2 nm of SiO_2. Thus, Ta_2O_5/Si dielectrics are applicable to 64 Mbyte DRAMs.[12,23]

These films, however, may not be applicable to 256 Mbyte and larger DRAMs which need equivalent oxide thicknesses no greater than 2.5 nm.[20] If Ta_2O_5 is to be used in such applications, then one must find a way to reduce or eliminate the formation of SiO_2 at the Ta_2O_5/Si interface while still retaining acceptable leakage currents. One way to do this would be to reduce SiO_2 formation with a shorter or lower temperature anneal cycle, though it has been our experience that this reduction leads to higher leakage currents. Another way may be to use rapid thermal anneal (RTA) instead of furnace anneal to reduce SiO_2 formation, although we anticipate that this process has a similar effect on leakage current.

Another way to reduce $t_{ox,eff}$ while still retaining acceptable leakage currents may be to place a physical barrier between the Ta_2O_5 and the Si that prevents oxidation of the Si, has a high dielectric constant, and has a high enough resistance for acceptably low leakage currents. This barrier

appears to be the most practical solution to the problem. Encouraging work with silicon nitride has been reported in this area[20,24] and more needs to be done.

Summary and Conclusions

High quality Ta_2O_5 films have been deposited by LPCVD. Tantalum pentaethoxide ($Ta(OC_2H_5)_5$) and oxygen were used as reactants. Our results are summarized as follows:

1. The films are stoichiometric as deposited and have carbon contamination levels below the sensitivity of AES.
2. Thickness reproducibility is ≤1% for 10 nm films. Run-vent plumbing is needed to obtain this reproducibility. Across-the-wafer thickness uniformity is ≤1.2% for 150 nm wafers. Wafer temperature variation must be no greater than ±1.5°C.
3. As-deposited and annealed films are highly conformal (>90%) with excellent coverage at the bottom corners of 0.35 μm wide ×1.0 μm deep trenches.
4. As-deposited films are amorphous with smooth surfaces. Annealed films are polycrystalline. The surfaces of 10 nm thick films are characterized by 2 nm high, 1 μm diam mounds surrounded by polycrystalline rings. These mounds appear to be nucleation sites, and the rings crystallization fronts.
5. This mound-ring structure could cause device integration problems because capacitors are approximately the same size as the surface structure. This similarity may cause excessive capacitance variation across a wafer.
6. The films must be annealed to obtain acceptable leakage currents. Leakage currents for 10 to 40 nm thick annealed films are independent of gate voltage. They are ≤10^{-9} A/cm^2 for a gate voltage of 1.5V.
7. Annealed Ta_2O_5 films on n^+ <100> Si and n^+ polysilicon exhibit similar electrical behavior.
8. The effective dielectric constant decreases with decreasing Ta_2O_5 thickness as does the equivalent oxide thickness, $t_{ox,eff}$. The smallest observed $t_{ox,eff}$ value was 3.5 nm for 7.5 nm of Ta_2O_5 on Si.
9. The leakage current and $t_{ox,eff}$ behavior can be explained by the presence of a thin, ≈2 nm SiO_2 layer at the annealed Ta_2O_5/Si interface. This SiO_2 layer dominates the leakage current and $t_{ox,eff}$ for thin Ta_2O_5 films.
10. Due to the presence of the thin SiO_2 layer, the minimum $t_{ox,eff}$ for Ta_2O_5/Si is on the order of 3 nm. This makes Ta_2O_5/Si suitable for 64 Mbyte DRAM use, but may preclude its use in 256 Mbyte DRAMs.
11. To obtain lower $t_{ox,eff}$ values with Ta_2O_5, we probably must incorporate an antioxidation barrier between the Ta_2O_5 and the Si or polysilicon substrate. This barrier must be thin, have low leakage current, and have a higher dielectric constant than SiO_2.

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