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A. Ritenour, A. Khakifirooz, D. A. Antoniadis, R. Z. Lei, W. Tsai, A. Dimoulas, G. Mavrou, and Y. Panayiotatos

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Subnanometer-equivalent-oxide-thickness germanium *p*-metal-oxide-semiconductor field effect transistors fabricated using molecular-beam-deposited high-*k*/metal gate stack

A. Ritenour, A. Khakifirooz, and D. A. Antoniadis
Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139

R. Z. Lei[a] and W. Tsai
Technology Manufacturing Group, Intel Corporation, Santa Clara, California 95054

A. Dimoulas, G. Mavrou, and Y. Panayiotatos
MBE Laboratory, Institute of Materials Science, National Center for Scientific Research Demokritos, 153 10, Athens, Greece

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Metal-oxide-semiconductor field effect transistors (MOSFET) with a thin high-*k* dielectric were fabricated on bulk *n*-type germanium substrates. Surface oxides were thermally desorbed *in situ* by heating the substrates under ultrahigh vacuum conditions. First an ultrathin passivating layer was formed by evaporating germanium in the presence of atomic oxygen and nitrogen supplied from a remote radio frequency plasma source. Subsequently, the HfO_2 dielectric was deposited by evaporating hafnium in the presence of atomic oxygen. An *in situ* TaN metal gate was similarly deposited. Long channel devices were fabricated using a standard process flow. These devices exhibited a low equivalent oxide thickness (EOT) of 0.7 nm with gate leakage less than 15 mA/cm^2 at $V_{FB}+1$ V. Device mobility was extracted from I_s-V_g and split *C*-*V* characteristics. Results indicate a 2× mobility enhancement in Ge *p*-MOSFET devices compared to Si control devices. The demonstration of subnanometer EOT suggests that high-*k* gate dielectrics on germanium are scalable to low EOT and suitable for use in ultrascaled MOSFET devices. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2189456]

Improving metal-oxide-semiconductor field effect transistor (MOSFET) performance through traditional device scaling is becoming increasingly difficult. Future improvements in performance will require high mobility semiconductor channels[1] such as germanium. One of the main obstacles in realizing Ge transistors is the lack of a good quality germanium oxide. This can be circumvented by using high-*k* gate dielectrics[2] that have been extensively investigated over the last few years for Si-based devices.

Since the demonstration of functional MOSFETs on bulk Ge channels with ZrO_2 (Ref. 3) and HfO_2 (Ref. 4) gate dielectrics, there has been significant progress showing performance improvement in strained Ge channels.[5,6] Several other papers have demonstrated deep submicron Ge *p*-MOSFETs from a 200 mm pilot processing line[7] and good quality Ge MOSFETs on heterogeneous Ge-on-Si (Ref. 8) and Ge-on-insulator (GOI).[9] *p*-MOSFETs show the best performance while *n*-MOSFETs show inferior device characteristics for reasons that are not completely understood at the present time. Much of the Ge transistor research thus far involves HfO_2 gate dielectrics with thin GeON interfacial layers. Subnanometer equivalent oxide thickness (EOT) has been measured using HfO_2/Ge metal-insulator-semiconductor capacitors[10] including those prepared by molecular beam epitaxy/deposition (MBE/MBD) techniques.[11,12] However, all functional transistors reported thus far have an EOT larger than 1 nm raising concerns about the dielectric scalability in HfO_2/Ge MOSFETs. In addition, no results are available on transistors with MBE/MBD-prepared gate stacks despite the fact that this method offers alternative surface preparation techniques[12,13] that could improve Ge device performance. In this work we report Ge *p*-MOSFETs with MBE/MBD-prepared TaN/HfO_2 gate stacks exhibiting capacitance equivalent thickness (CET) of 1.1 nm, which corresponds to 0.7 nm equivalent oxide thickness (EOT) after quantum mechanical correction.

The high-*k*/metal gate stacks were prepared on *n*-type (100) Ge substrates ($\rho \sim 0.025\ \Omega$ cm) by molecular beam deposition that is described in detail elsewhere.[12,13] The native oxide was thermally desorbed *in situ* by heating the Ge substrate to 360 °C for 15 min in ultrahigh vacuum.[12,13] An ultrathin Ge oxynitride layer was then deposited by evaporating Ge at 0.05 Å/s in combined atomic oxygen and nitrogen beams generated by a remote radio frequency plasma source.[13] HfO_2 was then deposited at 225 °C in an O_2 partial pressure of 4×10^{-6} Torr by evaporating hafnium at a rate of 0.15 Å/s in the presence of atomic oxygen supplied by the plasma source. The TaN gate metal was subsequently deposited at room temperature immediately after the oxide deposition without breaking vacuum. Tantalum was evaporated at a rate of 0.3 Å/s in the presence of atomic nitrogen supplied by the plasma source. During gate metal deposition, the N_2 partial pressure was approximately 1×10^{-5} Torr. The thicknesses of the HfO_2 and TaN layers were 5 and 70 nm, respectively, as measured by tunneling electron microscopy. Control samples with TaN/HfO_2 gate stacks on *n*-type Si ($\rho \sim 0.5\ \Omega$ cm) were also prepared by the same method, although the native oxide on the Si surface was desorbed

[a]Electronic mail: rzlei@mtl.mit.edu

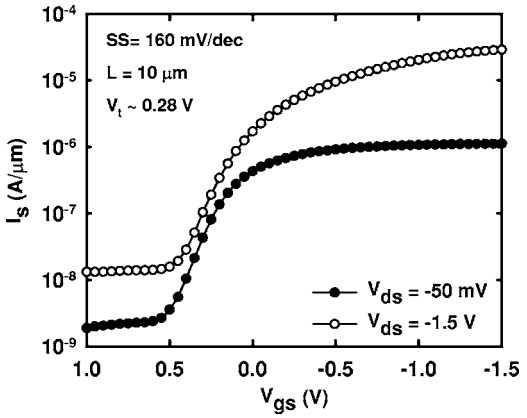

FIG. 1. Typical as-measured I_s-V_g characteristics for Ge *p*-MOSFETs. The current was measured at the source to eliminate drain junction leakage. The devices exhibited a 0.28 V threshold voltage and 160 mV/decade subthreshold swing.

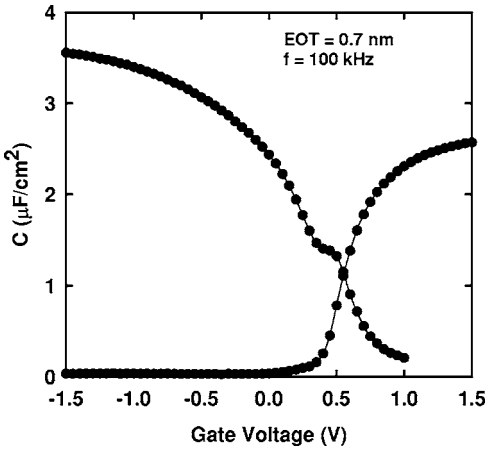

FIG. 3. Typical as-measured split *C-V* characteristics for Ge *p*-MOSFETs. The maximum inversion capacitance corresponds to a CET of 1.1 nm and EOT of 0.7 nm after quantum mechanical correction.

in situ at much higher temperature (810 °C). HfO_2 was deposited directly on the clean Si surface without an interfacial layer.

MOSFET devices were fabricated using a standard process flow. Ring-type structures with gate lengths of 5, 10, and 20 μm were used to eliminate the need for isolation. The TaN gate electrode was etched using CF_4-based reactive ion etching. The source-drain (S/D) regions were implanted with 3×10^{15} cm^{-2} BF_2 at 40 keV. Following S/D implantation, the HfO_2/GeO_xN_y stack was removed with buffered oxide etchant (BOE). Next, S/D activation was performed at 400 °C for 30 min in N_2, followed by PECVD oxide deposition, contact photolithography, and contact etching. 30 nm Ti/450 nm Al metallization was deposited using electron beam evaporation. Finally a postmetal anneal was performed at 300 °C for 30 min in forming gas (8% H_2 in N_2) at atmospheric pressure.

Typical as-measured characteristics for 10 μm gate length Ge *p*-MOSFETs are shown in Figs. 1–3. Figure 1 shows the I_s-V_g characteristics. The current was measured at the source to exclude the effect of drain junction leakage to the substrate. The devices exhibited a 0.28 V threshold voltage, 160 mV/decade subthreshold swing, and ON/OFF current ratio greater than 10^3 for a supply voltage of −1.5 V. The positive threshold voltage and high subthreshold swing suggest elevated interface trap and oxide charge densities.

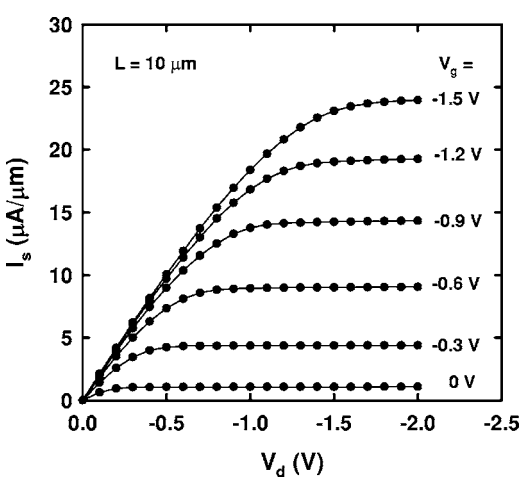

FIG. 2. Typical as-measured I_s-V_d characteristics for Ge *p*-MOSFETs.

Figure 2 shows typical I_s-V_d characteristics. Figure 3 shows the split C-V characteristics of these devices at 100 kHz. The peak inversion capacitance corresponds to a CET of 1.1 nm (without quantum mechanical correction). An EOT of 0.7 nm was extracted by analyzing the inversion side of the split C-V characteristics using Schred[14] which accounts for quantum mechanical effects by self-consistently solving the Poisson and Schrödinger equations. Effective mass approximations were modified within Schred to reflect Ge parameters. The metal work function and body doping were adjusted to fit the threshold voltage and the minimum capacitance in the full split C-V characteristics. With the HfO_2 physical thickness fixed at 5 nm, the dielectric constant was modified to fit the inversion capacitance. The extracted EOT value was confirmed by analyzing the accumulation capacitance of MOS capacitors fabricated in parallel on the same wafer.

Figure 4 shows the typical gate leakage for 10 μm gate length devices and capacitors with an area of 2.5×10^{-5} cm^2. At $V_{FB}+1$ V in accumulation, the MOSFET gate leakage is less than 15 mA/cm^2. This low gate leakage compares favorably to the leakage reported by Tsai *et al.*[15] for 0.75 nm EOT $TiN/HfO_2/Si$ *p*-MOSFET devices (less than 5 A/cm^2 at $V_{FB}+1$ V).

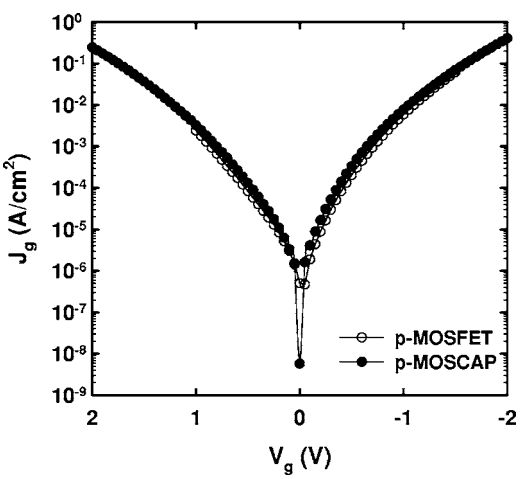

FIG. 4. Typical as-measured gate leakage for *p*-MOSFETs with a gate area of 6.6×10^{-5} cm^2 and capacitors with an area of 2.5×10^{-5} cm^2. At 1 V, the gate leakage for both is less than 3 mA/cm^2. The EOT for these devices is 0.7 nm.

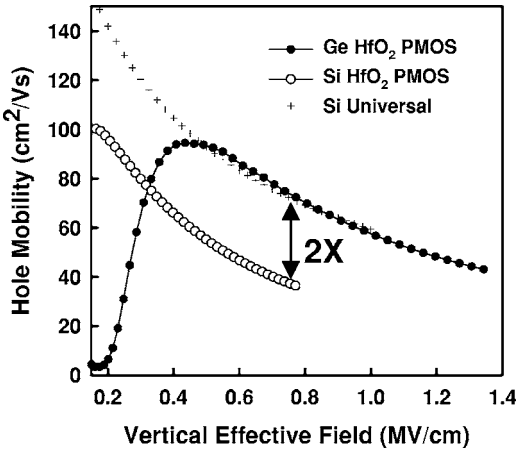

FIG. 5. Comparison of extracted hole mobility for Ge and Si control *p*-MOSFETs. The Ge devices show 2× enhancement compared to Si controls and match the Si-SiO_2 universal curve.

Figure 5 shows the extracted hole mobility of the Ge and Si control *p*-MOSFET devices. The carrier mobility was extracted using the integrated inversion charge (Q_{inv}) obtained from the inversion side of the split *C-V* and I_s-V_g data from the same device. The vertical effective field (E_{eff}) was taken as $(|Q_b|+|Q_{\text{inv}}|/3)/\varepsilon_{\text{Ge}}$, where Q_b was calculated from the body doping. Compared to the silicon control devices, Ge *p*-MOSFETs with MBD deposited TaN/HfO_2 gate stack show 2× enhancement in hole mobility. There was no enhancement compared to Si-SiO_2 universal mobility, which suggests that the surface passivation process needs further optimization in order to achieve the enhancement expected from comparing the bulk hole mobilities of silicon and germanium.

In conclusion, 0.7 nm EOT Ge *p*-MOSFETs with MBD-prepared TaN/HfO_2 gate stacks were demonstrated. This EOT was achieved with low gate leakage and suggests that the alternative surface preparation techniques available in MBD offer advantages over conventional processes. These devices exhibited reasonable performance as indicated by drive current, ON/OFF current ratio, and mobility. The hole mobility was enhanced by a factor of 2 compared to $TaN/HfO_2/Si$ control devices.

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