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Fabrication of n^+/p InP solar cells on silicon substrates

C. J. Keavney, S. M. Vernon, V. E. Haven, and S. J. Wojtczuk Spire Corporation, Patriots Park, Bedford, Massachusetts 01730

M. M. Al-Jassim Solar Energy Research Institute, Golden, Colorado 80401

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In P solar cells were fabricated from films deposited by metalorganic chemical vapor deposition on Si substrates (using a GaAs buffer layer) and on GaAs substrates. Air mass zero efficiencies of 7.1% and 9.4%, respectively, were achieved. Prospects are good for improving the material quality of the InP films, but more work is needed to make the n^+ -p- p^+ structure of the InP solar cells compatible with the silicon substrates, which cause *n*-type doping of the III-V films.

Recently, much effort has been devoted to the study of InP solar cells for space applications. This work was sparked by the discovery that exposure to radiation, as in earth orbit, causes less damage to the photovoltaic performance of these cells than to that of GaAs or Si cells. Furthermore, the damage which is done can be annealed at a relatively low temperature.^{1,2} The development of high-efficiency InP-based solar cell structures has proceeded quickly^{3–9}; efficiencies up to 18.8% AM0 (air mass zero, 25 °C) have been measured.³ Theory predicts an attainable beginning-of-life efficiency for this material nearly the same as that for GaAs. Because of the superior radiation resistance, this would correspond to a considerably higher end-of-life efficiency in typical space applications than any other known material.

The chief disadvantage of InP from a photovoltaic point of view is its cost. The cost could presumably be reduced in the face of a large demand for space solar cells, but is not expected to be much lower than GaAs. The largest commercially available InP wafers are of 75 mm diameter.

Another disadvantage of InP which is particularly important for space applications is its density (4.8 g/cm³). Although the active region of an InP solar cell is only about 3 μ m thick, the low mechanical strength of the material would make handling of cells less than 150 μ m very difficult. This corresponds to 72 mg/cm², or 2.7 g/W.

The use of Si substrates addresses both of these problems. Silicon wafers are commercially available in sizes up to 200 mm diameter, at costs which would contribute negligibly to the final cost of space solar cells. Si has a lower density than InP (2.3 g/cm³), and is considerably stronger. 50- μ mthick cells, which weigh only 12 mg/cm², are currently produced for space applications.

GaAs cells on silicon substrates have been investigated for several years, and some recent advances have been made. The minority-carrier lifetime in the material has been improved greatly by techniques such as thermal cycling, annealing, and the incorporation of strained-layer superlattices.^{10–13} Dislocation densities as low as 2×10^6 cm⁻² (Ref. 11) and efficiencies over 18% AM0 have been reported.¹² Since a recent theoretical study¹⁴ projected achievable efficiencies of 18% with InP if a dislocation density of 10^6 cm⁻² or less could be achieved, these results make InP on silicon solar cells a promising avenue of research.

In this work, n + /p - /p + InP films were grown by

metalorganic chemical vapor deposition (MOCVD) on Si substrates using GaAs buffer layers, and on GaAs substrates. InP substrates were also included as controls. All substrates were p type. MOCVD growth was carried out at atmospheric pressure in a Spire-manufactured system, model SPI-MO CVDTM 450. The InP deposition was done at 600 °C using trimethylindium and phosphine. The GaAson-Si growth used a three-step process¹⁵ consisting of a hightemperature (1000 °C) hydrogen bakeout, a low-temperature (400 °C) nucleation step, and GaAs film growth at 675 °C; the sources were trimethylgallium and arsine. Figure 1 shows a cross-sectional transmission electron micrograph of a typical InP/GaAs/Si structure; the dislocation density increases at each interface, then decreases again as the growth continues. Thermal cycling, annealing, or superlattices were not employed. The final dislocation density in the InP film was estimated at 3×10^8 cm⁻², as shown in Fig. 2. No cracks were observed in the films.



FIG. 1. Cross-sectional transmission electron micrograph of a typical InP/GaAs/Si structure. The dislocation density increases at each interface but decreases as the growth continues. InP thickness is $4 \mu m$; GaAs thickness is $1 \mu m$.



FIG. 2. Plan-view transmission electron micrograph of an InP film grown on a Si substrate (with a GaAs buffer layer). The dislocation density is approximately 3×10^8 cm⁻². The InP thickness is 4 μ m and the GaAs thickness is 1 μ m.

Solar cells were fabricated from these wafers using techniques established with homoepitaxial InP solar cells.⁴ Junction depths from 20 to 100 nm were used. The emitter (n +)and base (p -) doping densities were varied from 1 to 2×10^{18} cm⁻³ and from 3 to 6×10^{16} cm⁻³, respectively, but the effects of doping level were found to be not large enough to measure in this work. Contact to the substrate was made with Au-Zn alloy to the GaAs wafers, and with Al-Ti-Pd-Ag to the silicon wafers. Contact to the front was made with Cr-Au-Ag. A ZnS/MgF₂ antireflection coating was applied. The final cell area was 0.25 cm² and shadow loss amounted to approximately 5%.

Efficiency measurements of these cells were made with a Spectrolab X25 AM0 solar simulator at 25 °C. The light intensity was calibrated using a silicon reference cell. We have found previously that the silicon reference cell results in a measurable spectral mismatch error, but this was neglected because of the preliminary nature of this work. Efficiency was calculated based on the total area of the cell, and using a value of 137.2 mW/cm^2 for the solar constant.

It was found that the cells on the silicon substrates showed very low open-circuit voltages and fill factors, which decreased with increasing light level. The cause of this effect was traced to non-ohmic behavior at the Si/GaAs interface, which formed a second diode opposing the InP solar cell. These cells were measured by short circuiting the InP and GaAs buffer layers to the substrate at the periphery of the cell, so that the current could flow out to the edge of the cell through the p + buffer layers. Since the sheet resistivity of the *p*-type GaAs and InP layers is expected to be about 125 Ω , considerable resistance was still present, resulting in fill factors lower than those seen with GaAs substrates.

In each case the thinnest emitters yielded the highest efficiencies, consistent with the results obtained with InP substrates. Table I gives the measurements of the best cells,

TABLE I. Comparison of InP cells formed on Si, GaAs, and InP substrates. Measurements were made under air mass zero conditions, 137.2 mW/cm^2 , at 25 °C, and currents and efficiencies are calculated on a total area basis.

Open-circuit Short-circuit					
Cell No.	Structure	voltage (mV)	current (mA/cm ²)	Fill factor	Efficiency (%)
499as5	InP/GaAs/Si	636	25.58	0.601	7.1
499ag5	InP/GaAs	672	27.40	0.701	9.4
4970-6	InP/InP	868	33.88	0.838	17.9

compared to previous results with InP substrates.⁴

Spectral response and reflectance were made using a monochromator and a calibrated reference cell. Figure 3 shows the internal quantum efficiency for the three groups described in Table I. The spectral response at the red end is similar for the GaAs and Si substrates, indicating that the two lattice-mismatched interfaces together are no worse than one.

The low red response seen in Fig. 3 shows that, as expected, the InP films on foreign substrates have low carrier lifetimes, due to the high defect concentration. This is comparable to the case with GaAs-on-Si material when no annealing or other dislocation reduction techniques are used.

The voltage barrier at the GaAs-Si interface may be attributed to incorporation of Si in the GaAs during growth. Secondary-ion mass spectrometry measurements¹⁶ have shown that such incorporation does occur to the extent of 10^{19} cm⁻³ or more, although the electrically active fraction is unknown. If the silicon concentration in the GaAs is high enough to form an *n*-type layer between the *p*-type Si and the *p*-type GaAs, then a reverse diode will be formed, and behavior such as that we saw would be expected. Since all the GaAs-on-Si work,¹⁰⁻¹³ and the only other published result with InP-on-Si,¹⁷ are p + /n structures on *n*-type substrates, this problem has not been noted before. However, n + /pstructures currently yield the highest efficiencies in InP.

Theoretically, it should be possible to create a tunnel junction between this *n*-type layer and the *p*-type base of the cell by making the doping levels very high and the transition abrupt. Low band-gap materials such as $In_{0.53}Ga_{0.47}As$ may be helpful in this regard. It may also be possible to increase the *p*-type dopant concentration in the GaAs buffer layer



FIG. 3. Spectral response of InP cells on GaAs and Si substrates. The low red response is the result of a high defect density. The response of a homo-epitaxial InP cell is shown for comparison.

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sufficiently to prevent the formation of the reverse junction entirely. If neither of these approaches is successful, a twolevel metallization which connects the base of the cell to the substrate would allow large cells to be made without losses from the reverse junction, although at some cost in complexity.

These results show that, while lattice-mismatched films still suffer from high defect density, the exact value of the mismatch does not have a strong effect; the 8% mismatch between InP and Si can be accommodated in such a way that it does not result in more defects than the 4% mismatch between GaAs and Si. Furthermore, cracks in the heteroepitaxial film do not occur with InP, because of the lower growth temperature and better thermal expansion match.

The radiation tolerance of InP cells stems not only from a resistance to damage on the part of the lattice, but also from the optical absorption coefficient of InP, which is higher than that of GaAs over most of the spectrum, so that more light can be collected with the same diffusion length. This fact should make InP cells more tolerant of grown-in defects, such as the dislocations discussed here, than GaAs cells.

We can conclude, then, on the basis of this preliminary work, that prospects are good for high InP efficiencies on GaAs substrates, and on Si substrates as well if the problem of doping from the substrate can be overcome.

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