Investigation of the Effects of Very Low Pressure Chemical Vapor Deposited $TiSi_2$ on Device Electrical Characteristics

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ABSTRACT

We report for the first time the effects of very low pressure chemical vapor deposited (VLPCVD) titanium silicide on device electrical characteristics. The compatibility of this material for VLSI technology is examined through careful characterization of the shallow junction and gate oxide integrities, sheet resistance, and contact resistivity. It is shown that the integrity of the shallow junctions is preserved if the silicon consumption during the silicide deposition is controlled. If this consumption is not controlled, a Schottky diode behavior is observed for the source/drain junctions. It is shown that titanium silicide lowers the specific contact resistivity of metal/source-drain and metal/polysilicon structures by an order of magnitude and a factor of 4-5, respectively. The sheet resistance of the doped polysilicon (gate conductor) is reduced by more than two orders of magnitude through using a $TiSi_2$/polysilicon structure. In addition, it is shown that VLPCVD titanium silicide has no significant effect on the quality of the gate oxide. Slightly lower breakdown voltages for the $TiSi_2$/polysilicon capacitors are measured, which could be due to the stress induced by siliciding the gate. The results presented in this paper indicate the suitability of VLPCVD titanium silicide films for high quality device fabrication.

Vertical and lateral scaling of device dimensions have led to the speed enhancement of metal-oxide-semiconductor (MOS) transistors, and thus have led to an enhancement of the circuit performance. Scaling of device dimensions has also brought to attention the physical reliability limitations imposed by the metallization materials, such as integrity of shallow junctions, contact electromigration, etc. Addressing the reliability issue has driven the investigation of refractory metal silicides that have high conductivity, high temperature stability, and compatibility with existing process technologies.

We chose to investigate the very low pressure chemical vapor deposition (VLPCVD) of titanium silicide due to its low resistivity compared to the other refractory metal silicides ($TaSi_2$, WSi_2, and $MoSi_2$), and the low annealing temperature (~700°C) required to form this silicide (1), if necessary. A CVD approach was chosen due to its capability for excellent conformal coverage, which has become very important as device dimensions have scaled down. The potential advantages of the VLPCVD titanium silicide films for integrated circuit applications were investigated through fabrication of MOS devices, and contact and sheet resistances test structures. Exploration of these advantages necessitated the optimization of the deposition conditions by studying the relationship between the process variables and the deposition kinetics (2, 3).

A high vacuum system, located in a class 100 clean room, has been designed and built for the VLPCVD of titanium silicide. The details of this reactor are available elsewhere (3, 4). Briefly, the system is a cold wall reactor with the wafer being heated by radiant heating. A turbomolecular pump is used to obtain not only base pressures less than 10^{-7} torr, but also a contamination-free environment. SiH_4 and $TiCl_4$ are used as silicon and titanium sources, respectively. Smooth, reproducible, low resistivity (15-20 μΩ-cm) titanium silicide films have been successfully deposited in this reactor for a $SiH_4/TiCl_4$ flow rate ratio of 20/2, a pressure of 67 mtorr, and a temperature of 730°C (2, 3). The reactor has the capability of sequential deposition of materials, each at different temperatures.

The impact of VLPCVD titanium silicide on device electrical characteristics has been studied through fabrication of MOS transistors, capacitors, diodes, cross-bridge Kelvin and tapped resistor test structures. These test structures facilitated the determination of shallow junction integrity, gate oxide integrity, and contact and sheet resistance values. Hewlett Packard 4145 and 4275 measurement systems were used for the electrical measurements of the test devices. In this paper, we report for the first time the results of an investigation of the effects of VLPCVD titanium silicide on device electrical characteristics.

Experimental

The device fabrication schedule was based on the fabrication of n-channel MOS (NMOS) transistors. Two batches of wafers were processed: silicided source/drain contacts, and silicided gate. The starting substrates were 100 mm Czochralski-grown, (100) orientation, 18-25 Ω-cm, p-type silicon wafers. Table I summarizes the device fabrication schedule. In this fabrication process, the source/drain implant was used to simultaneously dope the polycrystalline silicon (polysilicon). It has been previously shown that titanium silicide does not nucleate on oxide, and any native oxide on polysilicon can inhibit the silicide nucleation (5). Thus, for the polycide transistors it was necessary to deposit the polysilicon in the VLPCVD reactor immediately before the silicide deposition. A two-etch process was used to etch the polycide structure. A wet chemical etch was used to remove the titanium silicide, and an SF_6 plasma etch was used to remove the polysilicon. Oxidation steps proceeding the titanium silicide deposition did not pose a problem, such as decomposition of the silicide, since a silicon layer was always present under the silicide during the oxidation. This underlying silicon layer provided the necessary silicon to form silicon dioxide (6). A sintering temperature-time combination of 400°C for 15 min was chosen to prevent junction spiking due to aluminum penetration into the shallow source/drain junction.

A SUPREM III process simulator (7) was used to design the impurity profiles and junction depth in the source/drain region, and to calculate the threshold voltages in the field and gate oxide regions. The dose and energy of the source/drain implant were carefully chosen to obtain a shallow junction of ~2100Å. The channel and field oxide implants were designed for threshold voltages of 0.56 and 25V, respectively. NMOS transistors were designed with a minimum channel length (L) and width (W) of 20 μm each to simplify the fabrication process.

Results and Discussion

Silicided source/drain contacts.—This section presents the results of the characterization of the silicided source/drain contact regions and their impact on the integrity of the shallow junctions. Titanium silicide was deposited onto the contacts of the source/drain regions after opening the contact holes to prevent the bridging short between source/drain and gate regions. The silicide deposition was then followed by sputtered Al:1% Si to form the final metallization layer. The metal sandwich was etched to form the final metal pattern.

Table II summarizes the contact properties of titanium silicide to the polysilicon and diffusion areas. Table II also

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Table I. Fabrication schedule for the silicided gate and silicided source/drain NMOS transistors

- Grow 400Å oxide at 950°C
- Field oxide implant, B^+, 70 keV, 3×10^{12} cm^{-2}
- Grow 5000Å field oxide at 950°C
- Scribe wafers into quarters
- Lithography, define active area
- Grow 200Å gate oxide at 950°C
- Enhancement channel implant, B^+, 100 keV and 30 keV, 5×10^{11} cm^{-2}
- Deposit 2000Å polysilicon
- For silicided gate, deposit 2000-2500Å of CVD titanium silicide
- Lithography, gate definition
- Implant source/drain and polysilicon, As, 60 keV, 7×10^{15} cm^{-2}
- Back-side strip
- Regrow undercut gate oxide at 900°C
- Deposit 6000Å CVD oxide
- Densify CVD oxide at 950°C
- Lithography, open contact holes
- For silicided source/drain, deposit ~2000Å CVD titanium silicide
- Sputter deposit 5000Å Al/1% Si
- Lithography, metal definition
- Sinter in forming gas (80% N_2:20% H_2) at 400°C

Table II. Contact properties of titanium silicide. Silicide1 is deposited under excess silicon consumption conditions, while silicide2 is deposited under the optimum conditions

	Specific contact resistance ($\mu\Omega$-cm^2)			
	Poly/metal	S-D/metal	Poly/$TiSi_2$/metal	S-D/$TiSi_2$/metal
Control	178	76.8	—	—
Silicide1	—	—	38.4	1.2
Silicide2	—	—	49.2	1.2

compares the specific contact resistivity of metal/source-drain and metal/polysilicon with that of the metal/$TiSi_2$/source-drain and metal/$TiSi_2$/polysilicon, where metal is sputtered Al:1% Si. In the sandwiched structure of metal/$TiSi_2$/source-drain or polysilicon, the measured specific contact resistivity relates to the specific contact resistivity of the $TiSi_2$/source-drain or polysilicon and not the metal/$TiSi_2$ combination due to the lower conduct resistivity of the metal/$TiSi_2$ structure. The specific contact resistivity is obtained by multiplying the contact resistivity by the contact area of 120 μm^2. Silicide in Table II refers to a condition where the $SiH_4/TiCl_4$ flow rate ratio was much less than 20/2, *i.e.*, a condition presenting excess silicon consumption during the silicidation (3). Silicide2 was deposited using the optimum condition of 20/2. This table demonstrates that siliciding the contact has improved the contact resistance of the metal/source-drain by a factor of 4-5, while the contact resistance of the metal/polysilicon has improved by an order of magnitude. Comparing the specific contact resistivity values in Table II with those reported in the literature, it is observed that the specific contact resistivities reported in the literature are lower by an order of magnitude: 3×10^{-7} Ω-cm^2 for an interface doping concentration of 1×10^{20} cm^{-3} (8), and 1.5×10^{-7} Ω-cm^2 for an interface doping concentration of 3×10^{20} cm^{-3} (9). The higher measured specific contact resistivity for the n^+ diffusion region in this work is possibly due to the lower than 10^{20} cm^{-3} interfacial doping concentration, surface contamination, and/or interfacial oxide. SUPREM III predicted a surface concentration greater than 10^{20} cm^{-3}; however, the silicon consumption during the titanium silicide formation could modify the interfacial doping concentration of the n^+ region (10). Taur *et al.* (8) reported a specific contact resistivity of 1.8×10^{-6} Ω-cm^2 for an interfacial doping concentration of 3×10^{19} cm^{-3}, which is similar to the observed specific contact resistivity to n^+ diffusion in Table II. This suggests that the interfacial doping concentration of the n^+ diffusion is in the low 10^{19} cm^{-3} range due to the segregation and/or redistribution of As ions in the titanium silicide layer during the silicide deposition (10). Surface contamination or interfacial oxide could also contribute to a higher specific contact resistivity due to the nonoptimized contact etching procedure. These two phenomena are process-related artifacts, and thus do not present a limitation to the titanium silicide process. Their effects can be minimized by improving the contact etching step. The high specific contact resistivity of the polysilicon/$TiSi_2$/metal structure is also attributed to the high sheet resistance of the polysilicon layer, as will be discussed in the next section.

Figure 1 shows the reverse bias characteristics of the source diode (n^+-p diode), which is 660 μm^2 in size, for silicide1, silicide2, and control diodes. It is apparent from this figure that the silicide2 diode, which corresponds to the optimum silicide deposition condition, has the same reverse leakage current characteristics as the control diode, which has no silicide in the source region. The silicide1 diode, which represents the excess silicon consumption case, has a very high leakage current, with its behavior resembling a reverse bias Schottky diode. It is believed that the silicide in the silicide1 diode has reached the p-type substrate at several places in the contact region and has formed a Schottky barrier.

Figure 2 shows the forward bias diode characteristics of the same three diodes in Fig. 1. It is observed from Fig. 2 that the silicide2 diode has the same forward bias diode characteristics as the control diode, while the silicide1 diode has a decreased slope in comparison to the other two diodes, indicating a serious deterioration in the junction integrity. The series resistance differences between the diodes (for $V > 0.4$V) is due to the back-side contact being made to the lightly doped substrate with no Al evaporation or p^+ implant. Table III summarizes the reverse bias and forward bias diode characteristics of silicide1, silicide2, and control diodes. The ideality factor n in this table was

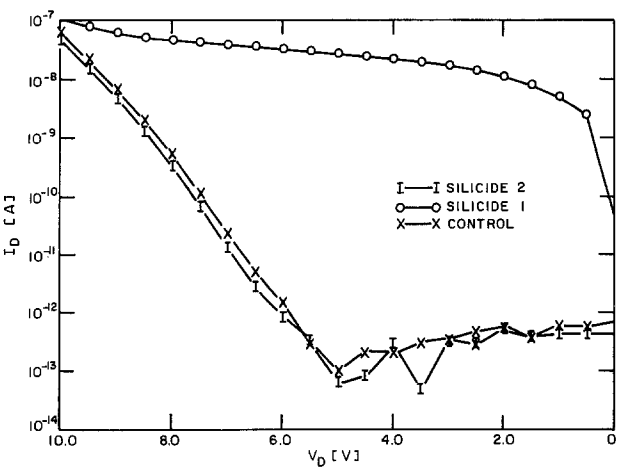

Fig. 1. Reverse bias characteristics of silicide1, silicide2, and control diodes, where the silicide1 diode presents the case of excess silicon consumption during the silicide deposition, and the silicide2 diode presents the case of optimum titanium silicide deposition conditions.

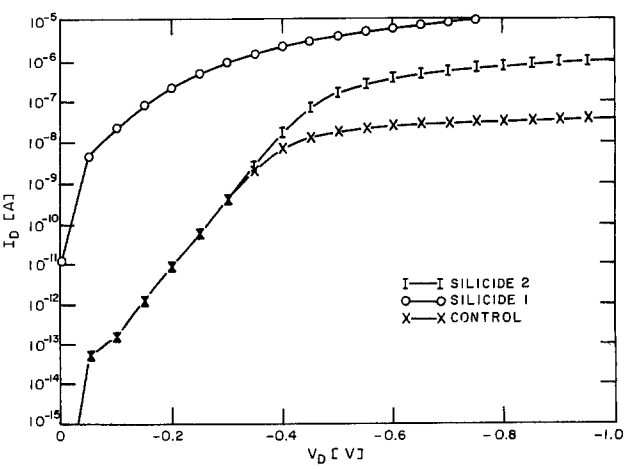

Fig. 2. Forward bias characteristics of the same diodes shown in Fig. 1

Table III. Summary of the reverse bias and forward bias diode characteristics presented in Fig. 1 and 2

	Lifetime (μs)	Ideality	Leakage @ 5V (μA/cm²)
Control	31.5	1.04	<0.1
Silicide1	4×10^{-4}	1.37	$\sim 6.9 \times 10^{3}$
Silicide2	141	1.01	<0.1

extracted through the following empirical expression describing the forward bias I-V characteristics (11, 12)

$$J_F = J_o \exp(qV/nkT) \quad [1]$$

where J_F is the forward bias current density, J_o is a fitting parameter, q is the unit of electron charge, k is the Boltzmann constant, and T is the temperature in degrees Kelvin. The ideality factor ranges from 1 to 2. An ideality factor of one indicates recombination in the neutral material, and thus high quality material. An ideality factor of two indicates depletion region recombination current, and thus poor quality material.

Lifetime of the minority carriers can be extracted either from the reverse or forward bias diodes. In the reverse bias case, the parameter of interest is the generation current, while in the forward bias case the parameter of interest is the depletion region recombination current. If there are no surface depletion effects or edge effects, the lifetimes extracted from either method should yield a similar value. Since surface and edge effects could degrade the reverse bias leakage current, forward bias diodes were used to extract the carrier lifetime. The total forward bias current can be written as follows (11, 12)

$$J_F = J_{diff} \exp(qV/kT) + J_{rec} \exp(qV/2kT) \quad [2]$$

$$\tau = \frac{qn_iW}{2J_{rec}} \quad [3]$$

where J_{diff} and J_{rec} are the diffusion and recombination saturation current densities, respectively, W is the width of the depletion layer, n_i is the intrinsic silicon carrier concentration, and τ is the minority carrier depletion region recombination lifetime.

Table III shows that the silicide2 and the control diodes have similar lifetimes, ideality factors, and reverse bias leakage currents, indicating no degradation in the junction characteristics for the optimized silicide condition. The silicide1 diode has a very high leakage current in conjunction with a poor lifetime and a high ideality factor due to excess silicon consumption during the titanium silicide deposition, which has caused the silicide to reach the p-type silicon substrate at several places, forming a Schottky barrier.

The Schottky behavior of the silicide1 diode can be examined through calculating the barrier height from the forward bias diode characteristics. The barrier height can be obtained from the following expression (13)

$$\phi_B = \frac{kT}{q} \ln \frac{A^{**}T^2}{J_s} \quad [4]$$

where ϕ_B is the barrier height, k is the Boltzmann constant, T is the temperature, A^{**} is the Richardson constant, and J_s is the saturation current density extrapolated from the forward bias characteristics for $V = 0$. The value of ϕ_B is not very sensitive to the choice of A^{**} (13). Choosing a typical value of 30 A/cm²-k² (p-type silicon) for A^{**} (13), ϕ_B can then be calculated to be 0.58 ± 0.02V, which is comparable to the reported barrier height of $TiSi_2$ to p-type silicon substrate (0.56V) (9). The error bar on the calculated barrier height is due to the uncertainty in the area caused by the silicon consumption during titanium silicide deposition.

Figure 3 shows the I_D-V_{DS} characteristics of the silicide1 transistor. The square current-voltage law is observed for this transistor, even though the silicide1 transistor has a poor source/drain leakage current. Thus, silicidation of the source and drain contacts of the NMOS transistors did not affect their characteristics due to the long channel length

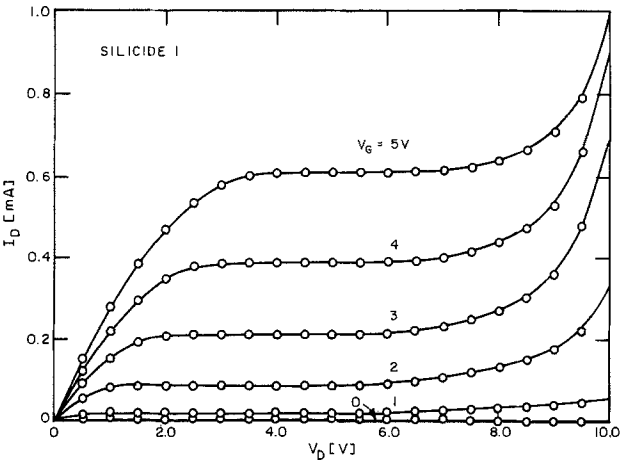

Fig. 3. I_D-V_{DS} characteristics of the silicide1 transistor, W/L = 20/20

of these transistors. In this case, the channel resistance of the transistor was much larger than the source/drain diffusion resistances, and although the silicidation of the source/drain contacts reduced their resistance, this phenomenon did not affect the current driving capability of the long channel transistors. Figure 4 shows the subthreshold I_D-V_{GS} characteristics of silicide1, silicide2, and control transistors. It is observed that all three transistors have the same subthreshold slope of about 80 mV/decade indicating that these transistors are of same quality, *i.e.*, the source/drain contact silicidation has not affected the interface trap density and the channel dopant concentration; however, the silicide1 transistor has a higher subthreshold leakage current.

Silicided gate.—This section presents the results of siliciding the gate of the transistors after the polysilicon deposition using the optimum 20/2 titanium silicide deposition condition. Referring to Table I, the wafers were processed at 950°C after depositing the titanium silicide, which also presents a test of the temperature stability of this material.

Table IV presents the measured sheet resistances of the diffusion, polysilicon, and titanium silicide/polysilicon layers. It is observed from this table that the As-implanted polysilicon has a relatively high sheet resistance. The deposition of titanium silicide on the polysilicon lowered the sheet resistance of the gate structure by two orders of magnitude, clearly showing the suitability of this material for VLSI technology.

Figure 5 shows the I_D-V_{GS} curve for the threshold voltage behavior of the control and the polycide transistors. It is observed from this figure that the threshold voltage for the polycide transistor is shifted from 0.42V (corresponding to V_T of the control) to 0.55V. The shift in the threshold voltage can be due to different interface trap densities and/or different channel doping concentration between the con-

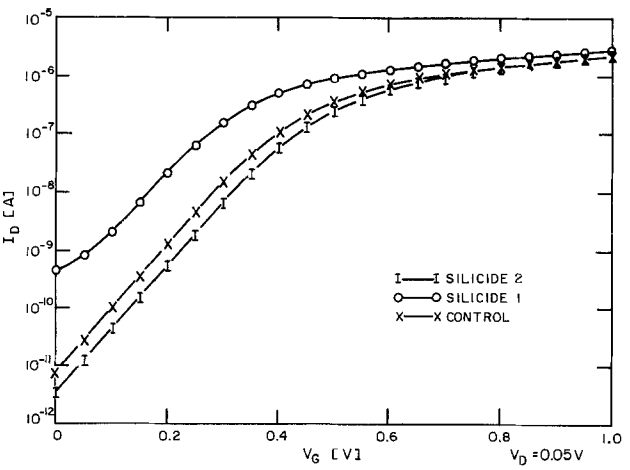

Fig. 4. Subthreshold behavior of silicide1, silicide2, and control transistors.

Table IV. Measured sheet resistances of diffusion, polysilicon, and titanium silicide/polysilicon for the polycide devices

Material	Sheet resistance (Ω/□)
Diffusion	30.5
Polysilicon	348
$TiSi_2$/polysilicon	1.6

trol and the polycide transistors. CV (Fig. 6) and subthreshold (Fig. 7) measurements can both provide additional information regarding these transistors. The CV measurement shown in Fig. 6 was performed on the gate of the NMOS transistors. In this measurement configuration, the inversion layer contacts the source/drain regions, which are forced to the same potential as the bulk. The source/drain regions can then supply and sink electrons for the inversion layer. This measurement configuration facilitates the observation of the low frequency curve at a higher frequency of 1 MHz.

From Fig. 7, subthreshold slopes of 88 and 94 mV/decade are calculated for the control and the polycide transistors, respectively. Assuming that there are no interface trap densities, a channel dopant concentration of 3×10^{16} cm^{-3} is calculated for the control transistor. Performing the same calculations for the polycide transistor by still assuming there are no interface trap densities, a channel dopant concentration of about 4.4×10^{16} cm^{-3} is obtained. Inserting this value of channel dopant concentration into the threshold voltage expression (14) results in a threshold voltage of 0.51V for the polycide transistor, which is within 7% of the measured threshold voltage. This V_T is obtained by neglecting the interface trap densities. The interface trap densities can be estimated by assuming that the polycide transistor has the same channel dopant concentration as the control, *i.e.*, 3×10^{16} cm^{-3}. The subthreshold slope calculations yield a value of 1.1×10^{11} cm^{-2} V^{-1} for the interface trap densities in the polycide transistor; this value was obtained by also assuming that there are no interface trap densities in the control transistor. Examining the CV curve for these two transistors in Fig. 6, it is observed that both transistors have similar slopes in the depletion, weak inversion, and inversion regions. This indicates that both transistors are of comparable quality. However, if the doping concentration in the polycide transistor is different from that of the control and the two slopes are comparable, the interface trap densities between these two transistors are not identical. It is concluded that both different channel doping concentrations and/or interface trap densities could be responsible for the shift in the threshold voltage, even though the separate contribution of each of these variables to the shift in V_T is not known due to the difficulty in decoupling of these components from the available data. The higher interface trap densities can be caused by stress induced during titanium silicide deposition, while the modified channel doping concentration can be due to poor

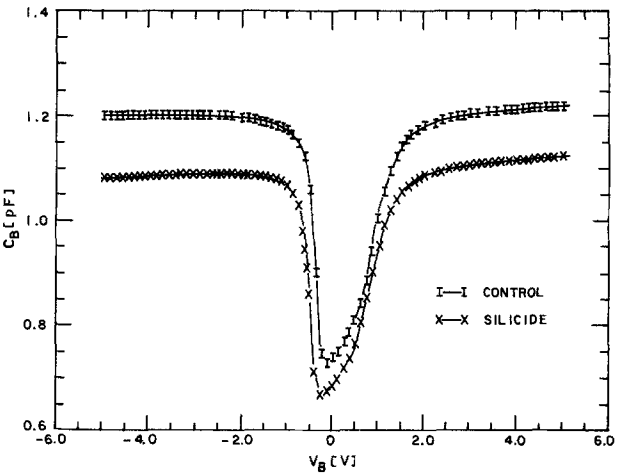

Fig. 6. CV measurements of the control and the silicided MOS gate capacitor at 1 MHz.

control over the repeatability of the channel threshold voltage implant.

The polycide and the control transistors have comparable electrical characteristics, except for the small difference in their threshold voltages. Figure 8 shows that the I_D-V_{DS} characteristics of the two transistors are nearly identical. The shifts in the silicide curve with respect to the control curve is due to the different threshold voltage. There is, however, a slight degradation in transistor breakdown characteristics due to gate silicidation. The gate oxide integrity of the polycide transistors was examined by measuring the gate breakdown voltage. The measured breakdown voltages for the control transistors were in the range of 12.5-15V, while for the polycide transistors the breakdown voltages were in the range of 9-10V. The breakdown voltage is defined as the voltage where the current density exceeds 1 μA/cm². The lower breakdown voltages for the polycide transistor can be due to the stress induced by the gate silicidation. This hypothesis was examined by measuring the breakdown voltage of the capacitors having silicided contacts (silicided source/drain contact batch). In this case, the area of the gate capacitor was covered by 50% titanium silicide and 50% doped polysilicon. Breakdown voltages in the range of 13-15V were measured for these capacitors, indicating that the stress relief of this structure prevented the degradation of the gate oxide. It is important to note that the high temperature processing steps following the titanium silicide deposition did not degrade the quality of the silicide.

Conclusions

This paper reported and discussed for the first time the results of using VLPCVD titanium silicide in device fabri-

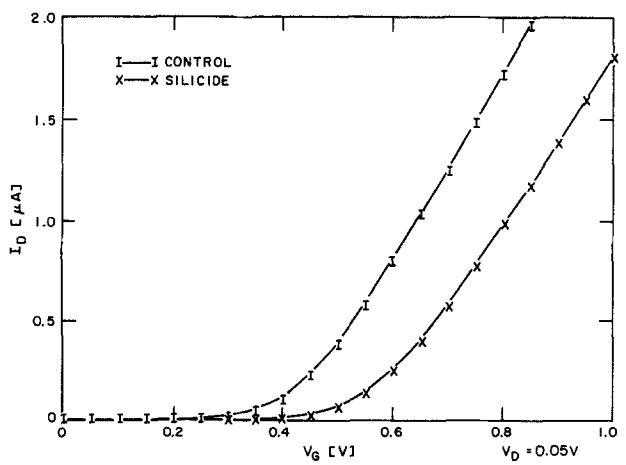

Fig. 5. Threshold voltage characteristics of the control and the polycide transistors.

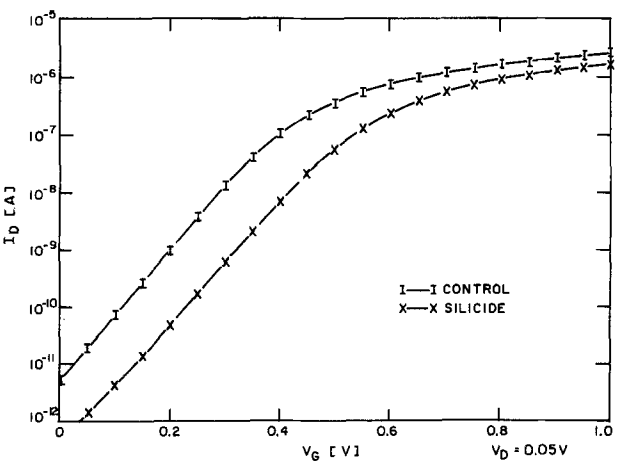

Fig. 7. Subthreshold characteristics of the polycide and the control transistors.

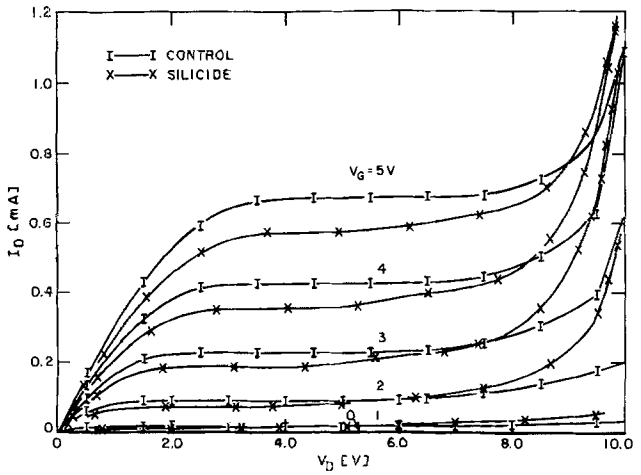

Fig. 8. I_D-V_{DS} characteristics of the polycide and the control transistors

cation. The compatibility of this material for VLSI technology was examined through careful characterization of the shallow junction and gate oxide integrities, sheet resistance, and contact resistivity. It was observed that the integrity of the shallow junctions is preserved if the silicon consumption during the silicide deposition is controlled. If this consumption is not controlled, a Schottky diode behavior is observed for the source/drain junctions with high reverse bias leakage current and poor lifetime and ideality factor. It was also shown that titanium silicide lowers the specific contact resistivity of metal/source-drain and metal/polysilicon structures by an order of magnitude and a factor of 4-5, respectively. The silicided source/drain did not affect the properties of the NMOS transistor.

VLPCVD titanium silicide had little effect on the quality of the gate oxide, where slightly lower breakdown voltages were measured for the polycide capacitors compared to the control capacitors. This is believed to be due to the stress induced by siliciding the gate. The properties of titanium silicide films did not degrade upon exposing the silicided devices to high temperature processing steps. This is observed through subthreshold and I-V characteristics, and the sheet resistance of the silicide. The sheet resistance of the doped polysilicon was reduced by more than an order of magnitude through the use of a polycide structure.

In conclusion, it is important to optimize the VLPCVD titanium silicide deposition conditions to minimize silicon consumption and hence preserve the integrity of shallow junctions and gate oxides. Optimized VLPCVD titanium silicide deposition conditions can additionally result in a lowering of the sheet and specific contact resistances.

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REFERENCES

1. S. P. Murarka, "Silicides for VLSI Applications," Academic Press, New York (1983).
2. V. Ilderem, J. Lee, and R. Reif, Abstract 1058, p. 1467, The Electrochemical Society Extended Abstracts, Vol. 87-2, Honolulu, HI, Oct. 18-23, 1987.
3. V. Ilderem and R. Reif, *This Journal*, **135,** 2590 (1988).
4. R. Reif, Prabha K. Tedrow, and V. Ilderem, U.S. Pat. No. 4,668,530 (May 1987).
5. V. Ilderem and R. Reif, *Appl. Phys. Lett.*, **53,** 687 (1988).
6. M. Tanielian, R. Lajos, S. Blackstone, and D. Pramanik, *This Journal*, **132,** 1456 (1985).
7. C. P. Ho and S. E. Hansen, SUPREM III, Tech. Report No. SEL83-001, Integrated Circuits Laboratory, Stanford University, Stanford, CA.
8. Y. Taur, J. Y-C Sun, D. Moy, L. K. Wang, B. Davari, S. P. Klepner, and C-Y Ting, *IEEE Trans. Electron Devices*, **ED-34,** 575 (1987).
9. J. Hui, S. Wong, and J. Moll, *IEEE Electron Device Lett.*, **EDL-6,** 479 (1985).
10. P. Revesz, J. Gyimesi, and E. Zsoldos, *J. Appl. Phys.*, **54,** 1860 (1983).
11. S. M. Sze, "Physics of Semiconductor Devices," 2nd ed., Chap. 2, John Wiley and Sons, New York (1981).
12. A. S. Grove, "Physics and Technology of Semiconductor Devices," Chap. 6, John Wiley and Sons, New York (1967).
13. S. M. Sze, "Physics of Semiconductor Devices," 2nd ed., Chap. 5, John Wiley and Sons, New York (1981).
14. S. M. Sze, "Physics of Semiconductor Devices," 2nd ed., Chap. 8, John Wiley and Sons, New York (1981).

A Kinetics Study of the Atmospheric Pressure CVD Reaction of Silane and Nitrous Oxide

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ABSTRACT

A mechanistic study of oxide deposition from silane and nitrous oxide between 495°C and 690°C was performed in a laminar flow, cool wall reactor. Results indicated the existence of two distinct chemical pathways. At high nitrous oxide concentrations, the deposition reaction is dominated by radical chain chemistry initiated by the decomposition of N_2O. At lower N_2O concentrations, the decomposition of silane to form silylene (SiH_2) initiates the deposition. Studies of the reaction of disilane and nitrous oxide confirmed the role of SiH_2 in the deposition. Reactions involving SiH_2 are used to explain the observed growth of sub-stoichiometric oxides under low N_2O conditions.

Extensive use has been made of the chemical vapor deposition (CVD) reaction of silane and nitrous oxide to deposit silicon dioxide thin films. This reaction system is particularly important because sub-stoichiometric oxide can be deposited under appropriate reaction conditions (1). Non-stoichiometric silicon oxide films have been used in a wide variety of electronics applications, from solar cells to read-only memories (2). Practical interest has spawned considerable research into the structure and material properties of non-stoichiometric oxides (1, 3-14). However, investigations of the chemical processes associated with the deposition have been limited. Hitchman and co-

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